

# SN54F74, SN74F74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDFS046A – MARCH 1987 – REVISED OCTOBER 1993

- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

### description

These devices contain two independent positive-edge-triggered D-type flip-flops. A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

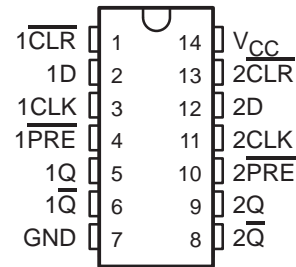
The SN54F74 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74F74 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

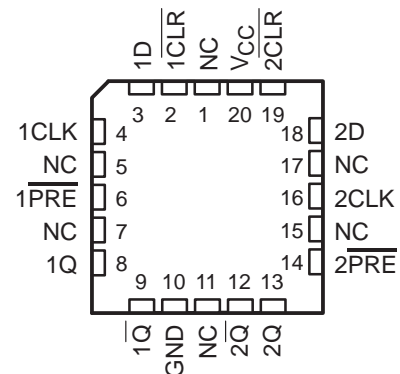
INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	$\text{H}^{\dagger}$	$\text{H}^{\dagger}$
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	L	X	$\text{Q}_0$	$\overline{\text{Q}}_0$

$\dagger$  The output levels are not guaranteed to meet the minimum levels for  $\text{V}_{\text{OH}}$ . Furthermore, this configuration is nonstable; that is, it will not persist when  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

SN54F74 ... J PACKAGE  
SN74F74 ... D OR N PACKAGE  
(TOP VIEW)



SN54F74 ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

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[illegible][illegible]

Supply voltage range, $V_{CC}$	−0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	−1.2 V to 7 V
Input current range	−30 mA to 5 mA
Voltage range applied to any output in the high state	−0.5 V to $V_{CC}$
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F74	−55°C to 125°C
SN74F74	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

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### recommended operating conditions

		SN54F74			SN74F74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current			–1			–1	mA
$I_{OL}$	Low-level output current			20			20	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F74		SN74F74		UNIT
				MIN	TYP†	MAX	MIN	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$				–1.2	–1.2	V
$V_{OH}$		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -1\text{ mA}$		2.5	3.4	2.5	3.4	V
		$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -1\text{ mA}$				2.7		
$V_{OL}$		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 20\text{ mA}$		0.3	0.5	0.3	0.5	V
$I_I$		$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1		0.1	mA
$I_{IH}$		$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20		20	μA
$I_{IL}$	Data, CLK	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.5\text{ V}$			–0.6		–0.6	mA
	PRE or CLR				–1.8		–1.8	
$I_{OS}^\ddagger$		$V_{CC} = 5.5\text{ V}$ , $V_O = 0$		–60	–150	–60	–150	mA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ , See Note 2		10.5	16	10.5	16	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with D, CLK, and PRE grounded then with D, CLK, and CLR grounded.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54F74		SN74F74		UNIT
			'F74						
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		0	100	0	80	0	100	MHz
t <sub>w</sub>	Pulse duration		CLK high, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4	4	4		ns	
			CLK low	5	6	5			
t <sub>su</sub>	Setup time, data before CLK↑	High	2	3	2		ns		
		Low	3	4	3				
	Setup time, inactive-state before CLK↑§	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ to CLK	2	3	2				
t <sub>h</sub>	Hold time, data after CLK↑	High	1	2	1		ns		
		Low	1	2	1				

§ Inactive-state setup time is also referred to as recovery time.



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## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH CLEAR AND PRESET

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#### switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			'F74			SN54F74		SN74F74		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			100	145		80		100		MHz
t <sub>PLH</sub>	CLK	Q or $\overline{Q}$	3	4.9	6.8	3.8	8.5	3	7.8	ns
t <sub>PHL</sub>			3.6	5.8	8	4.4	10.5	3.6	9.2	
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	2.4	4.2	6.1	3.2	8	2.4	7.1	ns
t <sub>PHL</sub>			2.7	6.6	9	3.5	11.5	2.7	10.5	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9759201Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9759201QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9759201QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/34101B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/34101BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/34101BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SN54F74J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN74F74D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74F74DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74F74N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74F74N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74F74NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ54F74FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54F74J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54F74W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

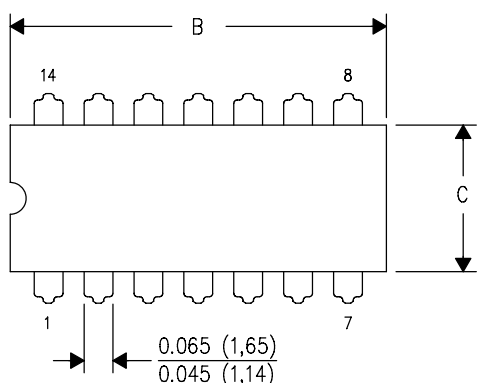
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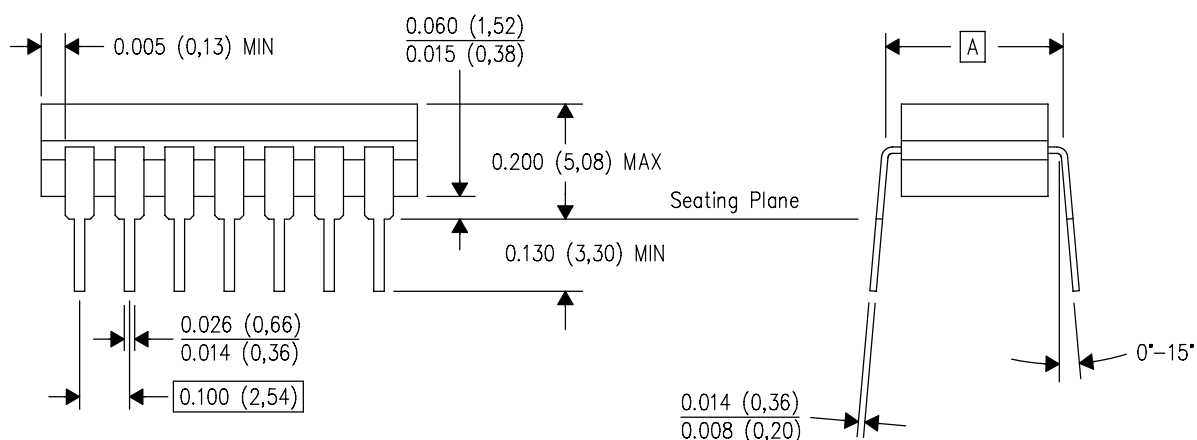
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

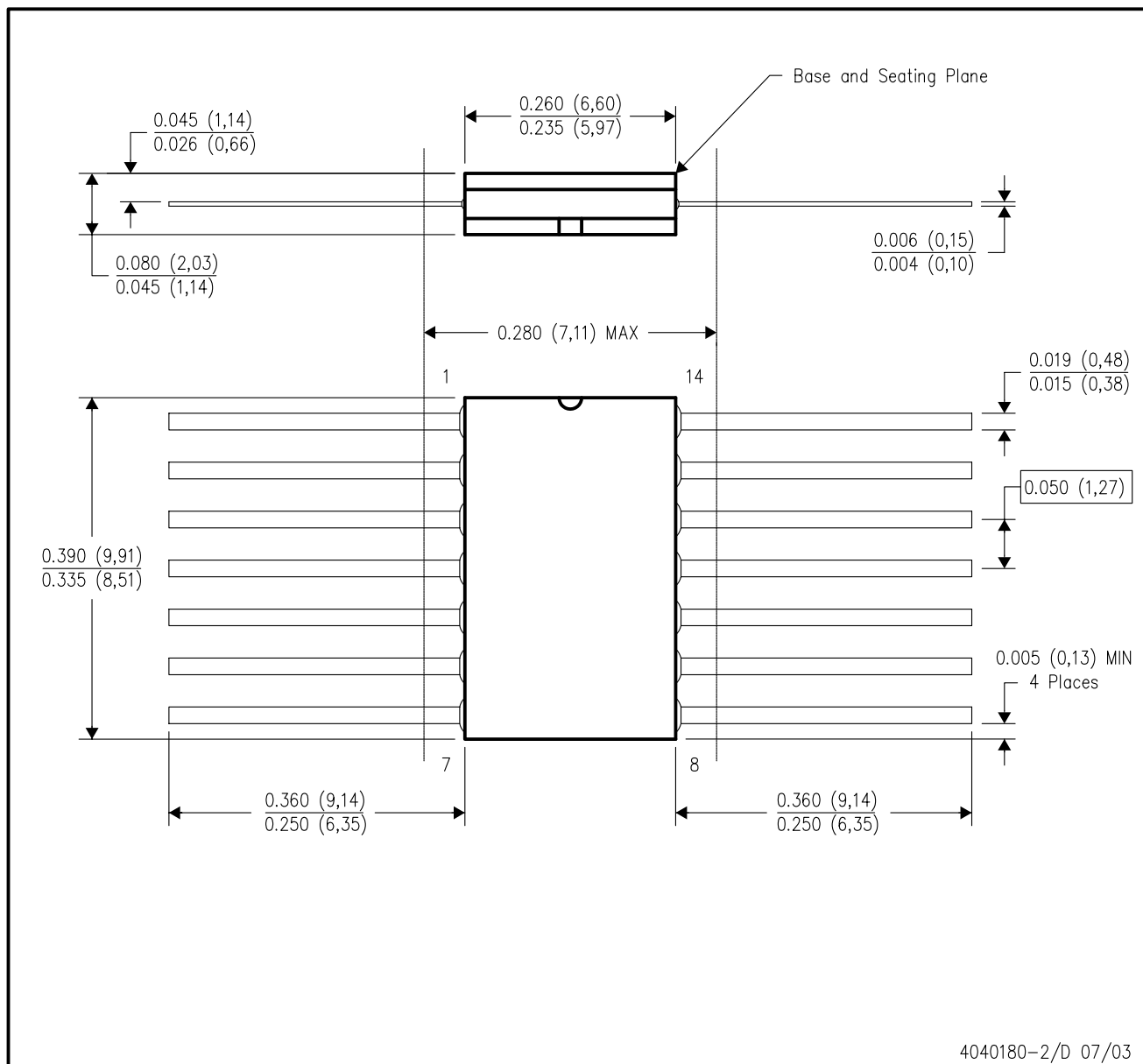


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

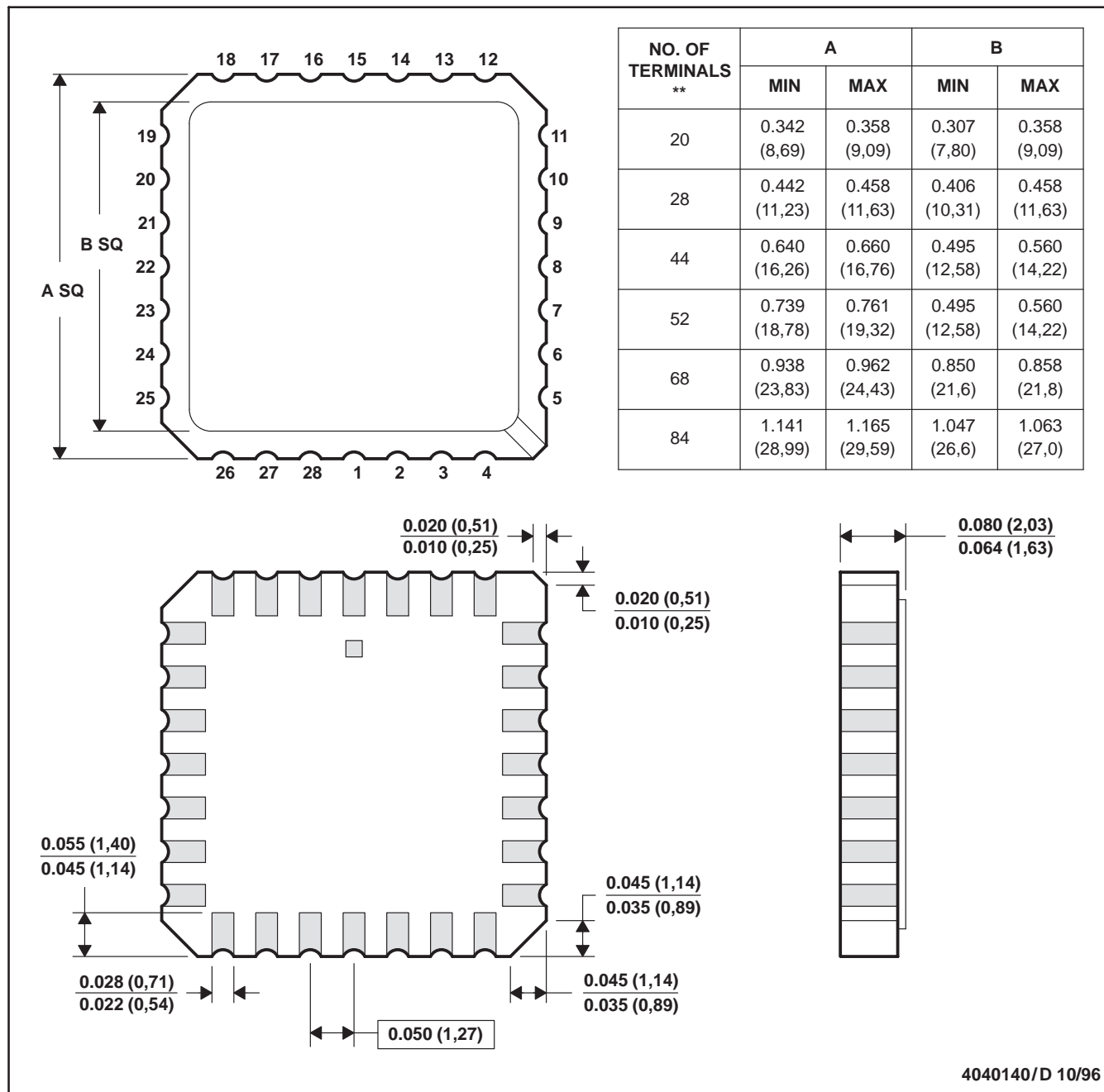


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

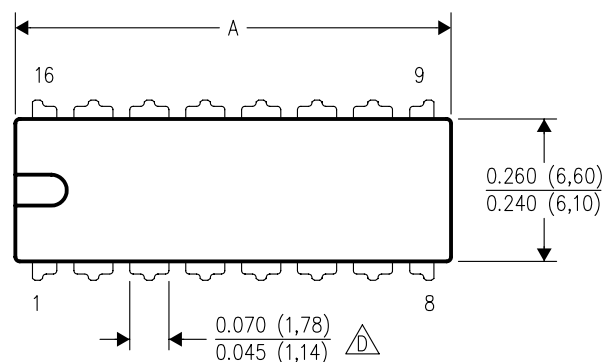


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

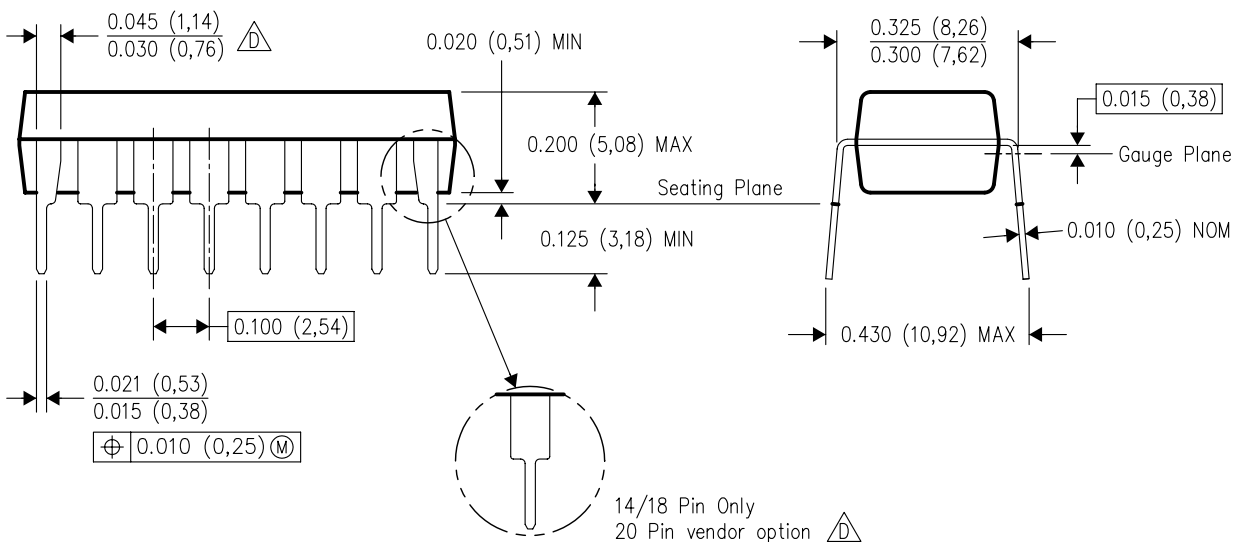
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE





PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



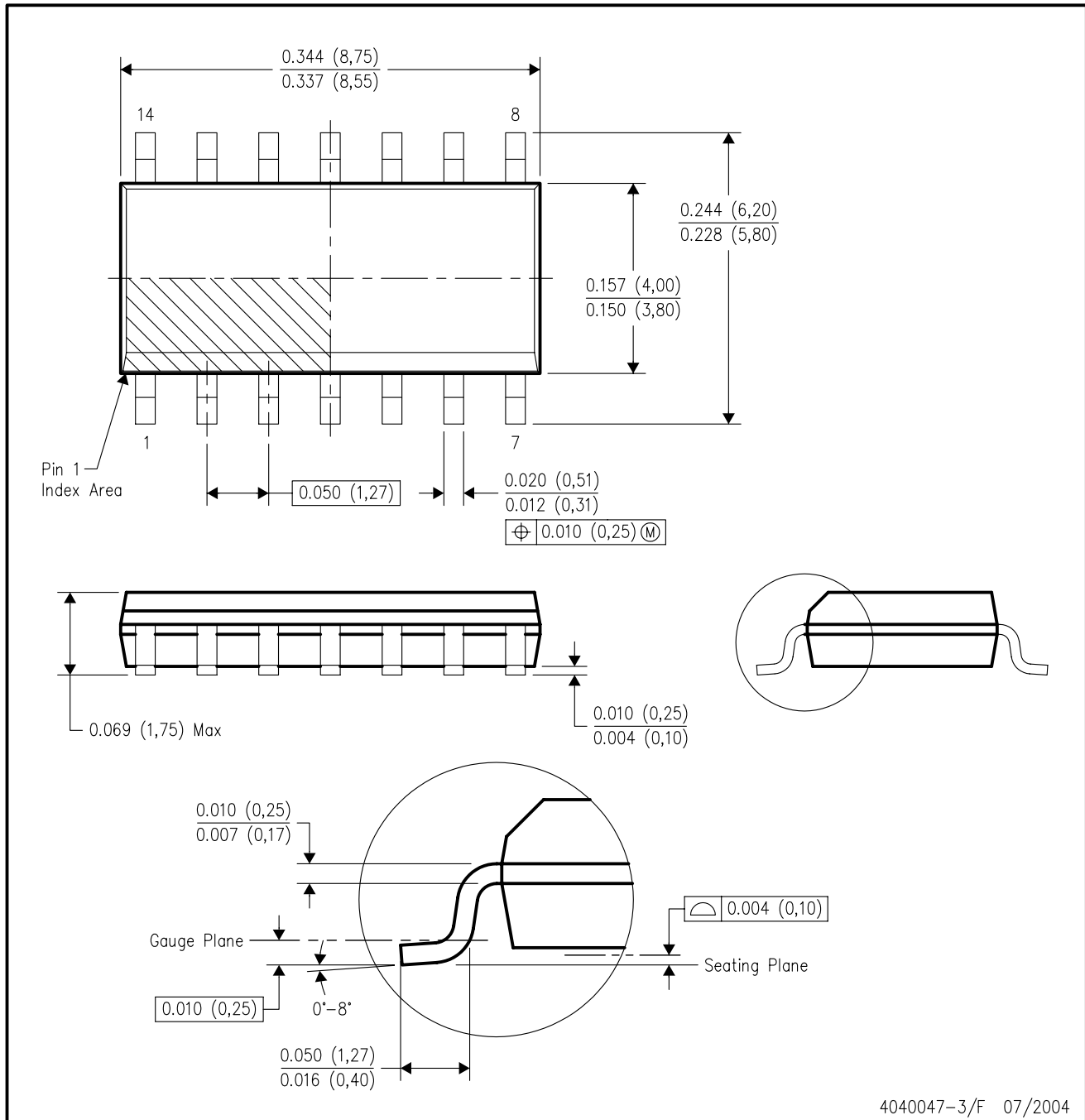
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G14)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-012 variation AB.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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