



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package			
				TO-39	TO-92	TO-220	DICE†
200V	6Ω	1.0A	1.6V	TN0620N2	TN0620N3	TN0620N5	TN0620ND
240V	6Ω	1.0A	1.6V	TN0624N2	TN0624N3	TN0624N5	TN0624ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Low threshold — 1.6V max.
- ☐ High input impedance
- ☐ Low input capacitance — 110 pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

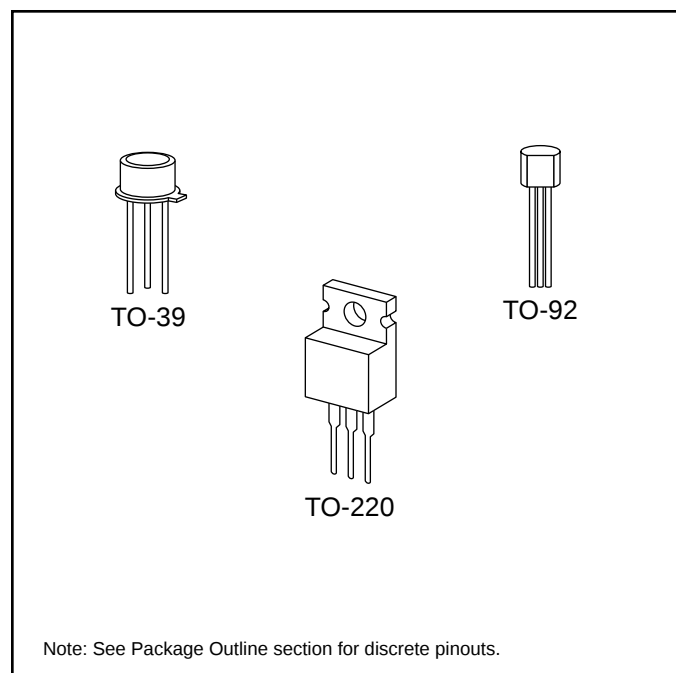
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{jc} $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
TO-39	0.7A	2.5A	6W	20.8	125	0.7A	2.5A
TO-92	0.4A	2.0A	1W	125	170	0.4A	2.0A
TO-220	1.5A	2.5A	45W	2.7	70	1.5A	2.5A

* I_D (continuous) is limited by max rated T_J .

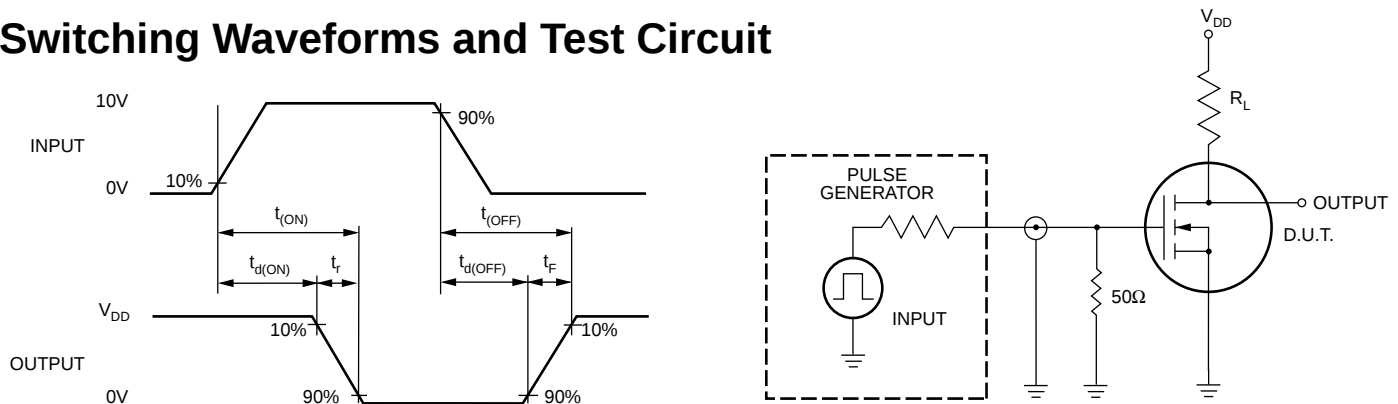
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0624	240			V	$V_{GS} = 0, I_D = 2.0\text{mA}$
		TN0620	200				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	$V_{GS} = V_{DS}, I_D = 1.0\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-5.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1.0\text{mA}$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
					1.0	mA	$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		0.5			A	$V_{GS} = 5\text{V}, V_{DS} = 25\text{V}$
			1.0				$V_{GS} = 10\text{V}, V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			6	8	Ω	$V_{GS} = 5\text{V}, I_D = 0.25\text{A}$
				4	6		$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.4	%/ $^\circ\text{C}$	$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$
G_{FS}	Forward Transconductance		300	400		m Ω	$V_{DS} = 25\text{V}, I_D = 0.5\text{A}$
C_{ISS}	Input Capacitance			110	150	pF	$V_{GS} = 0, V_{DS} = 25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance			40	85		
C_{RSS}	Reverse Transfer Capacitance			10	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = 25\text{V}$ $I_D = 1.0\text{A}$ $R_{GEN} = 25\Omega$
t_r	Rise Time				8.0		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	$V_{GS} = 0, I_{SD} = 1.0\text{A}$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0, I_{SD} = 1.0\text{A}$

Notes:

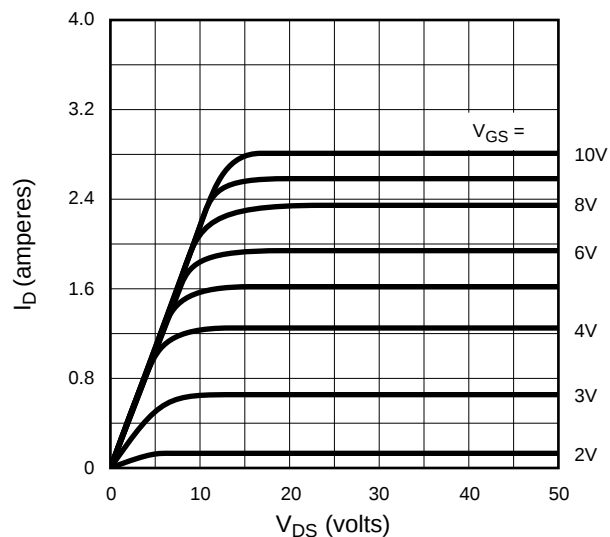
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

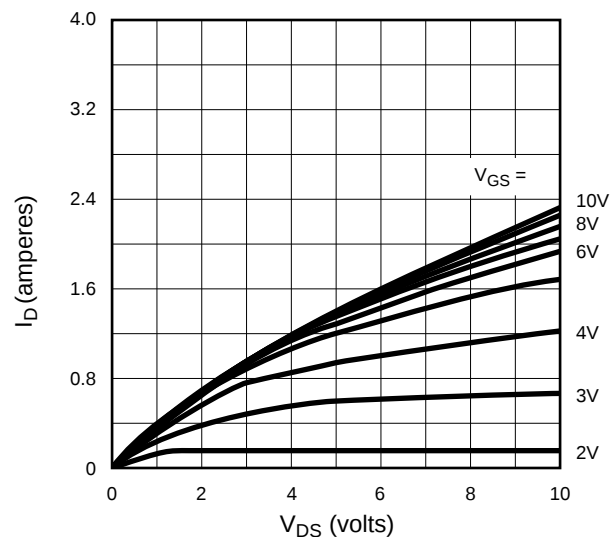


Typical Performance Curves

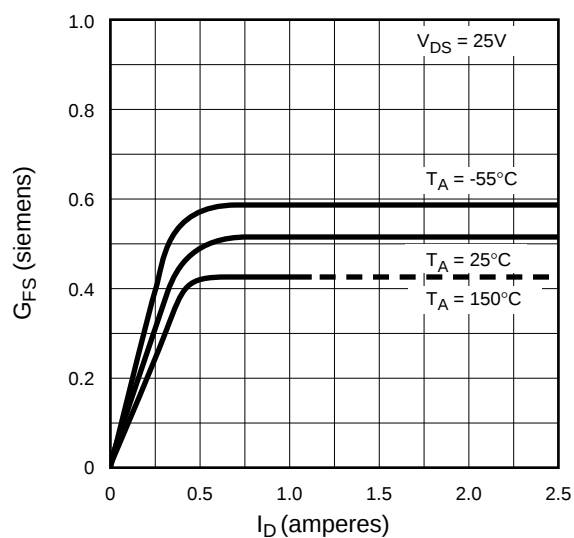
Output Characteristics



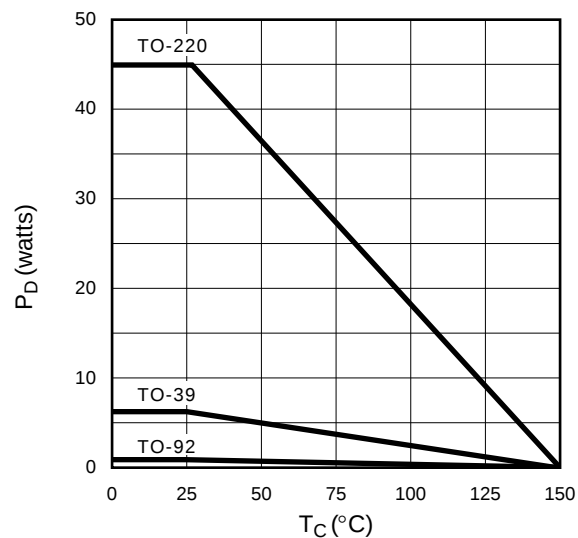
Saturation Characteristics



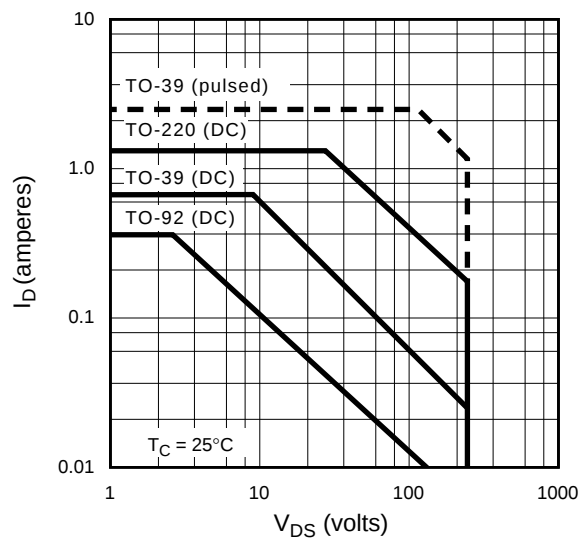
Transconductance vs. Drain Current



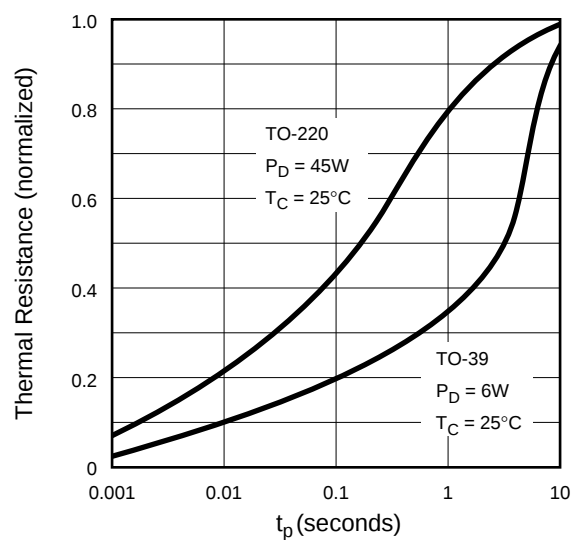
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

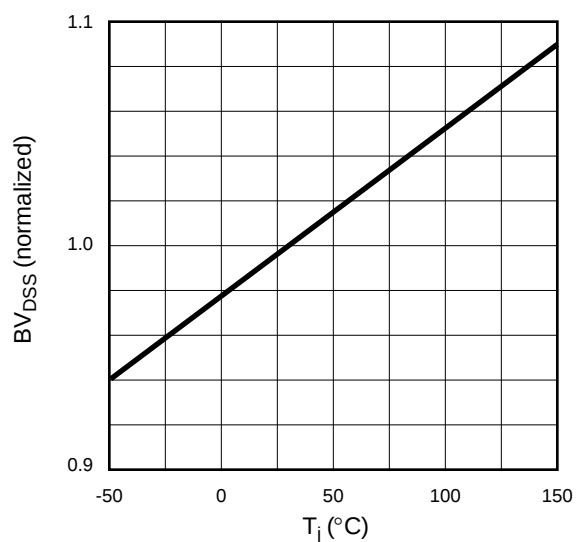


Thermal Response Characteristics

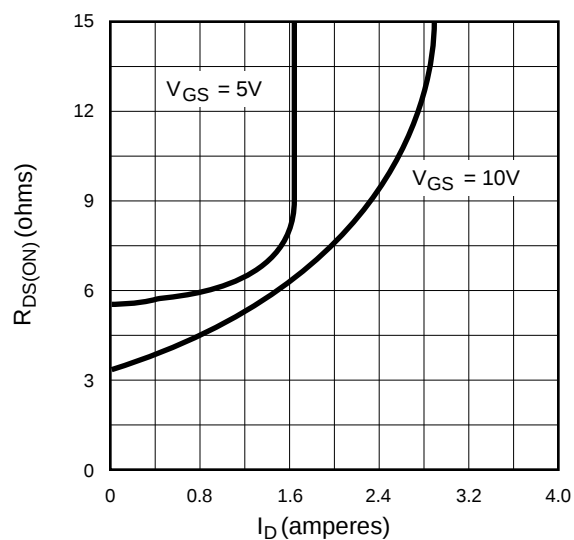


Typical Performance Curves

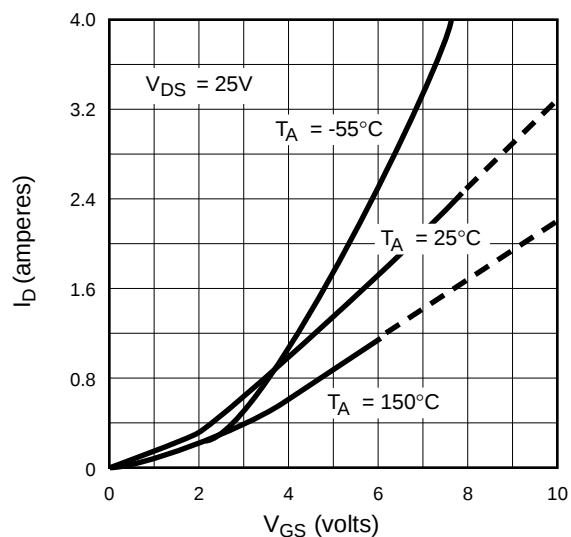
BV_{DSS} Variation with Temperature



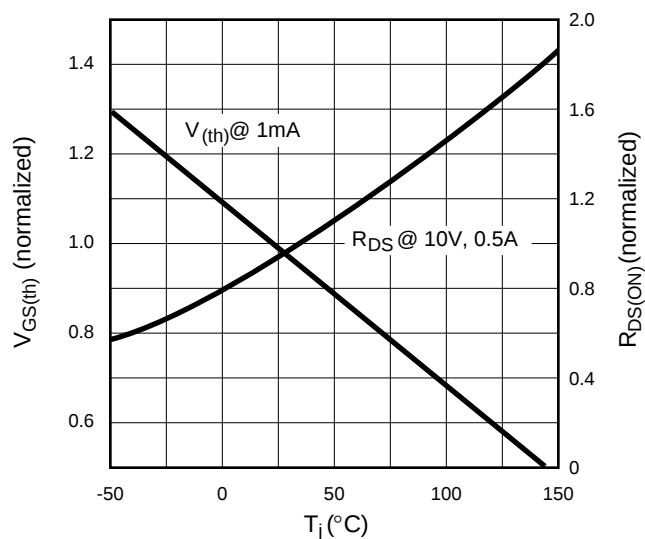
On-Resistance vs. Drain Current



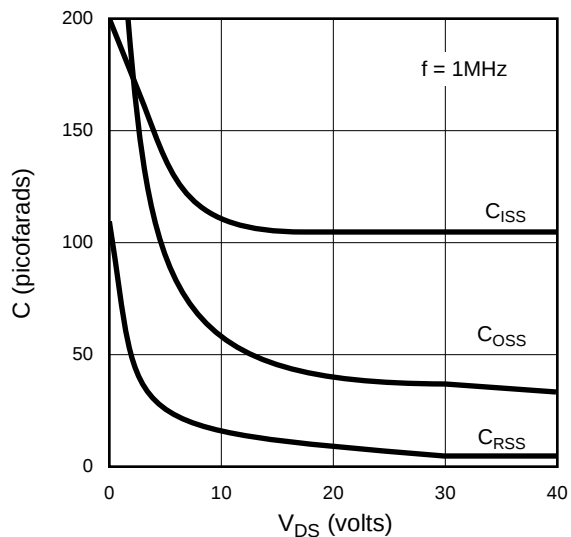
Transfer Characteristics



V_(th) and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

