21152 PCI-to-PCI Bridge

Specification Update

April 2001

Notice: The 21152 may contain design defects or errors known as errata. Characterized errata that may cause the 21152's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278272-004

Contents

Revision History

Date	Version	Description
4/30/01	004	Changed TG21152 naming convention to S21152 naming convention within this document.
		Changed 21152AB Device ID Register Value to 0024 hex within this document.
		Changed S21152BB Device ID Register Value to B152 hex within this document.
		Changed Steppings column label to Markings column label in Table "Errata, Table "Specification Changes, and Table "Specification Clarifications" on page 9.
4/06/01	003	Errata 3 changes the minimum and maximum cycles for s_rst_l deassertion after p_rst_l deassertion.
		Updated steppings and markings versions to AB and BB.
3/17/00	002	New stepping of this device offered.
02/24/99	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents. This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
21152 PCI-to-PCI Bridge Preliminary Data Sheet	278060-001

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 21152 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Markings		Page	Status	ERRATA
	AB	BB			
1	X		11	Fix	Reserved bit in Power Management Capabilities Register has incorrect value
2	X		11	Fix	Hold time violations of primary PCI bus control signals
3	X	X	11	No Fix	The minimum and maximum cycles for s_rst_l deassertion after p_rst_l deassertion have changed.

Specification Changes

No.	Markings		Page	Status	SPECIFICATION CHANGES
	AB	BB			
1			12	Eval	None for this revision of this specification update.

Specification Clarifications

No.	Markings		Page	Status	SPECIFICATION CLARIFICATIONS
	AB	BB			
1			13		None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	DOCUMENTATION CHANGES
1	278060-001	14	Section 15, Table 15-6 Reset Timing Specifications Change

Identification Information

Markings

The 21152 is a legacy component that was initially introduced by Digital Semiconductor, a business division of Digital Equipment Corporation. The characteristics are described in the following table.

21152 Marking

Package Marking	Legacy Marking	VENDOR ID Register Value[a]	DEVICE ID Register Value[b]	REV ID Register Value[c]	Package Type	Speed (MHz)	Stepping
21152AB DC1051A	Yes (Digital Semiconductor)	1101 hex	0024 hex	03 hex	160-PQFP	33	A
S21152BB	No	8086 hex	B152 hex	01 hex	160-PQFP	33	A

a. Identify VENDOR ID by reading VENDOR ID Register at 00 hex in PCI configuration space
b. Identify DEVICE ID by reading DEVICE ID Register at 02 hex in PCI configuration space
c. Identify REV ID by reading REV ID register at 08 hex in PCI configuration space

Errata

1. Reserved bit in Power Management Capabilities Register has incorrect value

Problem: In the 21152's Power Management Capabilities Register (Offset DEh), reserved bits 24:22 are read-only bits that should read 000b. However, bit 24 is incorrectly set in the hardware and the three bits read 100b. In the *PCI Bus Power Management Interface Specification, Revision 1.1*, these three bits correspond to Aux_current. The 21152 does not support PME# generation and therefore the incorrect setting of this bit will not have an impact on the power management operation of the bridge.

Implication: It has no influence on the operation of the part and the 21152 will operate as specified in a power management state.

Workaround: There are no workarounds for this errata.

Status: Fix. This errata exists in 21152AB devices and has been fixed in S21152BB devices.

2. Hold time violations of primary PCI bus control signals

Problem: Hold time violations on primary bus PCI control signals: p_frame_l, p_irdy_l, p_devsel_l, p_stop_l, p_trdy_l, p_lock_l. The PCI Specification, Revision 2.1, specifies a hold time of 0ns in Section 4.2.3.2. The 21152 requires a minimum hold time of 1ns.

Implication: In general, no impact on performance of the 21152. Most PCI devices do not require 0ns hold times.

Workaround: There are no workarounds for this errata.

Status: Fix. This errata exists in 21152AB devices and has been fixed in S21152BB devices.

3. The minimum and maximum cycles for s_rst_l deassertion after p_rst_l deassertion have changed.

Problem: The minimum and maximum cycle values for s_rst_l deassertion after p_rst_l deassertion have changed to less than 3 cycles maximum. No fix is planned.

Implication: No impact on the 21152.

Workaround: There are no workarounds for this errata.

Status: No Fix. This errata exists in 21152AB and S21152BB devices.

Specification Changes

1. None for this revision of this specification update.

Specification Clarifications

1. None for this revision of this specification update.

Documentation Changes

1. Section 15, Table 15-6 Reset Timing Specifications Change

Issue: The minimum and maximum cycles for s_rst_l deassertion after p_rst_l deassertion have changed. Table 15-6 now appears as follows:

Table 15-6. Reset Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{rst}	**p_rst_l** active time after power stable	1	—	µs
$T_{rst-clk}$	**p_rst_l** active time after **p_clk** stable	100	—	µs
$T_{rst-off}$	**p_rst_l** active-to-output float delay	—	40	ns
T_{srst}	**s_rst_l** active after **p_rst_l** assertion	—	40	ns
$T_{srst-on}$	**s_rst_l** active time after **s_clk** stable	100	—	µs
T_{dsrst}	**s_rst_l** deassertion after **p_rst_l** deassertion	—	3	Cycles
	p_rst_l slew rate[a]	50	—	mV/ns

a. Applies to rising (deasserting) edge only.

Affected Docs: 21152 PCI-to-PCI Bridge Preliminary Data Sheet.