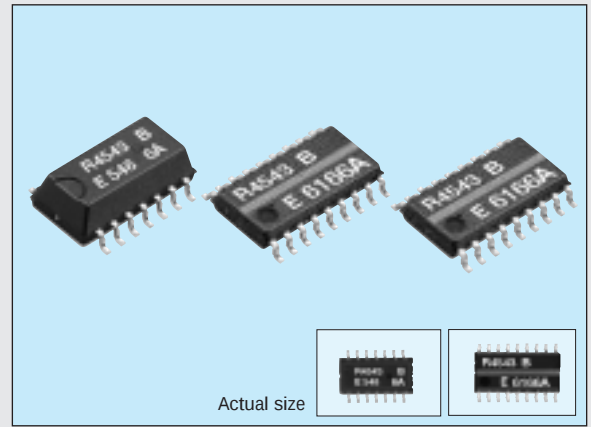


SERIAL-INTERFACE REAL TIME CLOCK MODULE

RTC-4543SA/SB

- Built-in crystal unit allows adjustment-free efficient operation.
- Automatic leap year correction.
- Output selectable between 32.768 KHz/1 Hz.
- Operating voltage range: 2.5V to 5.5V.
- Supply voltage detection voltage: $1.7 \pm 0.3V$.
- Low current consumption: $1.0 \mu A/2.0V$ (Max.)



■ Specifications (characteristics)

■ Absolute Max. rating

Item	Symbol	Condition	Min.	Max.	Unit
Power source voltage	V _{DD}	V _{DD} -GND	-0.3	7.0	V
Input voltage	V _{IN}	—		V _{DD} +0.3	
Output voltage	V _{OUT}				
Storage temperature	T _{STG}		-55	+125	°C

■ Operating range

Item	Symbol	Condition	Min.	Max.	Unit
Operating voltage	V_{DD}	—	2.5	5.5	V
Date holding voltage	V_{CLK}		1.4		
Operating temperature	T_{OPR}		-40	+85	

■ Frequency characteristics

Item	Symbol	Condition	Range	Unit
Frequency tolerance	$\Delta f/f_0$	$T_a=25^\circ C, V_{DD}=5V$	5 ± 23	ppm
Frequency temperature characteristics	T_{OP}	-10 to $+70^\circ C$	$+10/-120$	
Frequency voltage characteristics	f_v	$T_a=25^\circ C, V_{DD}=2.0$ to $5.5V$	± 2	ppm/V
Oscillation start time	t_{OSC}	$T_a=25^\circ C, V_{DD}=2.5V$	3	s
Aging	f_a	First year $T_a=25^\circ C, V_{DD}=5V$	± 5	ppm/year

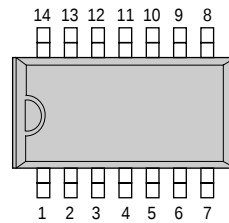
■ DC characteristics

(V_{DD}=5V±0.5V, T_a=-40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	WR, DATA, CE, CLK, F _{OE} , F _{SEL} pins	$0.8V_{DD}$	—	—	V
"L" input voltage	V_{IL}		—		$0.2V_{DD}$	
Input off-leak current	I_{OFF}	WR, CE, CLK, F _{OE} , F _{SEL} pins	—	—	0.5	μA
"H" output voltage	V_{OH1}	$V_{DD}=5.0V$	$I_{OH}=-1.0$ mA	—	—	V
	V_{OH2}	$V_{DD}=3.0V$	DATA, F _{OUT} pins		—	
"L" output voltage	V_{OL1}	$V_{DD}=5.0V$	$I_{OH}=1.0$ mA	—	0.5	V
	V_{OL2}	$V_{DD}=3.0V$	DATA, F _{OUT} pins		0.8	
Output leak current	I_{OZH}	$V_{OUT}=5.5V$	DATA, F _{OUT} pins	-1.0	1.0	μA
	I_{OZL}	$V_{OUT}=0V$				
Supply detection voltage	V_{DT}	—	1.4	1.7	2.0	V
Output load conditions	CL	F _{OUT} pin	30 pF(max.)	—	—	V
	N					
Current consumption	1	I_{DD1}	$V_{DD}=5.0V$	—	1.5	μA
	2	I_{DD2}	$V_{DD}=3.0V$		1.0	
	3	I_{DD3}	$V_{DD}=2.0V$		0.5	
	4	I_{DD4}	$V_{DD}=5.0V$		4.0	
	5	I_{DD5}	$V_{DD}=3.0V$		2.5	
	6	I_{DD6}	$V_{DD}=2.0V$		1.5	

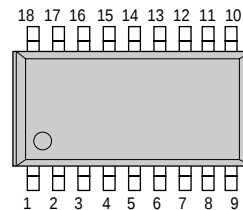
■ Terminal connection

● RTC-4543SA



No.	4543SA	4543SB
1	GND	N.C
2	N.C	N.C
3	CE	N.C
4	FSEL	N.C
5	WR	F _{OE}
6	F _{OE}	WR
7	N.C	FSEL
8	N.C	CE
9	V _{DD}	GND
10	CLK	F _{OUT}
11	DATA	DATA
12	N.C	CLK
13	N.C	N.C
14	F _{OUT}	V _{DD}
15	—	N.C
16	—	N.C
17	—	N.C
18	—	N.C

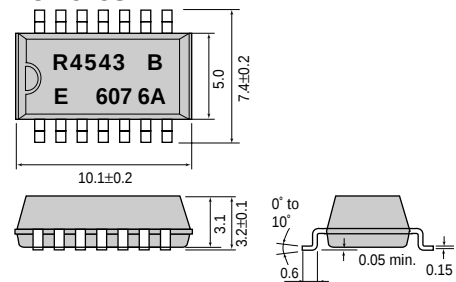
● RTC-4543SB



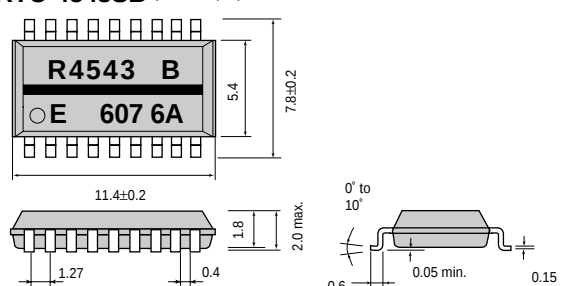
■ External dimensions

(Unit: mm)

● RTC-4543SA (SOP 14-pin)



● RTC-4543SB (SOP 18-pin)



Register table

	MSB							
Seconds (0 to 59)	FDT	s 40	s 20	s 10	s 8	s 4	s 2	s 1
Minutes (0 to 59)	*	mi 40	mi 20	mi 10	mi 8	mi 4	mi 2	mi 1
Hour (0 to 23)	*	*	h 20	h 10	h 8	h 4	h 2	h 1
Day of the week (1 to 7)					*	w 4	w 2	w 1
Day (1 to 31)	*	*	d 20	d 10	d 8	d 4	d 2	d 1
Month (1 to 12)	TM	*	*	mo 10	mo 8	mo 4	mo 2	mo 1
year (0 to 99)	y 80	y 40	y 20	y 10	y 8	y 4	y 2	y 1

FDT bit: Supply voltage detection bit.

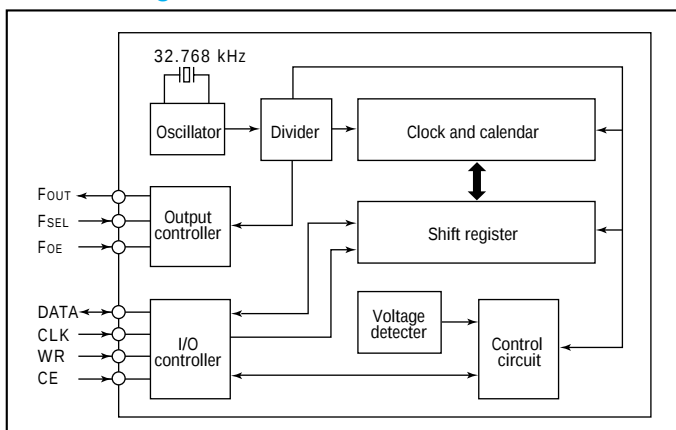
TM bit: Test bit always set this bit to "0".

Switching characteristics

(Ta=-40 to +85°C, CL=30 pF)

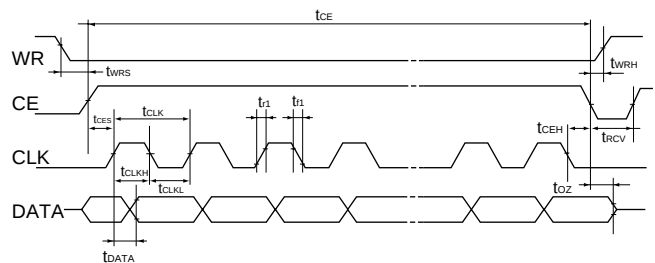
Item		Symbol	V _{DD} = 5V± 10%		V _{DD} = 3V± 10%		Unit
			Min.	Max.	Min.	Max.	
CLK clock cycle		t _{CLK}	0.75	7800	1.5	7800	μs
CLK high pulse width		t _{CLKH}	0.375	3900	0.75	3900	
CLK low pulse width		t _{CLKL}					
CE setup time		t _{CES}					
CE hold time		t _{CEH}	—	—	—	—	
CE enable time		t _{CE}	—	0.9	—	0.9	s
Write data setup time		t _{SD}	0.1	—	0.2	—	μs
Write data hold time		t _{HD}			0.1		
WR setup time		t _{WRS}	100		100	100	100
WR hold time		t _{WRH}					
DATA output delay time		t _{DATA}	—	0.2	—	0.4	μs
DATA output floating time		t _{DZ}		0.1		0.2	
Clock input rise time		t _{r1}		50	100	100	ns
Clock input fall time		t _{f1}		100		200	
F _{OUT} rise time	C _L = 30pF	t _{r2}					
F _{OUT} fall time		t _{f2}					
Disable time		t _{X2}					
Enable time		t _{ZX}					
F _{OUT} duty ratio		Duty	40	60	40	60	%
Wait time		t _{rcv}	0.95	—	1.9	—	μs

Block diagram

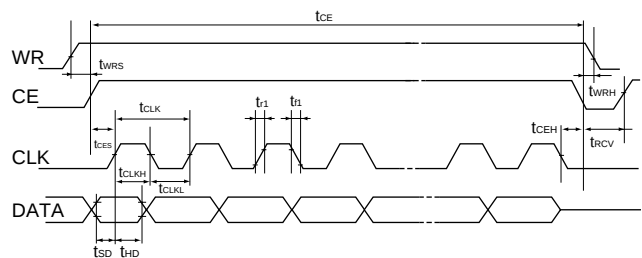


Timing chart

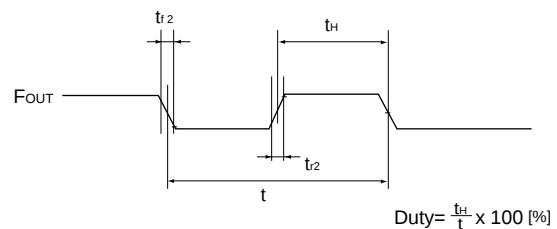
• Data read



• Data write



• F_{OUT}



• Disabled and Enabled

