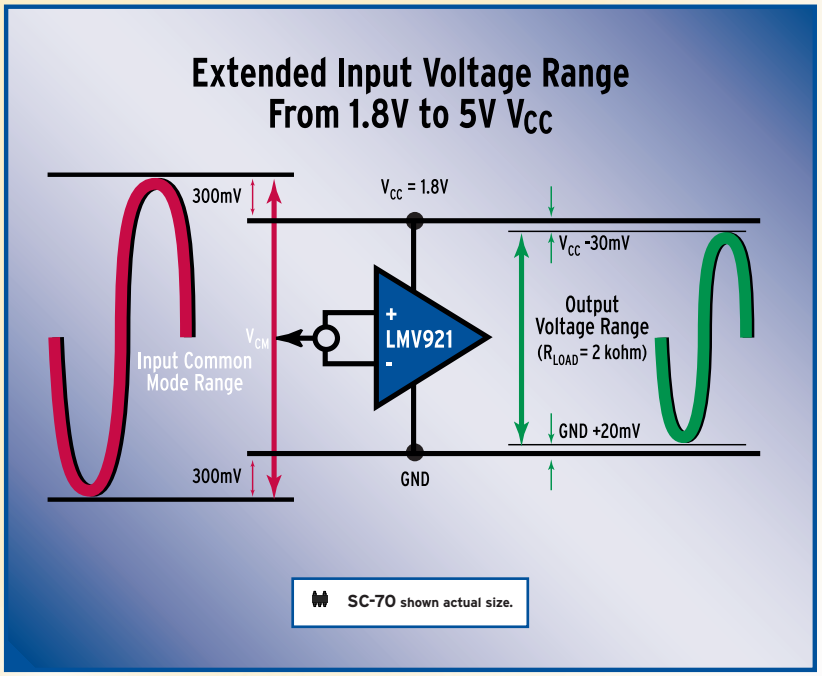
LMV921

Qualification Package

World's Smallest 1.8V RR I/O Op Amp

- CMVR 300mV beyond rails
- RR output swing within 30mV @ 2K load
- SC-70 and SOT packaging
- LMV321 pin-compatible



National Semiconductor

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LMV921
QUALIFICATION PACKAGE

Summer 1999

Table of Contents

1.0 INTRODUCTION

1.1 General Product Description

This qualification booklet covers a general purpose Op Amp. It is available in 2 different packages.

Single Op Amp	LMV921IM5/IM5X (5 lead SOT-23 package) LMV921IM7/IM7X (5 lead SC-70 package)

1.2 Technical Product Description

The LMV921 is manufactured using National's advanced Submicron Silicon Gate BiCMOS process. Internal name for this process is CS80CBi, which uses 6-inch wafers.

1.3 Reliability/Qualification Overview

Copies of all reliability test reports listed below can be found under Reliability Reports section 5.0 later in this qualification booklet.

1.4 Technical Assistance

Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

Europe
Fax: +49 (0) 1 80 5 30 85 86
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Deutsch Tel: +49 (0) 1 80 5 30 85 85
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Japan
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

Asia Pacific
Fax: 65-2504466
Email: sea.support@nsc.com
Tel: 65-2544466
(IDD telephone charge to be paid by caller)

See us on the Worldwide Web @ http://www.national.com

2.0 DEVICE INFORMATION

2.1 Datasheet

National Semiconductor

April 1999

LMV921
1.8V, 1MHz, Low Power Operational Amplifier with Rail-To-Rail Input and Output in SC70-5 package

General Description

The LMV921 is guaranteed to operate from +1.8V to +5.0V supply voltages and has rail-to-rail input and output. This rail-to-rail operation enables the user to make full use of the entire supply voltage range. The input common mode voltage range extends 300mV beyond the supplies and the output can swing rail-to-rail unloaded and within 100mV from the rail with 600Ω load at 1.8V supply. The LMV921 is optimized to work at 1.8V which makes it ideal for portable two-cell battery-powered systems and single cell Li-Ion systems.

The LMV921 exhibits excellent speed-power ratio, achieving 1 MHz gain bandwidth product at 1.8V supply voltage with very low supply current. The LMV921 is capable of driving 600Ω load and up to 1000pF capacitive load with minimal ringing. The LMV921's high DC gain of 100dB makes it suitable for low frequency applications.

The LMV921 is offered in a space saving SC70-5 and SOT23-5 packages. The SC70-5 package is only 2.0X2.1X1.0mm. These small packages are ideal solutions for area constrained PC boards and portable electronics such as cellphones and PDAs.

Features

(Typical 1.8V Supply Values; Unless Otherwise Noted)

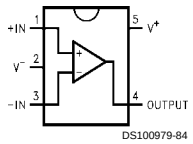
- Guaranteed 1.8V, 2.7V and 5V specifications
- Rail-to-Rail Input & Output Swing
  - — w/600 Ω Load: 100 mV from rail
  - — w/2kΩ Load: 30 mV from rail
- V_{CM}: 300mV beyond rails
- Ultra Tiny, SC70-5 package
- 90dB gain w/600Ω load
- Supply Current: 145µA
- Gain Bandwidth Product: 1MHz
- Maximum V_{OS}: 6mV

Applications

- Cordless/Cellular Phones
- Laptops
- PDAs
- PCMCIA
- Portable/Battery-Powered Electronic Equipment
- Supply Current Monitoring
- Battery Monitoring

Connection Diagram

5-Pin SC70-5/SOT23-5



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Top View

Ordering Information

Package	Temperature Range Industrial −40˚C to +85˚C	Packaging Marking	Transport Media	NSC Drawing
5-Pin SC70-5	LMV921M7	A21	250 Units Tape and Reel	MAA05A
	LMV921M7X	A21	3k Units Tape and Reel	
5-Pin SOT23-5	LMV921M5	A29A	250 Units Tape and Reel	MA05B
	LMV921M5X	A29A	3k Units Tape and Reel	

 DS100979

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	100V
Human Body Model	2000V
Differential Input Voltage	± Supply Voltage
Supply Voltage (V^+–V^-)	5.5V
Output Short Circuit to V^+ (Note 3)	
Output Short Circuit to V^- (Note 3)	
Storage Temperature Range	−65˚C to 150˚C
Junction Temperature (Note 4)	150˚C
Mounting Temp.	
Lead Temp. (Soldering, 10 sec)	260˚C
Infrared (10 sec)	215˚C

Operating Ratings (Note 1)

Supply Voltage	1.5V to 5.0V
Temperature Range	−40˚C ≤ T_J ≤ 85˚C
Thermal Resistance (θ_{JA})	
Ultra Tiny SC70-5 Package 5-Pin Surface Mount	440 ˚C/W
Tiny SOT23-5 Package 5-Pin Surface Mount	265 ˚C/W

1.8V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 1.8V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
V_{OS}	Input Offset Voltage		−1.8	6 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/˚C
I_B	Input Bias Current		12	35 **50**	nA max
I_{OS}	Input Offset Current		2	25 **40**	nA max
I_S	Supply Current		145	185 **205**	µA max
CMMR	Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 0.6V	82	62 **60**	dB min
		−0.2V ≤ V_{CM} ≤ 0V 1.8V ≤ V_{CM} ≤ 2.0V	74	50	
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V, V_{CM} = 0.5V	78	67 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2 **0**	V min
			2.15	2.0 **1.8**	V max
A_V	Large Signal Voltage Gain	R_L = 600Ω to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V	91	77 **73**	dB min
		R_L = 2kΩ to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V	95	80 **75**	dB min
V_O	Output Swing	R_L = 600Ω to 0.9V V_{IN} = ± 100mV	1.7	1.68 **1.66**	V min
			0.075	0.090 **0.105**	V max
		R_L = 2kΩ to 0.9V V_{IN} = ± 100mV	1.77	1.76 **1.75**	V min
			0.025	0.035 **0.040**	V max
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	6	4 **3.3**	mA min
		Sinking, V_O = 1.8V V_{IN} = −100mV	10	7 **5**	mA min

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 1.8V, V^- = 0V, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1$ MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 7)	0.39	V/µs
GBW	Gain-Bandwidth Product		1	MHz
Φ_m	Phase Margin		60	Deg.
G_m	Gain Margin		10	dB
e_n	Input-Referred Voltage Noise	f = 1 kHz, V_{CM} = 0.5V	45	$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.1	$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600kΩ, V_{IN} = 1 V_{PP}	0.089	%

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1$ MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
V_{OS}	Input Offset Voltage		−1.6	6 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/˚C
I_B	Input Bias Current		12	35 **50**	nA max
I_{OS}	Input Offset Current		2	25 **40**	nA max
I_S	Supply Current		147	190 **210**	uA max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.5V	84	62 **60**	dB min
		−0.2V ≤ V_{CM} ≤ 0V 2.7V ≤ V_{CM} < 2.9V	73	50	
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V, V_{CM} = 0.5V	78	67 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2 **0**	V min
			3.050	2.9 **2.7**	V max
A_V	Large Signal Voltage Gain	R_L = 600Ω to 1.35V, V_O = 0.2V to 2.5V	98	80 **75**	dB min
		R_L = 2kΩ to 1.35V, V_O = 0.2V to 2.5V	103	83 **77**	dB min
V_O	Output Swing	R_L = 600Ω to 1.35V V_{IN} = ± 100mV	2.62	2.6 **2.580**	V min
			0.075	0.095 **0.115**	V max
		R_L = 2kΩ to 1.35V V_{IN} = ± 100mV	2.675	2.660 **2.650**	V min
			0.025	0.040 **0.045**	V max

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	27	20 **15**	mA min
		Sinking, V_O = 2.7V V_{IN} = −100mV	28	22 **16**	mA min

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 7)	0.41	V/µs
GBW	Gain-Bandwidth Product		1	MHz
Φ_m	Phase Margin		65	Deg.
G_m	Gain Margin		10	dB
e_n	Input-Referred Voltage Noise	f = 1 kHz, V_{CM} = 0.5V	45	$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.1	$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600kΩ, V_{IN} = 1 V_{PP}	0.077	%

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1 MΩ.**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
V_{OS}	Input Offset Voltage		−1.5	6 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/˚C
I_B	Input Bias Current		12	35 **50**	nA max
I_{OS}	Input Offset Current		2	25 **40**	nA max
I_S	Supply Current		160	210 **230**	uA max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.8V	86	62 **61**	dB min
		−0.2V ≤ V_{CM} ≤ 0V 5.0V ≤ V_{CM} ≤ 5.2V	72	50	
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V V_{CM} = 0.5V	78	67 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2 **0**	V min
			5.350	5.2 **5.0**	V max
A_V	Voltage Gain	R_L = 600Ω to 2.5V V_O = 0.2V to 4.8V	104	86 **82**	dB min
		R_L = 2kΩ to 2.5V V_O = 0.2V to 4.8V	108	89 **85**	dB min

5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
V_O	Output Swing	R_L = 600Ω to 2.5V V_{IN} = ± 100mV	4.895	4.865 **4.840**	V min
			0.1	0.125 **0.150**	V max
		R_L = 2kΩ to 2.5V V_{IN} = ± 100mV	4.965	4.945 **4.935**	V min
			0.035	0.055 **0.065**	V max
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	98	85 **68**	mA min
		Sinking, V_O = 5V V_{IN} = −100mV	75	65 **45**	mA min

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 7)	0.45	V/µs
GBW	Gain-Bandwidth Product		1	MHz
Φ_m	Phase Margin		70	Deg.
G_m	Gain Margin		15	dB
e_n	Input-Referred Voltage Noise	f = 1 kHz, V_{CM} = 1V	45	$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.1	$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600Ω, V_O = 1 V_{PP}	0.069	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. Machine model, 200Ω in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of 45 mA over long term may adversely affect reliability.

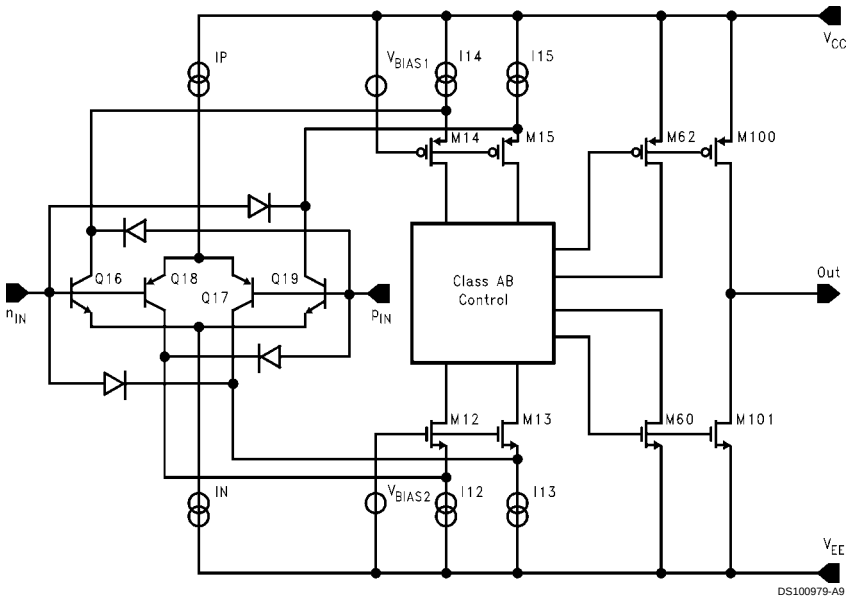
Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 5V. Connected as voltage follower with 5V step input. Number specified is the slower of the positive and negative slew rates.

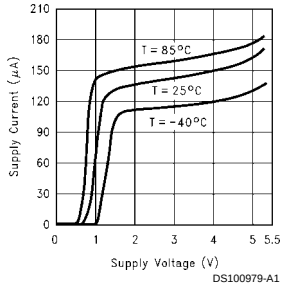
Simplified Schematic



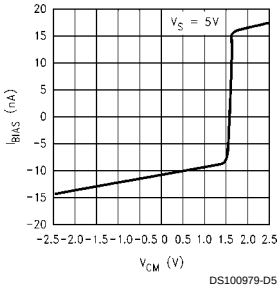
Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C.

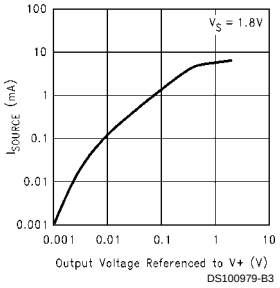
Supply Current vs Supply Voltage



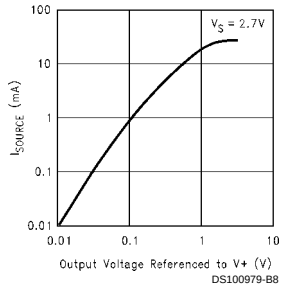
Input Bias Current vs V_{CM}



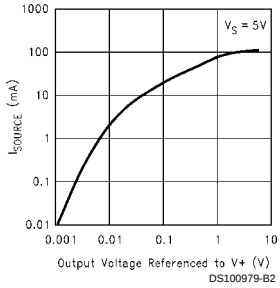
Sourcing Current vs Output Voltage



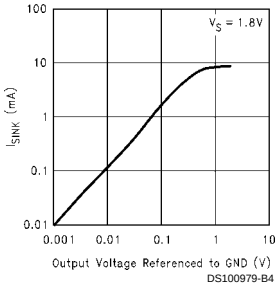
Sourcing Current vs Output Voltage



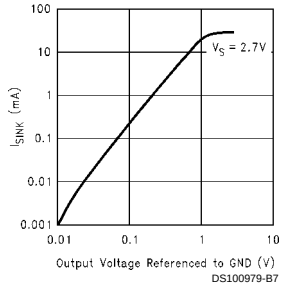
Sourcing Current vs Output Voltage



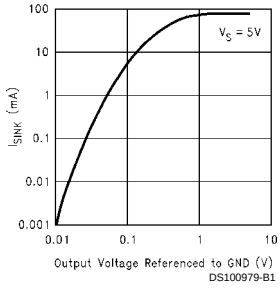
Sinking Current vs Output Voltage



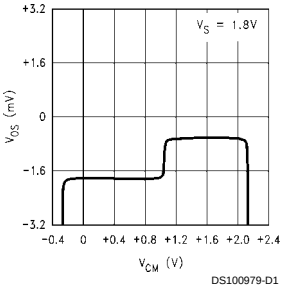
Sinking Current vs Output Voltage



Sinking Current vs Output Voltage



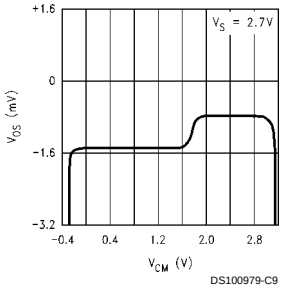
Offset Voltage vs Common Mode Voltage



Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Offset Voltage vs Common Mode Voltage



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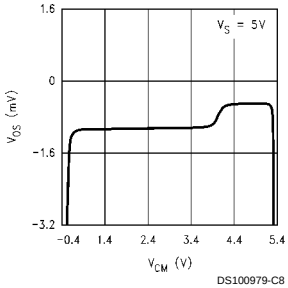
Offset Voltage vs Common Mode Voltage



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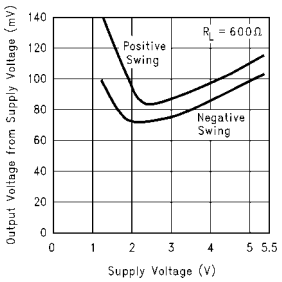
Output Voltage Swing vs Supply Voltage



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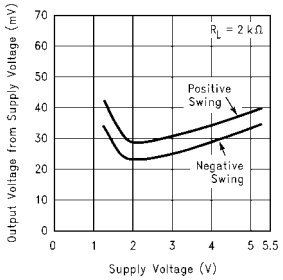
Output Voltage Swing vs Supply Voltage



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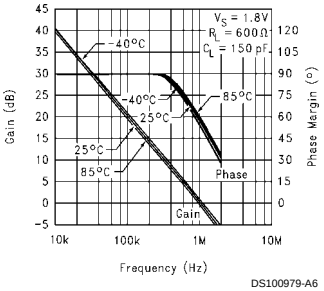
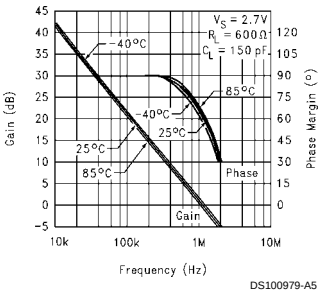
Gain and Phase Margin vs Frequency



DS100979-A6

Gain and Phase Margin vs Frequency



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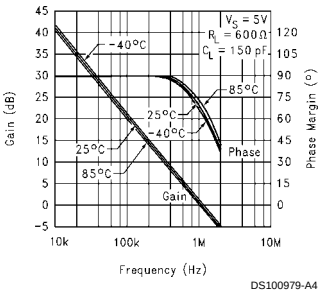
Gain and Phase Margin vs Frequency



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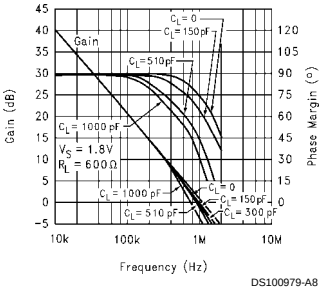
Gain and Phase Margin vs Frequency



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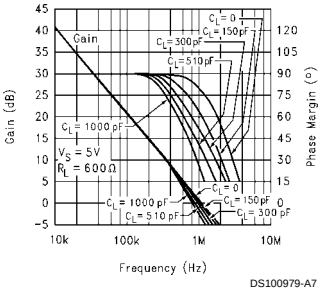
Gain and Phase Margin vs Frequency

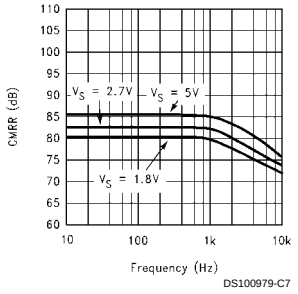


DS100979-A7

Typical Performance Characteristics

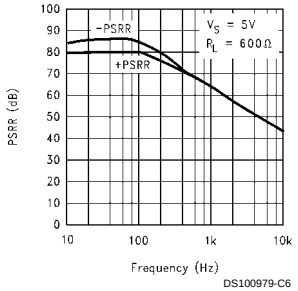
Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

CMRR vs Frequency



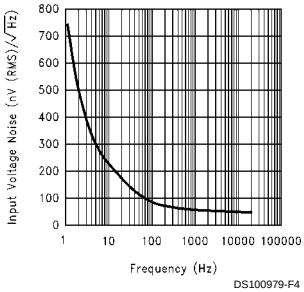
DS100979-C7

PSRR vs Frequency



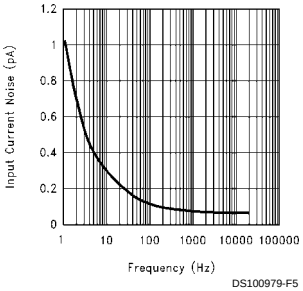
DS100979-C6

Input Voltage Noise vs Frequency



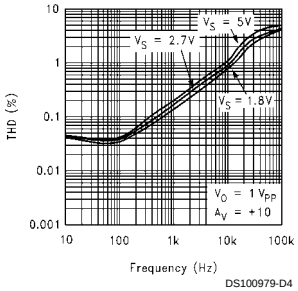
DS100979-F4

Input Current Noise vs Frequency



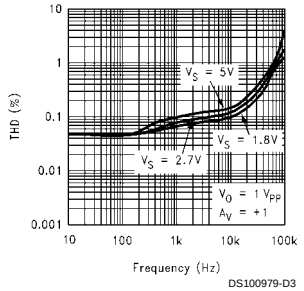
DS100979-F5

THD vs Frequency



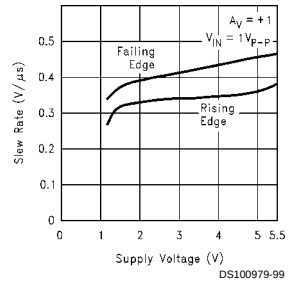
DS100979-D4

THD vs Frequency



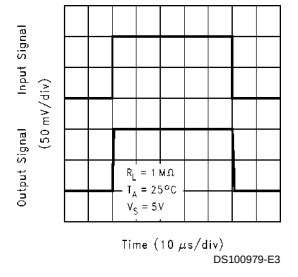
DS100979-D3

Slew Rate vs Supply Voltage



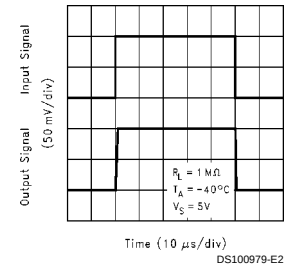
DS100979-99

Small Signal Non-Inverting Response



DS100979-E3

Small Signal Non-Inverting Response

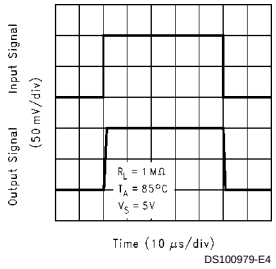


DS100979-E2

Typical Performance Characteristics

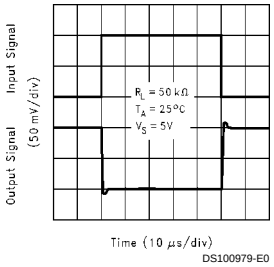
Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Small Signal Non-Inverting Response



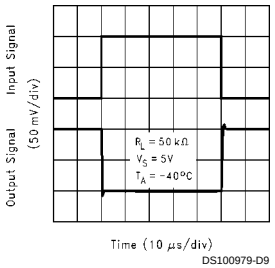
DS100979-E4

Small Signal Inverting Response



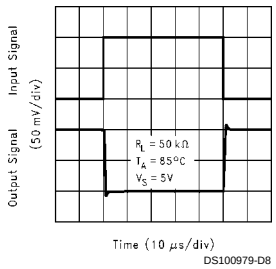
DS100979-E0

Small Signal Inverting Response



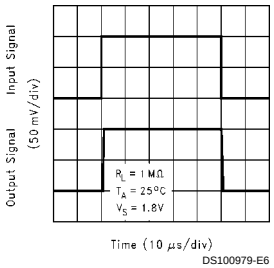
DS100979-D9

Small Signal Inverting Response



DS100979-D8

Small Signal Non-Inverting Response



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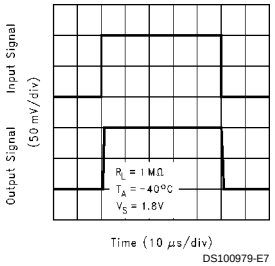
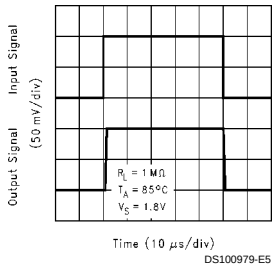
Small Signal Non-Inverting Response



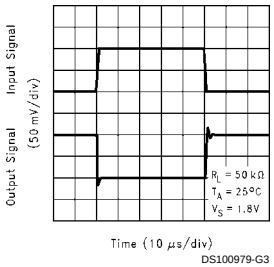
DS100979-E7

Small Signal Non-Inverting Response



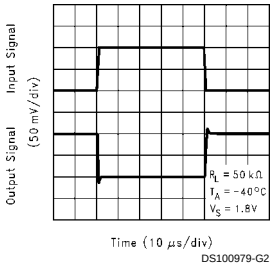
DS100979-E5

Small Signal Inverting Response



DS100979-G3

Small Signal Inverting Response

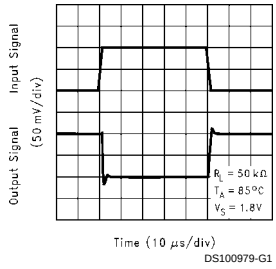


DS100979-G2

Typical Performance Characteristics

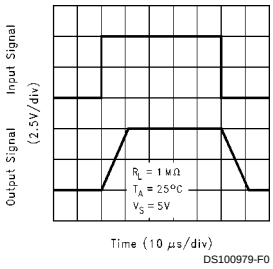
Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Small Signal Inverting Response



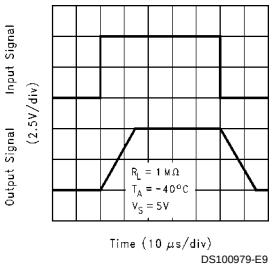
DS100979-G1

***Large Signal Non-Inverting Response**



DS100979-F0

***Large Signal Non-Inverting Response**



DS100979-E9

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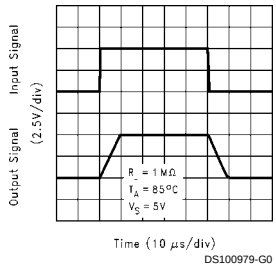

DS100979-G0

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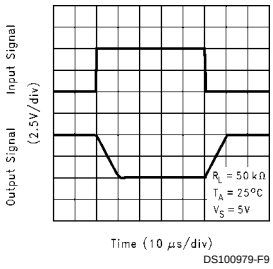

DS100979-F9

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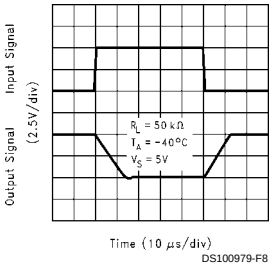
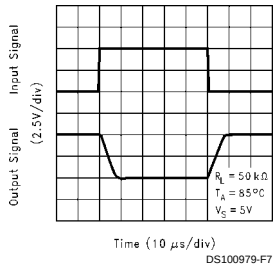


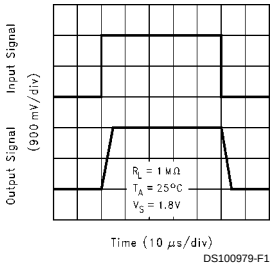
DS100979-F8

***Large Signal Inverting Response**



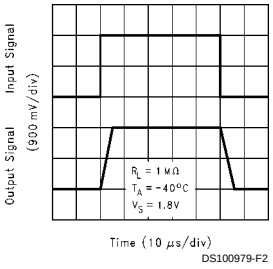
DS100979-F7

***Large Signal Non-Inverting Response**



DS100979-F1

***Large Signal Non-Inverting Response**



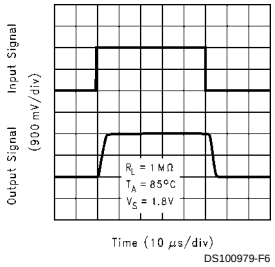
DS100979-F2

*For large signal pulse response in the unity gain follower configuration, the input is 5mV below the positive rail and 5mV above the negative rail at 25˚C and 85˚C. At −40˚C, input is 10mV below the positive rail and 10mV above the negative rail.

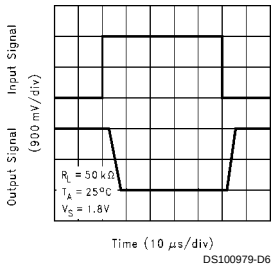
Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

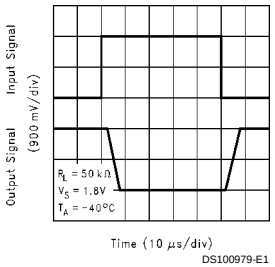
***Large Signal Inverting Response**



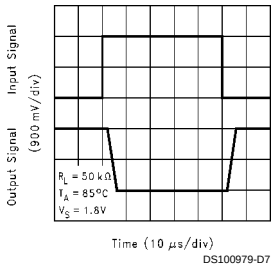
***Large Signal Inverting Reponse**



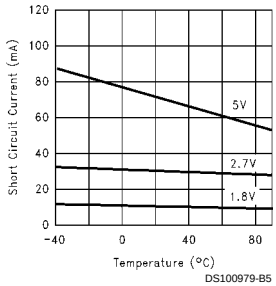
***Large Signal Inverting Reponse**



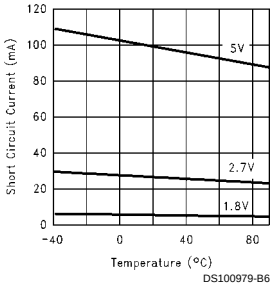
***Large Signal Inverting Reponse**



Short Circuit Current vs Temperature (sinking)



Short Circuit Current vs Temperature (sourcing)



*For large signal pulse response in the unity gain follower configuration, the input is 5mV below the positive rail and 5mV above the negative rail at 25˚C and 85˚C. At −40˚C, input is 10mV below the positive rail and 10mV above the negative rail.

Application Note

1.0 Unity Gain Pulse Response Considerations

The unity-gain follower is the most sensitive configuration to capacitive loading. The LMV921 can directly drive 1nF in a unity-gain with minimal ringing. Direct capacitive loading reduces the phase margin of the amplifier. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. The pulse response can be improved by adding a pull up resistor as shown in *Figure 1*

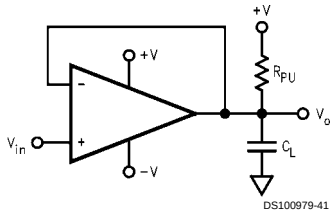


FIGURE 1. Using a Pull-Up Resistor at the Output for Stabilizing Capacitive Loads

Higher capacitances can be driven by decreasing the value of the pull-up resistor, but its value shouldn't be reduced beyond the sinking capability of the part. An alternate approach is to use an isolation resistor as illustrated in *Figure 2.*

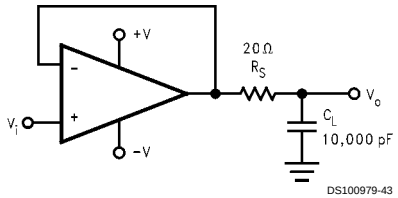


FIGURE 2. Using an Isolation Resistor to Drive Heavy Capacitive Loads

2.0 Input Bias Current Consideration

The LMV921 has a bipolar input stage. The typical input bias current (I_B) is 12nA. The input bias current can develop a significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 50nA (max room) and R_F is 100kΩ, then an offset voltage of 5mV will develop ($V_{OS} = I_B X R_F$). Using a compensation resistor (R_C), as shown in *Figure 3*, cancels this affect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner.

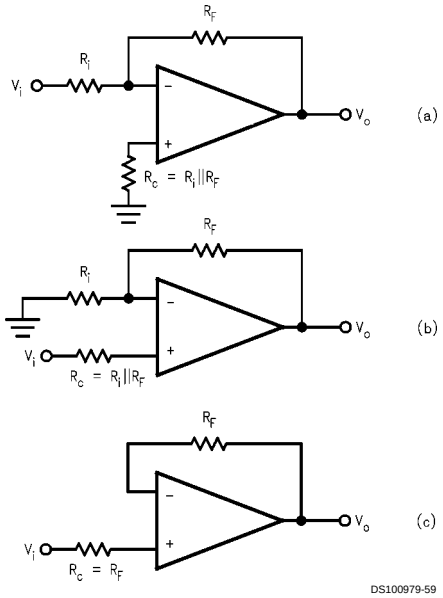


FIGURE 3. Canceling the Voltage Offset Effect of Input Bias Current

3.0 Operating Supply Voltage

The LMV921 is guaranteed to operate from 1.8V to 5.0V. The LMV921 will begin to function at power voltages as low as 1.2V at room temperature when unloaded. Start up voltage increases to 1.5V when the amplifier is fully loaded (600Ω to mid-supply). Below 1.2V the output voltage is not guaranteed to follow the input. *Figure 4* below shows the output voltage vs. supply voltage with the LMV921 configured as a voltage follower at room temperature.

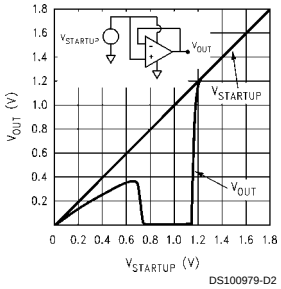


FIGURE 4.

4.0 Input and Output Stage

The rail-to-rail input stage of LMV921 provides more flexibility for the designer. The LMV921 uses a complimentary PNP and NPN input stage in which the PNP stage senses common mode voltage near V^- and the NPN stage senses common mode voltage near V^+. The transition from the PNP stage to NPN stage occurs 1V below V^+. Since both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common mode voltage and has a crossover point at 1V below V^+ as shown in the V_{OS} vs. V_{CM} curves.

Application Note (Continued)

This V_{OS} crossover point can create problems for both DC and AC coupled signals if proper care is not taken. For large input signals that include the V_{OS} crossover point in their dynamic range, this will cause distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity gain buffer configuration and with V_S = 5V, a 5V peak-to-peak signal will contain input-crossover distortion while a 3V peak-to-peak signal centered at 1.5V will not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of −1 circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common mode DC voltage can be set at a level away from the V_{OS} cross-over point.

For small signals, this transition in V_{OS} shows up as a V_{CM} dependent spurious signal in series with the input signal and can effectively degrade small signal parameters such as gain and common mode rejection ratio. To resolve this problem, the small signal should be placed such that it avoids the V_{OS} crossover point.

In addition to the rail-to-rail performance, the output stage can provide enough output current to drive 600Ω loads. Because of the high current capability, care should be taken not to exceed the 150˚C maximum junction temperature specification.

5.0 Power-Supply Considerations

The LMV921 is ideally suited for use with most battery-powered systems. The LMV921 operates from a single +1.8V to +5.0V supply and consumes about 145µA of supply current. A high powersupply rejection ratio of 78dB allows the amplifier to be powered directly off a decaying battery voltage extending battery life.

Table 1 lists a variety of typical battery types. Batteries have different voltage ratings; operating voltage is the battery voltage under nominal load. End-of-Life voltage is defined as the voltage at which 100% of the usable power of the battery is consumed. *Table 1* also shows the typical operating time of the LMV921.

6.0 Distortion

The two main contributors of distortion in LMV921 are:

1. Output crossover distortion occurs as the output transitions from sourcing current to sinking current.

2. Input crossover distortion occurs as the input switches from NPN to PNP transistor at the input stage.

To decrease crossover distortion:

1. Increase the load resistance. This lowers the output crossover distortion but has no effect on the input crossover distortion.

2. Operate from a single supply with the output always sourcing current.

3. Limit the input voltage swing for large signals between ground and one volt below the positive supply.

4. Operate in inverting configuration to eliminate common mode induced distortion.

5. Avoid small input signal around the input crossover region. The discontinuity in the offset voltage will effect the gain, CMRR and PSRR.

TABLE 1. LMV921 Characteristics with Typical Battery Systems.

Battery Type	Operating Voltage (V)	End-of-Life Voltage (V)	Capacity AA Size (mA - h)	LMV921 Operating time (Hours)
Alkaline	1.5	0.9	1000	6802
Lithium	2.7	2.0	1000	6802
Ni - Cad	1.2	0.9	375	2551
NMH	1.2	1.0	500	3401

Typical Applications

1.0 Half-wave Rectifier with Rail-To-Ground Output Swing

Since the LMV921 input common mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is needed are two external resistors; there is no need for diodes or matched resistors. The half wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

In *Figure 5* the circuit is referenced to ground, while in *Figure 6* the circuit is biased to the positive supply. These configurations implement the half wave rectifier since the LMV921 can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier can not swing the output beyond either rail therefore the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage. R_I should be large enough not to load the LMV921.

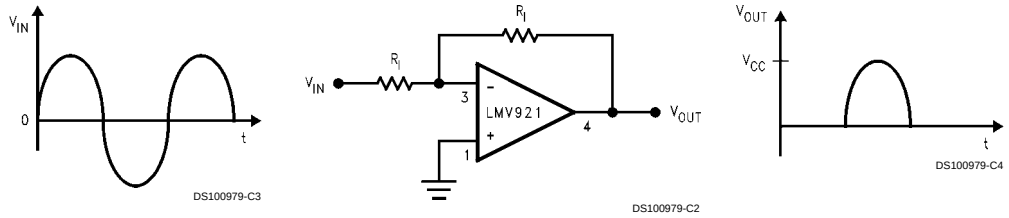


FIGURE 5. Half-Wave Rectifier with Rail-To-Ground Output Swing Referenced to Ground

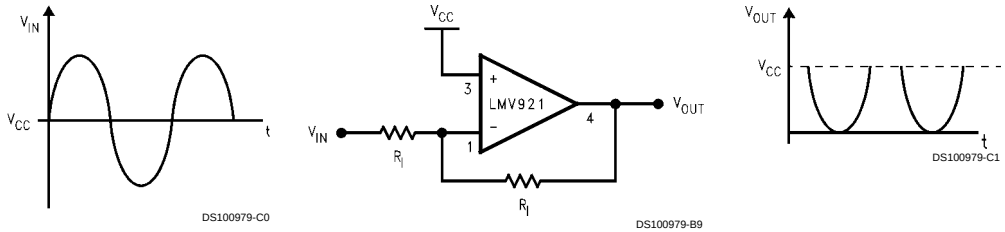


FIGURE 6. Half-Wave Rectifier with Negative-Going Output Referenced to V_{CC}

Typical Applications (Continued)

2.0 Instrumentation Amplifier with Rail-To-Rail Input and Output

Using three LMV921 Amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made.

Some manufactures use a precision voltage divider array of 5 resistors to divide the common mode voltage to get a rail-to-rail input range. The problem with this method is that it also divides the signal, so in order to get unity gain, the amplifier must be run at high loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMRR as well. Using the LMV921 eliminates all of these problems.

In this example, amplifiers A and B act as buffers to the differential stage. These buffers assure that the input impedance is very high and require no precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching R_1-R_2 with R_3-R_4.

The gain is set by the ratio of R_2/R_1 and R_3 should equal R_1 and R_4 equal R_2.

With both rail-to-rail input and output ranges, the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common mode voltages plus the signal should not be greater that the supplies or limiting will occur. For additional applications, see National Semiconductor application notes AN-29, AN-31, AN-71, and AN-127.

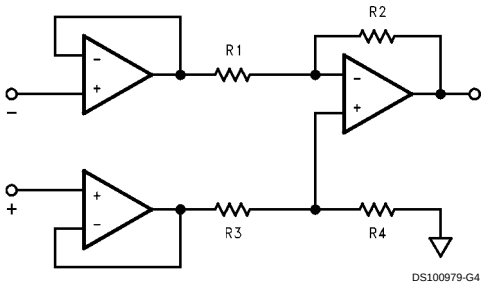
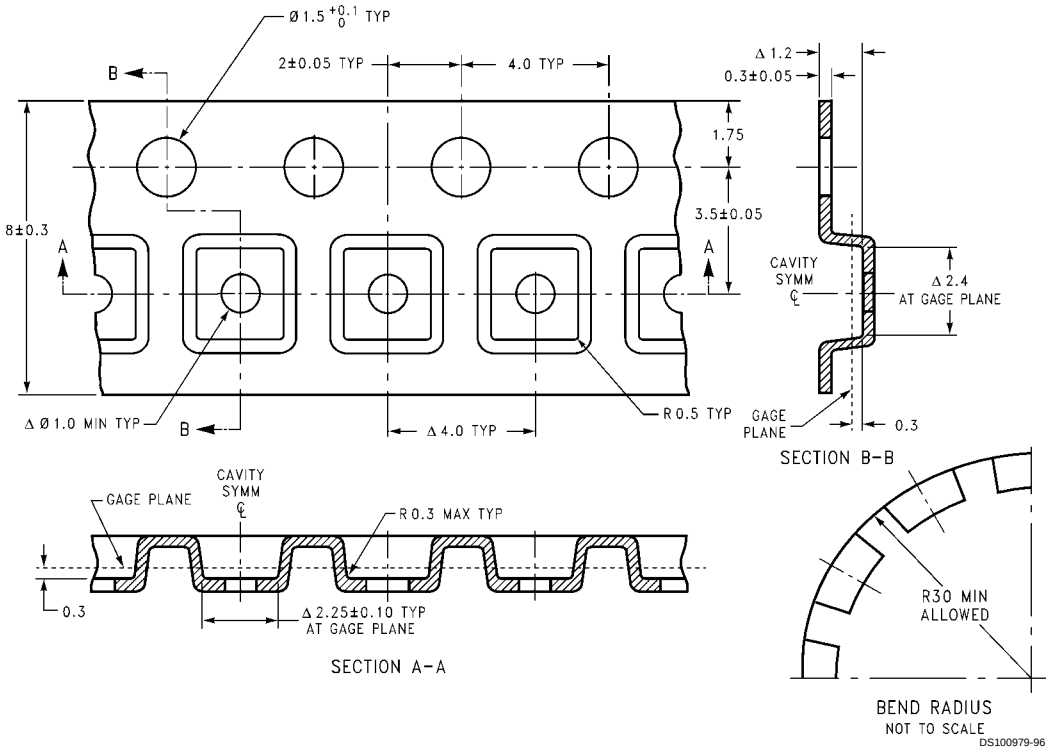


Figure 7. Rail-to-rail instumentation amplifier using three LMV921 amplifiers

SC70-5 Tape Dimensions

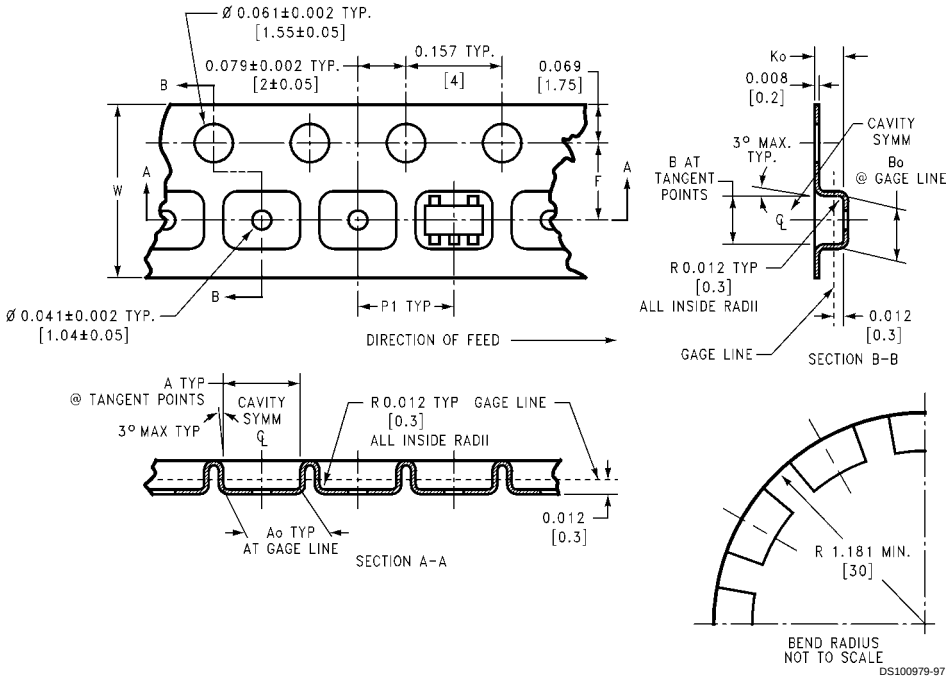


SOT23-5 and SC70-5 Tape Format

Tape Format

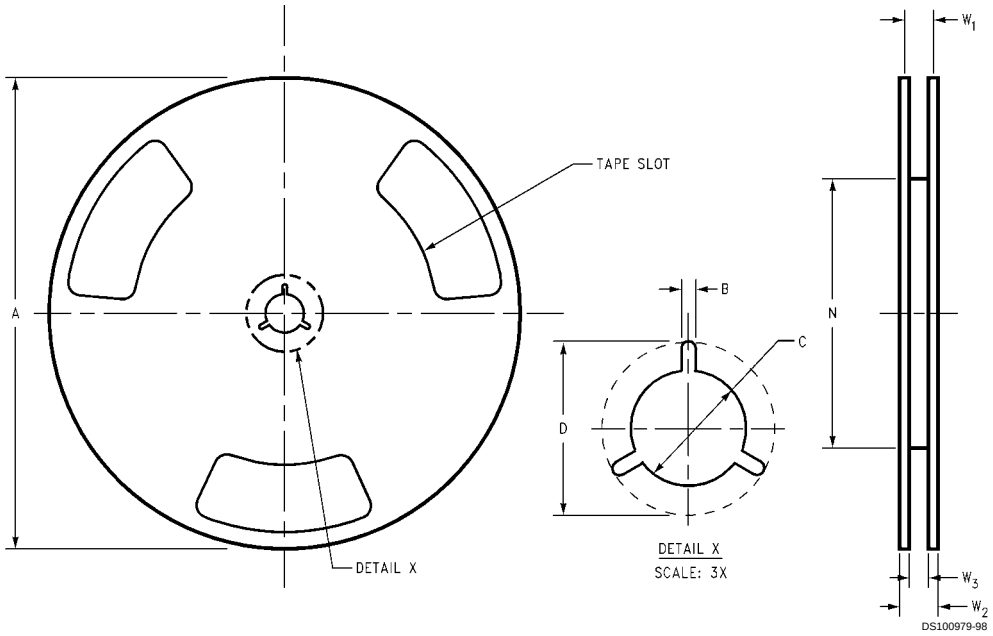
Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader	0 (min)	Empty	Sealed
(Start End)	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer	125 (min)	Empty	Sealed
(Hub End)	0 (min)	Empty	Sealed

SOT23-5 Tape Dimensions



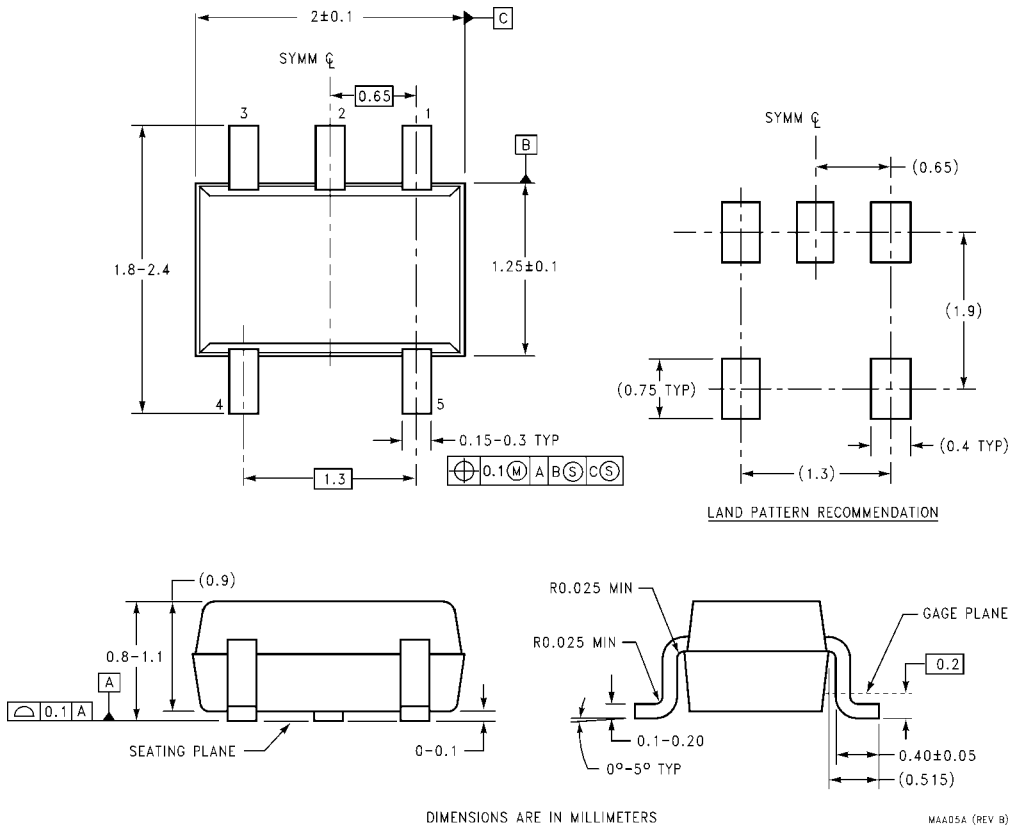
8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

SOT23-5 and SC70-5 Reel Dimensions



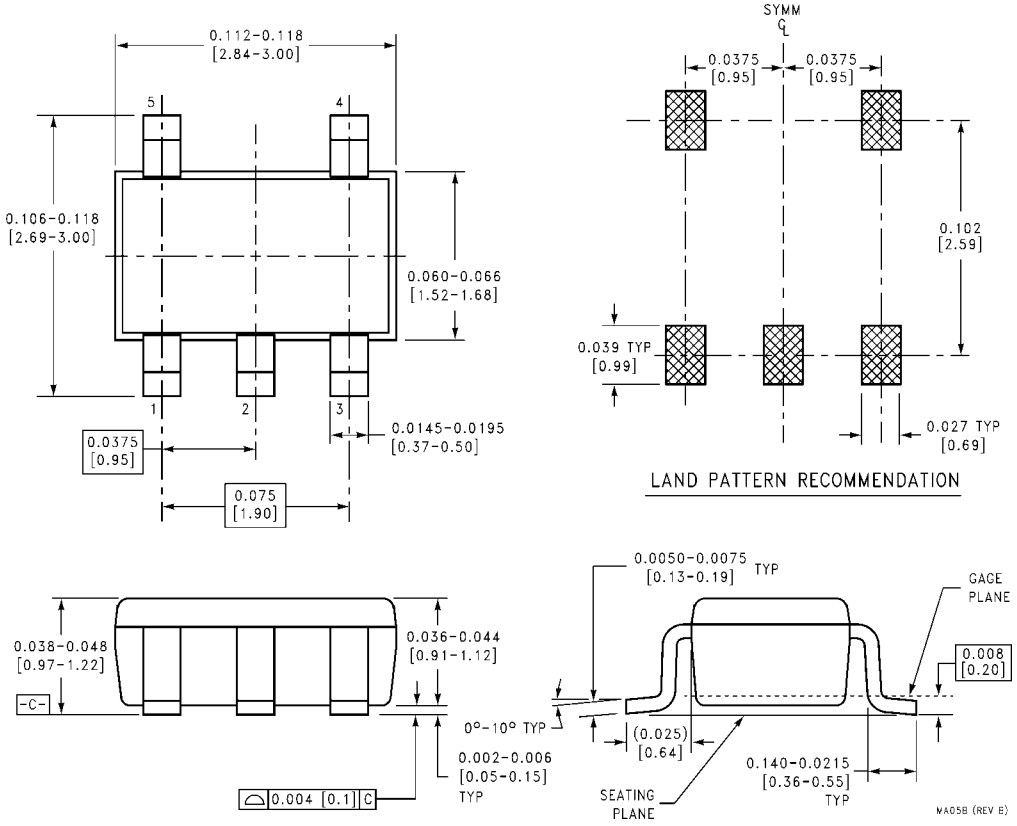
8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 + 0.059/−0.000 8.40 + 1.50/−0.00	0.567 14.40	W1+ 0.078/−0.039 W1 + 2.00/−1.00
Tape Size	A	B	C	D	N	W1	W2	W3

Physical Dimensions inches (millimeters) unless otherwise noted



SC70-5
Order Number LMV921M7 or LMV921M7X
NS Package Number MAA05A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



SOT 23-5
Order Number LMV921M5 or LMV921M5X
NS Package Number MA05B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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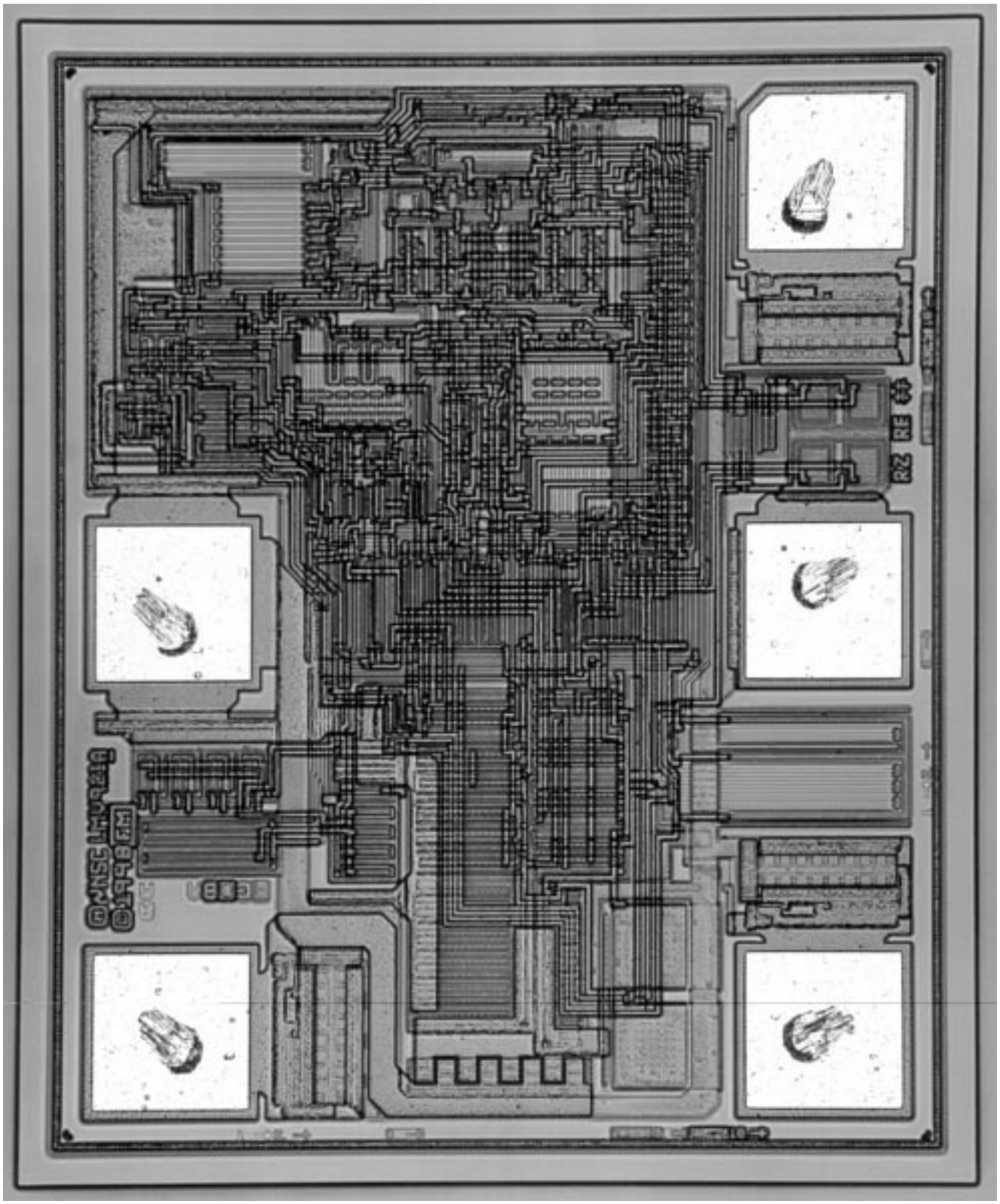
2.2 Die Photo



3.0 PROCESS INFORMATION

3.1 Process Details

Fabrication Site: South Portland Fairchild
Process Technology: CS80CBI (Submicron Silicon Gate CMOS/Bipolar)
Minimum Feature Size: 0.8 microns
Wafer Diameter: 6 inches
Number of Masks: 18
Metallization: 0.5% Copper, dual layer Aluminum metal
1st layer = 7,500 Å thick
2nd layer = 12,000 Å thick
Top Side Passivation: Over Nitride (11,500 Å thick)
Over Oxide (5,000 Å thick)

3.2 Process Detail & Masks

STAGE 1:	Initial Ox
STAGE 2:	Trench Define & Etch
STAGE 3:	Mask 0.6, N-Iso
STAGE 4:	N-Iso Implant
STAGE 5:	N-Iso Drive
STAGE 6:	N-Iso Ox Strip & Screen Ox
STAGE 7:	Mask 0.8, N+ Buried layer
STAGE 8:	N+ Buried Layer Implant
STAGE 9:	Mask 0.9,P+ Buried Layer
STAGE 10:	P+ Buried Layer Implant
STAGE 11:	Buried Layer Anneal
STAGE 12:	Epi Growth
STAGE 13:	Pad Oxide & Nitride
STAGE 14:	Mask 1.0, N-Well
STAGE 15:	N-Well Implant
STAGE 16:	Selective Oxide
STAGE 17:	N-Well Nitride Strip
STAGE 18:	P-Well implant
STAGE 19:	Selective Oxide Etch
STAGE 20:	N-Well & P-Well Drive-In Oxide
STAGE 21:	Drive-In Oxide Strip
STAGE 22:	Mask 2.0, Composite
STAGE 23:	Composite Pad Oxide & Composite Nitride
STAGE 24:	Composite Mask Etch
STAGE 25:	Mask 3.0, P-Field
STAGE 26:	P-Field Implant
STAGE 27:	Iso Field Oxide
STAGE 28:	Active (Composite Area) Nitride Strip
STAGE 29:	Pad Oxide Removal & Sacrificial Oxide Growth & Vt Adjust Implant
STAGE 30:	Sacrificial Oxide Strip & Gate Oxide & Poly Deposition

3.2 Process Detail & Masks (cont)

STAGE 31:	Poly Dope, Poly Anneal
STAGE 32:	Mask 4.0, Poly
STAGE 33:	Poly Etch
STAGE 34:	Poly Seal Oxide
STAGE 35:	Mask 4.3, P-LDD
STAGE 36:	P-LDD Implant
STAGE 37:	Mask 4.5, N-LDD
STAGE 38:	N-LDD Implant
STAGE 39:	Spacer Oxide Deposit & Etch
STAGE 40:	Mask 5.0, N+
STAGE 41:	N+ Implant
STAGE 42:	Mask 5.5, Base
STAGE 43:	Base Etch & Base Implant
STAGE 44:	N+ Drive
STAGE 45:	Mask 6.0, P+
STAGE 46:	P+ Implant
STAGE 47:	Dielectric Layer1 & P+ Anneal
STAGE 48:	SOG
STAGE 49:	Mask 7.0, Window
STAGE 50:	Window Etch & Contact Dielectric
STAGE 51:	Mask 7.1, Contact
STAGE 52:	Contact Etch
STAGE 53:	Contact Plug & Etchback
STAGE 54:	Metal 1 Deposition
STAGE 55:	Mask 8.0, Metal 1
STAGE 56:	Metal 1 Etch
STAGE 57:	Metal 1 Alloy
STAGE 58:	Dielectric Layer2
STAGE 59:	Mask 9.0, Via
STAGE 60:	Via Etch
STAGE 61:	Via Deposition & Metal 2 Deposit
STAGE 62:	Mask 10.0, Metal 2
STAGE 63:	Metal 2 Etch
STAGE 64:	Passivation Oxide/Nitride/Polyamide
STAGE 65:	Mask 13.0, Passivation
STAGE 66:	Passivation Etch

3.3 Masking Sequence

Layer Title	Mask
0.6A	N-Iso
0.8A	N+ Buried Layer
0.9A	P+ Buried Layer
1.0A	N-Well
2.0A	Composite
3.0A	P-Field
3.5A	Cap Implant
4.0A	Poly
4.3A	P-LDD
4.5A	N-LDD
5.0A	N+
5.5A	BASE
6.0A	P+
7.1A	Contact
8.0C	Metal 1
9.0C	Via
10.0B	Metal 2
13.0A	Passivation

4.0 PACKAGING INFORMATION

4.1 Package Material

Generic Package Type	5 Lead SOT23	5 Lead SC-70
NS Package Number	MA05B	MAA005B
Package/Compound	Epoxy Cresol Novolac	Epoxy Cresol Novolac
Manufacturer	Sumitomo	Sumitomo
Package/Compound	Sumitomo EME-6710	Nitto MP-8000C
Manufacturer's Designation	NSC B18	
Lead Frame Material	Copper	Copper
Lead Frame Manufacturer	NSC-DCI	Enomoto
External Lead Frame Coating	Solder Plate Sn/Pb	Solder Plate Sn/Pb
Pins	Gull Wing 6mils Thick	Gull Wing 6mils Thick
Die Attach Method	Eutectic, Cr/Ag/Sn	Eutectic, Cr/Ag/Sn
Bond Wire	Gold, 1.0 mils	Gold, 1.0 mils
Bond Type	Hot Thermosonic Ball	Hot Thermosonic Ball
Package Thermal	265°C/W	478°C/W

4.2 Bonding Diagrams

4.2.1 SC-70

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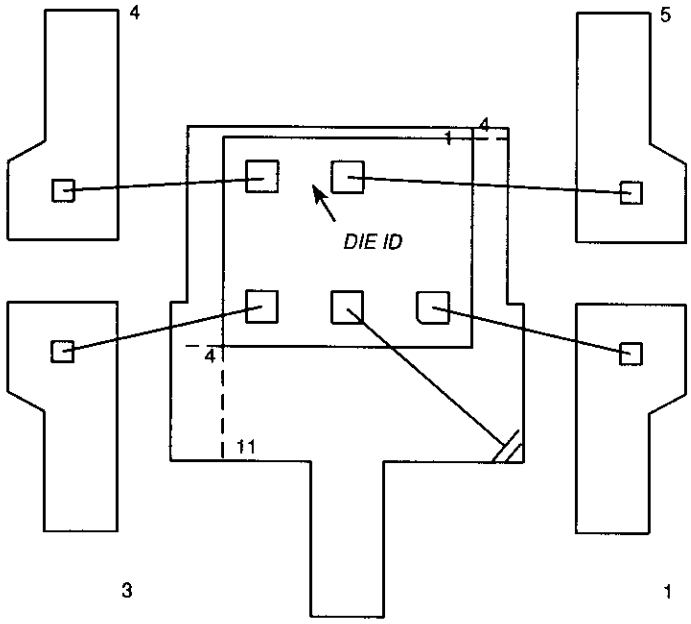

FRAME SK: 022539	DWG: 36-0882-01 PAD: .031 X .032	AD- MAA005AB MB Rev: C PKG: MAA	METALIZ.: 0.5%CU/2M	BOND CODE:
		DIE ID: LMV921AZ STEP/REV: A		
DIE ATTACH SK: N/A	TYPE: N/A	PHYS DIE ID: LMV921A	MBS NOTE: 1. DO NOT BOND TO LEAD NUMBER TW O. 2. L/F STOCK NUMBER 064319. 3 . NSC DWG NUMBER 36-0882-01.	
WIRE SK: 022628 DIA = 0.00100	TYPE: AU # WIRES: 5	DIE SIZE(* CALCULATED) (MIL): 24 X 20 (MIC): 610 X 508 * DIE PLACEMENT X= 4 Y= 11 ANGLE= 0.0		
MOLD COMPOUND SK: N/A	TYPE: N/A	USER NOTE: DIE ATTACH TYPE: EUTECTIC USE MP-8000C MOLD COMPOUND ASSEMBLE AT CARSEM	102198 clxlem 102298 cdkssc	
MIN. PAD PITCH: 10.34 MILS		ASS'Y : LMV921M7	DASH- 02 REV: B	PDCN: BS0758

4.2.2 SOT23-5

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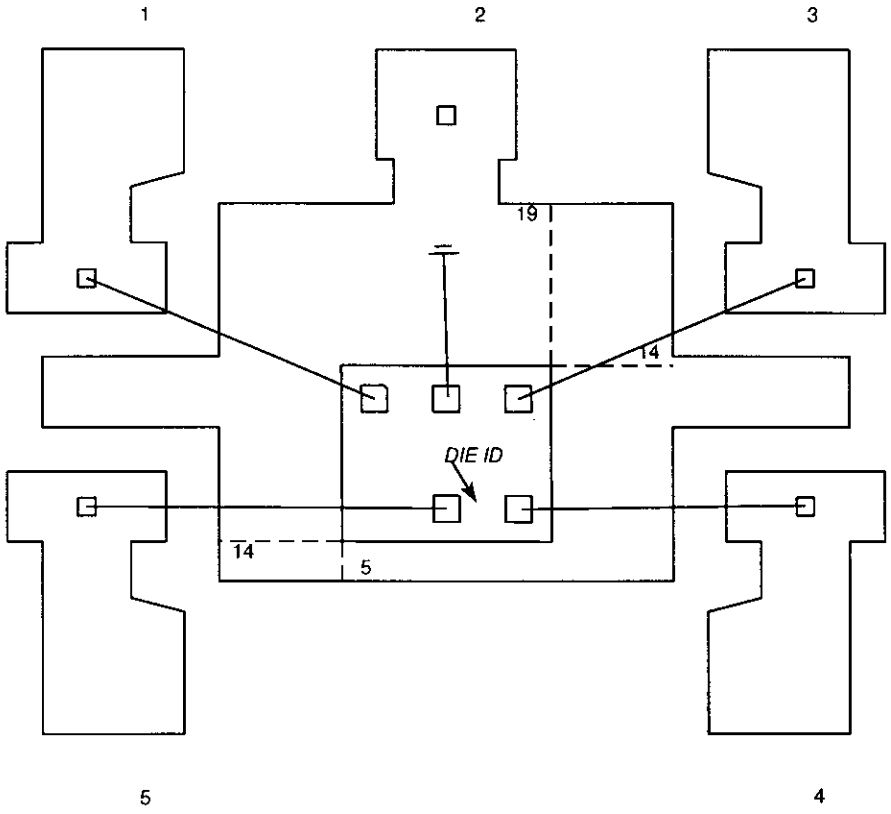

FRAME SK: 061543	DWG: 36-0831-01 PAD: .052 X .043	AD- MA005ACI MB Rev: A PKG: MA DIE ID: LMV921AZ STEP/REV: A	METALIZ.: 0.5%CU/2M BOND CODE:
DIE ATTACH SK: N/A	TYPE: N/A	PHYS DIE ID: LMV921A	
WIRE SK: 022628 DIA = **0.00100**	TYPE: AU # WIRES: 5	DIE SIZE(* CALCULATED) (MIL): 24 X 20 (MIC): 610 X 508 * DIE PLACEMENT X= 14 Y= 5 ANGLE= 0.0	MBS NOTE
MOLD COMPOUND SK: 064764	TYPE: B18	USER NOTE: DIE ATTACH TYPE: EUTECTIC	102698 cllhem 102698 cdkssc
MIN. PAD PITCH: 6.25 MILS		ASS'Y : LMV921M5 DASH- 01 REV: A PDCN: BS0760	

5.0 RELIABILITY DATA

5.1 LMV921 Reliability Report

National Semiconductor

Reliability Test Report

File Number:
FSC19990091
Originator:
Alex Ruiz
Date:March 29, 1999

Purpose

LMV921 Low Voltage
RRIO Op Amp
New Device Qualification

Approvals

Reliability Engineer	Date 4/7/99
Reliability Engineering Manager	Date 4 5 99
Product Line Engineer	Date 4/7/99
Product Line Engineering Manager	Date 4/7/99
Product Line General Manager/V.P.	Date 4/7/99
Corporate Reliability Director	Date 4/7/99
QA&R V.P.	Date 4/7/99

Reference File Numbers

RSC199900984
RSC199900210
Q19980588

Distribution List

APG Reliability: Alex Ruiz, Thai Ta, Nick Stanco
Amplifier Group: Dennis Smith, Carlos Sanchez

Abstract

The LMV921 is being qualified as a new product by the Amplifiers product line. The LMV921 is a low voltage, RRIO op amp processed on CS80CBI and assembled in both the SOT23-5 and the SC70 packages. The LMV921 will be positioned next to the LMC7101, but offers RRIO and equal or better specs than the LMC7101 including operation at 1.8 V and SC70 packaging.

The LMV921 passed all required reliability tests with the exception of MM ESD which passes only 100V. The LMV921 is being released to production with a waiver for MM ESD performance. No corrective action is required for the LMV921, but all derivative products including the dual (LMV922), quad (LMV924) and low-power versions must include design enhancements resulting in 200V or higher MM ESD performance. The datasheet for the LMV921 must show the 100V MM ESD rating.

5.0 RELIABILITY DATA

Description

Test Request	Device Name	Sbgp	Wafer Die Run	Fab Loc	Tech Code	Pkg Code	# Leads	Assy Loc	Date Cd	Mold Cmpd
RSC199900210	LMV921M7	A		FM	BB	N\SC70	5	EM	9852	MP-8000C
RSC199900984	LMV921M5	A		FM	BB	N\TG23	5	EM		B18

Tests Performed

Test: Autoclave Test (ACLV)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900210	LMV921M7	A	100	1 atm	121	0

Test: High Temperature Storage test (bake) (HTSL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900210	LMV921M7	A	0	0	150	0

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900210	LMV921M7	A	0	0	150	0

Test: Temperature Cycle (TMCL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900210	LMV921M7	A	0	0	150	-65

Test: Temperature Humidity Bias Test (THBT)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900210	LMV921M7	A	85	0	85	0

Test: Electrostatic Discharge - Machine Model (ESDM)

Test Request	Device	Method
RSC199900984	LMV921M5	
	Note: package type is SOIC.	ATE

Test: Electrostatic Discharge - Human Body Model (ESDH)

Test Request	Device	Method
RSC199900984	LMV921M5	
	Note: Package type is SOIC.	ATE

Test: Latch Up -Static (LUPS)

Test Request	Device	Fail Criteria	Method
RSC199900984	LMV921M5		
	Note: Package type is SOIC.	0002	ATE

IB1 Preconditioning Flow: all THBT, TMCL and ACLV units were subjected to the following preconditioning flow prior to stress testing.

temp cycle - 5 cycles at -40/60C → bake - 16 hours at 125C → moisture sensitivity level 1 - moisture soak for 168 hours at 85C and 85%RH → 235C IR reflow , 3 passes → Flux immersion → DI water rinse → dry → electrical test

Environmental Test Results

Tests	Time-Point (hrs)	Lot A	Lot B
DOPL (Dynamic Operating Life)	168	0/100	-
	500	0/100	-
	1000	0/100	-

Environmental Test Results (continued)

Tests	Time-Point (hrs)	Number of Failures
ACLV (Autoclave)	168	0/50
TMCL (Temp Cycle)	500	0/100
	1000	0/100
THBT (Temp Humidity Bias Test)	168	0/100
	500	0/100
	1000	0/100
HTSL (High Temperature Storage Test)	500	0/100
	1000	0/100

ESD (Electro-Static Discharge) Test Results

Tests	Voltage (V)	Number of Failures
ESD Human Body Model	500	0/4
	1000	0/4
	1500	0/4
	2000	0/4
	2500	4/4
ESD Machine Model	50	0/4
	100	0/4
	150	2/4
	200	0/4
	250	4/4

Latch-up Test Results

Tests	Temperature (C)	Number of Failures
Latch-up	25	0/5
	70	0/5

Qualification Requirements and Status Summary

Tests	Requirements	Status
DOPL (Dynamic Operating Life)	500 hours	Pass
ACLV (Autoclave)	168 hours	Pass
TMCL (Temp Cycle)	500 hours	Pass
THBT (Temp Humidity Bias Test)	500 hours	Pass
HTSL (High Temp Storage)	500 hours	Pass
ESD Human Body Model	2000 V	Pass
ESD Machine Model	200 V	Fail (release with waiver)
Latch-up	25 and 70 C	Pass

FIT and EFR Calculation

FIT (Failure Unit) – a measure of failure rate, defined as one failure in on billion device-hours.

Assume: 1) Tj = 150 C
2) Tj Application = 55 C
3) Activation Energy = 0.7 ev
4) Acceleration Factor = 259.07
5) Confidence Factor = 60%

Then:
FIT = 35.37 failures per one billion device-hours

5.0 RELIABILITY DATA

Conclusion

The LMV921 product qualification has successfully satisfied all reliability requirements per qual plan Q19980588 with the exception of Machine Model (MM) ESD testing. The LMV921 is being released to production with a waiver for MM ESD performance with no requirement for corrective action on the LMV921. As a condition of this waiver all future derivative products, including planned dual, quad and low-power versions of the LMV921 must meet a minimum of 200V MM ESD prior to release.

The LMV921 is now fully qualified and approved for production release in both the 5L SOT-23 and 5L SC70 packages.

National Semiconductor supplies a comprehensive set of service and support capabilities. Complete product information and design support is available from National's customer support centers.

To receive sales literature and technical assistance, contact the National support center in your area.

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