

Document Title

128Kx8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Design target	September 9, 1998	Preliminary
1.0	Finalize - Change Icc1 : 3 to 4mA	April 13, 1998	Final

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128Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : TFT
- Organization : 128Kx8
- Power Supply Voltage
 - KM68V1000E Family : 3.0V ~ 3.6V
 - KM68U1000E Family : 2.7V ~ 3.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 32-SOP, 32-TSOP1-0820F, 32-TSOP1-0813.4F

GENERAL DESCRIPTION

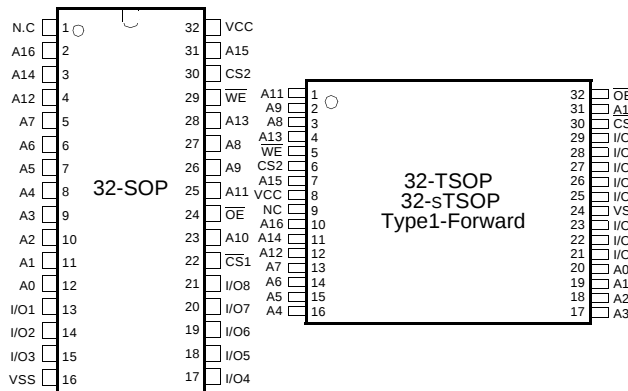
The KM68V1000E and KM68U1000E families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
KM68V1000EL-L KM68U1000EL-L	Commercial(0~70°C)	3.0~3.6V 2.7~3.3V	70 ¹⁾ /100	10μA	30mA	32-SOP 32-TSOP1-0820F 32-TSOP1-0813.4F
KM68V1000ELI-L KM68U1000ELI-L	Industrial(-40~85°C)	3.0~3.6V 2.7~3.3V				

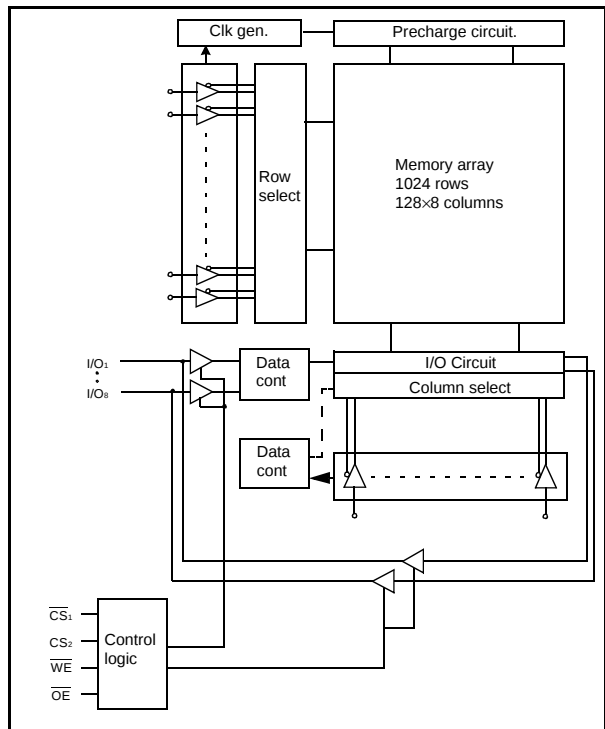
1. The parameters are tested with 30pF test load

PIN DESCRIPTION



Name	Function
A0~A16	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}, \overline{CS2}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
KM68V1000ELG-7L	32-SOP, 70ns, 3.3V	KM68V1000ELGI-7L	32-SOP, 70ns, 3.3V
KM68V1000ELG-10L	32-SOP, 100ns, 3.3V	KM68V1000ELGI-10L	32-SOP, 100ns, 3.3V
KM68V1000ELT-7L	32-TSOP F, 70ns, 3.3V	KM68V1000ELTI-7L	32-TSOP F, 70ns, 3.3V
KM68V1000ELT-10L	32-TSOP F, 100ns, 3.3V	KM68V1000ELTI-10L	32-TSOP F, 100ns, 3.3V
KM68V1000ELTG-7L	32-sTSOP F, 70ns, 3.3V	KM68V1000ELTGI-7L	32-sTSOP F, 70ns, 3.3V
KM68V1000ELTG-10L	32-sTSOP F, 100ns, 3.3V	KM68V1000ELTGI-10L	32-sTSOP F, 100ns, 3.3V
KM68U1000ELG-7L	32-SOP, 70ns, 3.0V	KM68U1000ELGI-7L	32-SOP, 70ns, 3.0V
KM68U1000ELG-10L	32-SOP, 100ns, 3.0V	KM68U1000ELGI-10L	32-SOP, 100ns, 3.0V
KM68U1000ELT-7L	32-TSOP F, 70ns, 3.0V	KM68U1000ELTI-7L	32-TSOP F, 70ns, 3.0V
KM68U1000ELT-10L	32-TSOP F, 100ns, 3.0V	KM68U1000ELTI-10L	32-TSOP F, 100ns, 3.0V
KM68U1000ELTG-7L	32-sTSOP F, 70ns, 3.0V	KM68U1000ELTGI-7L	32-sTSOP F, 70ns, 3.0V
KM68U1000ELTG-10L	32-sTSOP F, 100ns, 3.0V	KM68U1000ELTGI-10L	32-sTSOP F, 100ns, 3.0V

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM68V1000EL, KM68U1000EL
		-40 to 85	°C	KM68V1000ELI, KM68U1000ELI

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	KM68V1000E Family KM68U1000E Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	KM68V1000E, KM68U1000E Family	2.2	-	V _{CC} +0.3	V
Input low voltage	V _{IL}	KM68V1000E, KM68U1000E Family	-0.3 ³⁾	-	0.6	V

Note:

1. Commercial Product : T_A=0 to 70°C, otherwise specified
Industrial Product : T_A=-40 to 85°C, otherwise specified
2. Overshoot : V_{CC}+2.0V in case of pulse width≤30ns
3. Undershoot : -2.0V in case of pulse width≤30ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

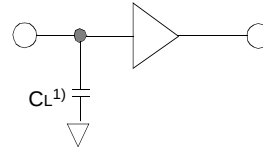
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS_1}$ =V _{IH} or CS ₂ =V _{IL} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL} , Read	-	-	4	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS_1}$ ≤0.2V, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V	-	-	4	mA
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	25	30	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS_1}$ =V _{IH} , CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	0.3	mA
Standby Current(CMOS)	I _{SB1}	$\overline{CS_1}$ ≥V _{CC} -0.2V, CS ₂ ≥V _{CC} -0.2V or CS ₂ ≤0.2V, Other inputs=0~V _{CC}	-	0.2	10	μA

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V
 Input rising and falling time : 5ns
 Input and output reference voltage :1.5V
 Output load(see right) : $C_L=100\text{pF}+1\text{TTL}$
 $C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS (KM68V1000E Family : $V_{CC}=3.0\sim3.6\text{V}$, KM68U1000E Family : $V_{CC}=2.7\sim3.3\text{V}$ Commercial Product : $T_A=0$ to 70°C , Industrial Product : $T_A=-40$ to 85°C)

Parameter List		Symbol	Speed Bins				Units
			70ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	trc	70	-	100	-	ns
	Address access time	tAA	-	70	-	100	ns
	Chip select to output	tCO1, tCO2	-	70	-	100	ns
	Output enable to valid output	toE	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	30	ns
	Output disable to high-Z output	toHZ	0	25	0	30	ns
	Output hold from address change	toH	10	-	15	-	ns
Write	Write cycle time	twc	70	-	100	-	ns
	Chip select to end of write	tcw	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	80	-	ns
	Write pulse width	tWP	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	ns
	Data to write time overlap	tdw	30	-	40	-	ns
	Data hold from write time	tdH	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	ns

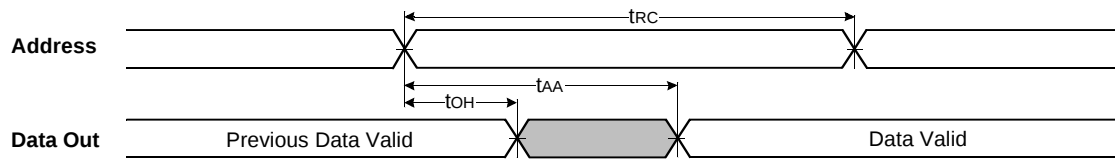
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for data retention	V_{DR}	$\overline{CS}_1 \geq V_{CC}-0.2V^{(1)}$	2.0	-	3.6	V
Data retention current	I_{DR}	$V_{CC}=3.0V, \overline{CS}_1 \geq V_{CC}-0.2V^{(1)}$	-	0.2	10	μA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t_{RDR}		5	-	-	

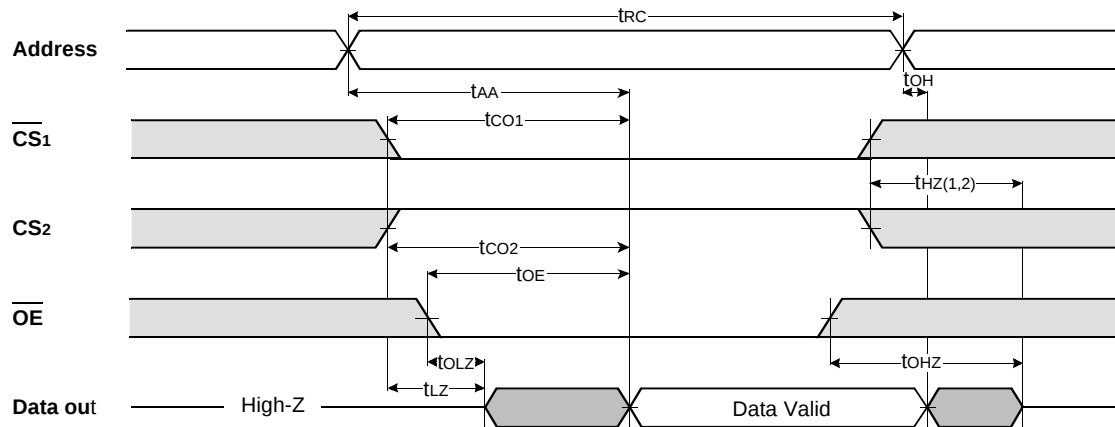
1. $\overline{CS}_1 \geq V_{CC}-0.2V$, $\overline{CS}_2 \geq V_{CC}-0.2V$ ($\overline{CS}_1$ controlled) or $\overline{CS}_2 \leq 0.2V$ ($\overline{CS}_2$ controlled)

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$)



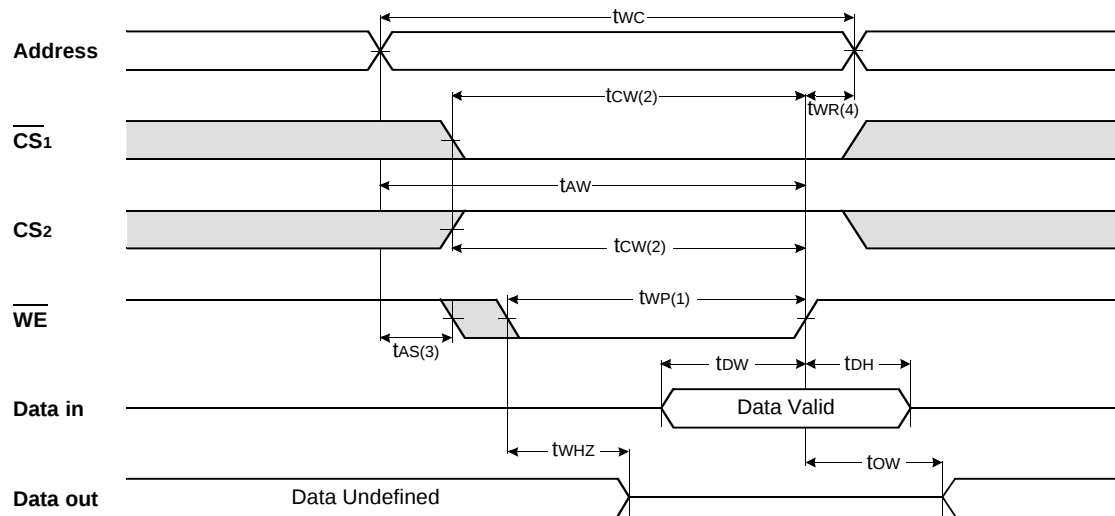
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



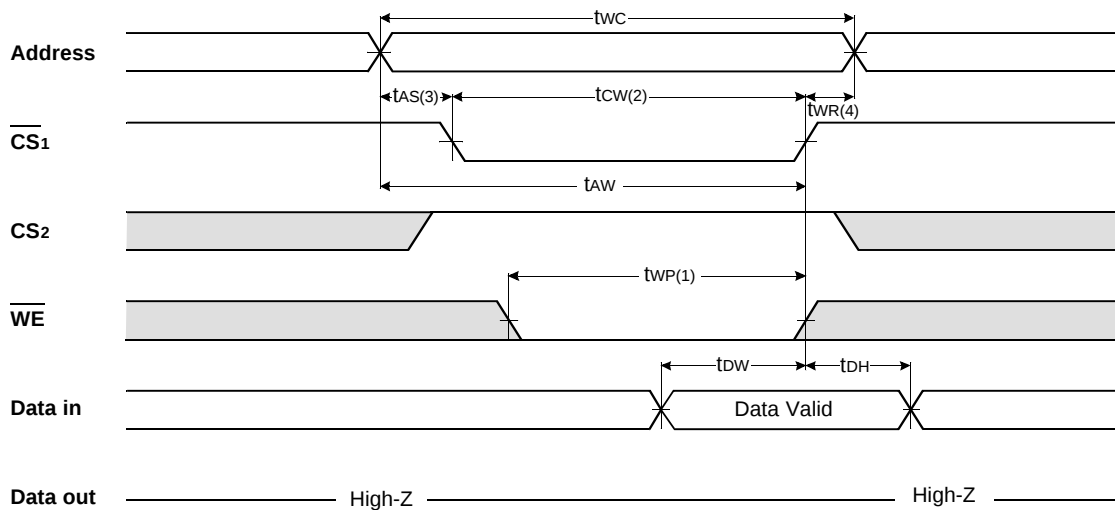
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

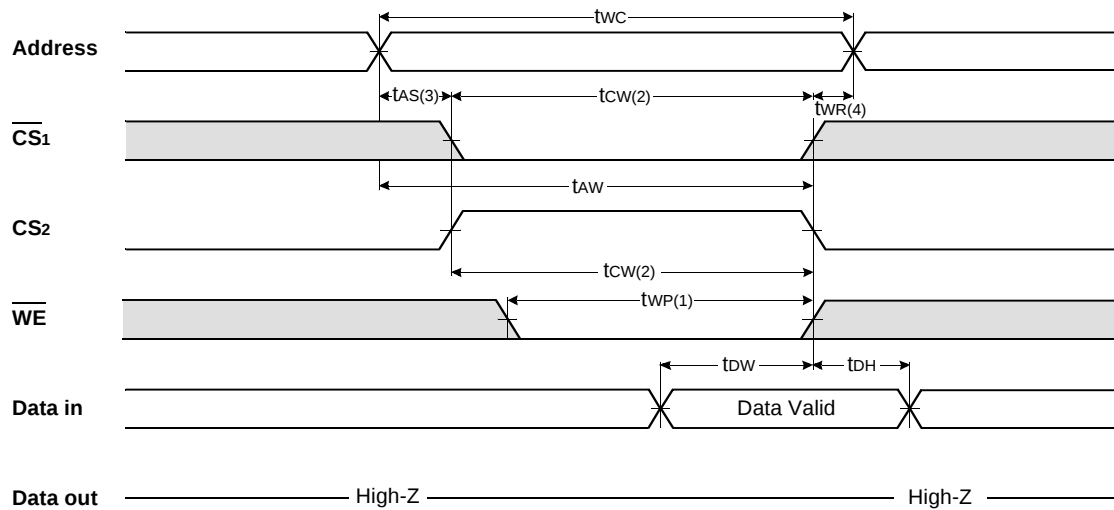
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS1}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

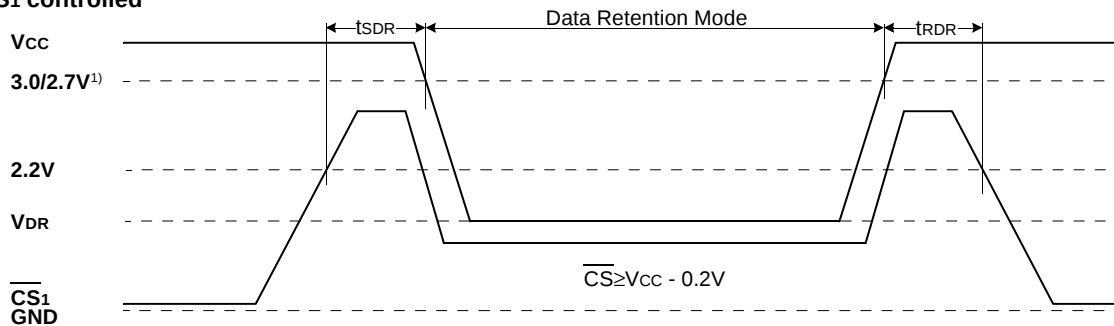


NOTES (WRITE CYCLE)

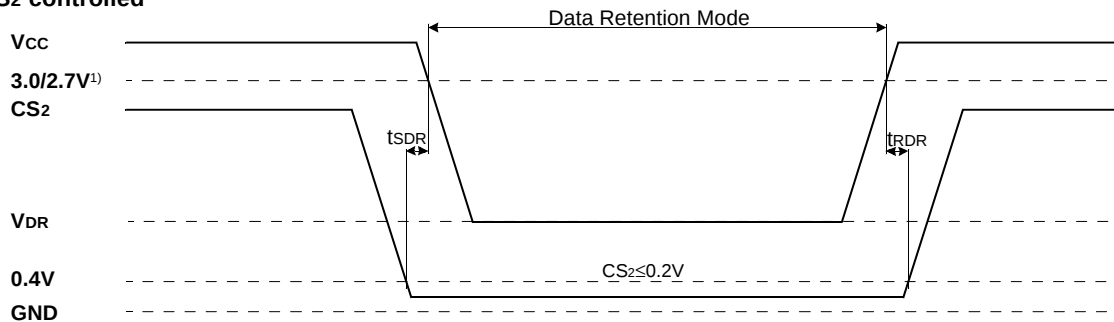
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low : A write ends at the earliest transition among CS_1 going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the CS_1 going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high t_{WR2} applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

CS₁ controlled



CS₂ controlled



1. 3.0V for KM68V1000E Family, 2.7V for KM68U1000E Family

Units: millimeters(inches)

The drawing illustrates the mechanical specifications of a 32-pin Quad Flat Pack (QFP) package. It includes three views: a top view, a side view, and a detail view of the lead profile.

Top View Dimensions:

- Pin 1 location: 0.71 ± 0.028 mm
- Pin pitch: 0.41 ± 0.004 mm
- Distance from pin 1 to pin 17: 20.87 ± 0.822 mm
- Distance from pin 1 to pin 16: 20.47 ± 0.806 mm
- Distance from pin 1 to pin 15: 1.27 ± 0.050 mm
- Distance from pin 1 to pin 14: 0.05 ± 0.002 mm
- Distance from pin 1 to pin 13: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 12: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 11: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 10: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 9: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 8: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 7: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 6: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 5: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 4: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 3: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 2: 0.016 ± 0.002 mm
- Distance from pin 1 to pin 1: 0.016 ± 0.002 mm

Side View Dimensions:

- Package height: 14.12 ± 0.556 mm
- Lead height: 11.43 ± 0.450 mm
- Lead thickness: 13.34 ± 0.525 mm
- Lead angle: $0-8^\circ$
- Lead width: 0.20 ± 0.10 mm
- Lead thickness: 0.008 ± 0.004 mm
- Lead width: 0.80 ± 0.20 mm
- Lead thickness: 0.031 ± 0.008 mm

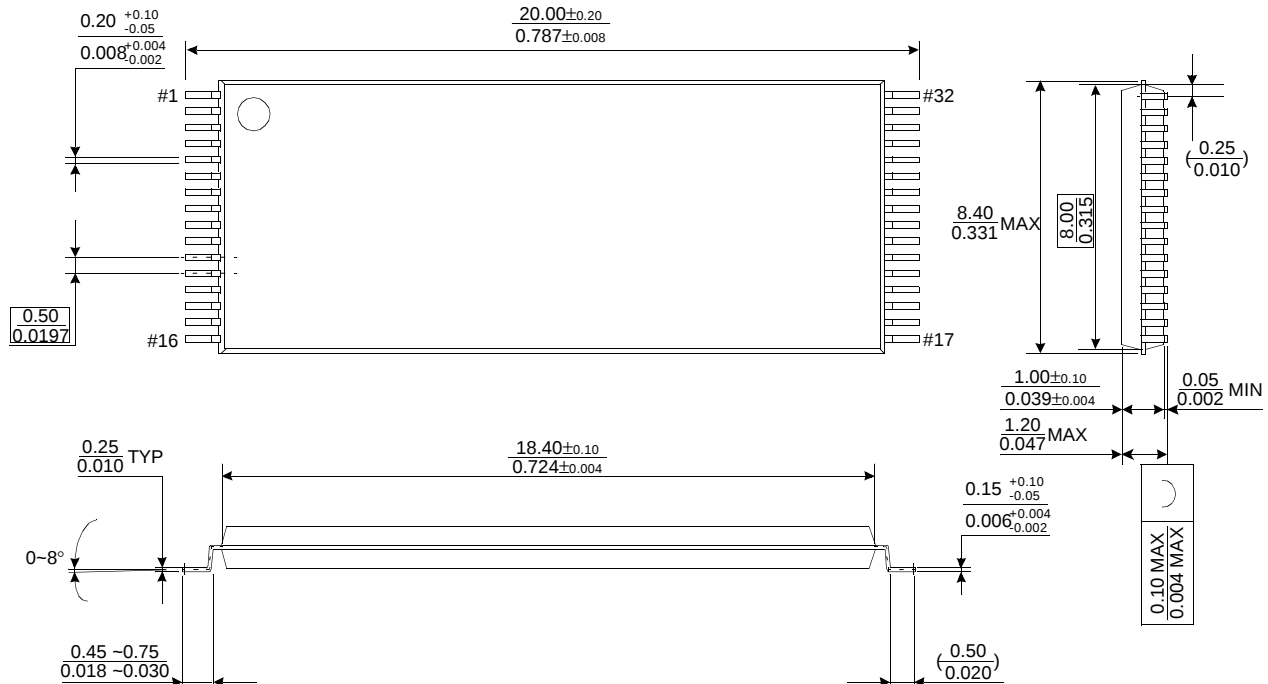
Detail View Dimensions:

- Lead thickness: 0.10 ± 0.004 mm
- Lead width: 0.10 ± 0.004 mm

PACKAGE DIMENSIONS

Units: millimeters(inches)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)

