

## 15.1 Introduction

Since the introduction of Chip Scale Packages (CSP's) only a few short years ago, they have become one of the biggest packaging trends in recent history. There are currently over 50 different types of CSP's available throughout the industry and the numbers are increasing almost daily.

Intel Flash memory products began using CSP's in the  $\mu$ BGA\* package a few years ago and have expanded into multiple types of CSP's in order to meet the needs of new product functionality and applications. Currently, the majority of Intel's CSP's are used for flash memory products. However, other types of Intel products are beginning to take advantage of the benefits of CSP's as well.

CSP's are evolving so rapidly, that by the time you read this chapter, there will probably be new package information and design considerations to take into account. Intel has attempted to include as much as possible in this chapter, reviewing many different areas such as package information, application considerations, printed circuit board (PCB) design and manufacturing tips and tools. However, since CSP's are continually evolving, the contents of this chapter will continue to evolve. Therefore, until new versions of this package guide are printed, new CSP information and manufacturing considerations for Intel Flash Memory products will continue to be updated in the Flash Memory CSP User's Guide on the WWW at:

<http://developer.intel.com/design/flash/packtech/index.htm>.

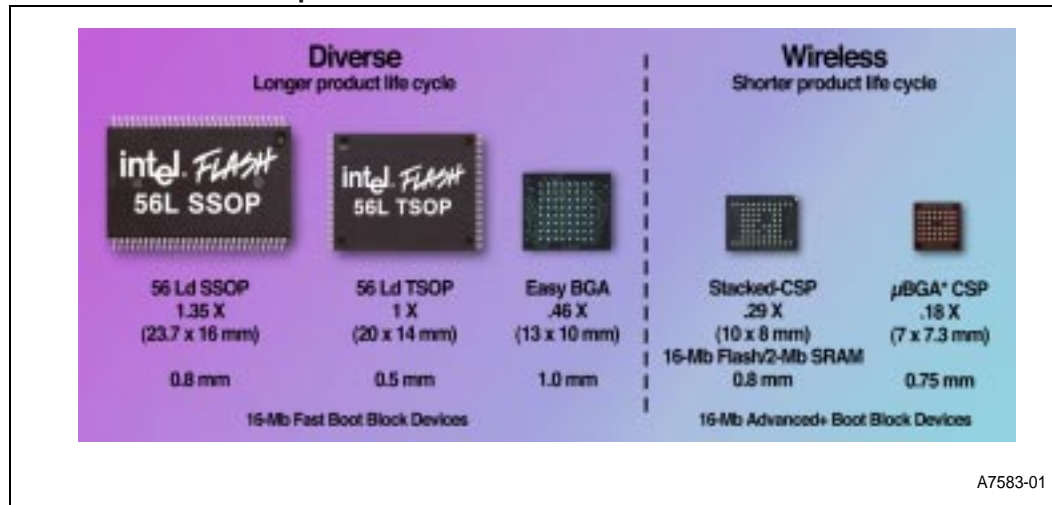
There are many reasons why CSPs have been so well accepted within the industry. One of the biggest advantages of CSPs is the size reduction of the package (see figure 15.1) vs. more traditional peripherally leaded packages. This is mainly due to the Ball Grid Array (BGA) design of the package. By designing all interconnects under the package in the BGA style, you can increase the number of interconnects while saving PCB routing space. Other manufacturing advantages of CSPs include the self alignment characteristics during PCB assembly reflow and lack of bent leads which cause coplanarity issues. Both of these CSP features increase PCB assembly yields and lower manufacturing costs.

One of the barriers for new packages to be accepted in the industry is the lack of existing Surface Mount Technology (SMT) infrastructure such as assembly and manufacturing processes and equipment. This is not the case for CSPs which take advantage of existing infrastructure and in most cases require no capital equipment investment to implement CSPs .

In the past, CSP's have been defined as a package that is 1.2X the size of the die. However, some types of CSPs maintain their package size as the internal silicon die reduces in size as a result of the fabrication lithography process gets smaller (die shrink). This effect changes the package to die size ratio. As CSP's have evolved, the definition has changed to "near die size packages with a ball pitch of 1mm or less".

As mentioned earlier, Intel has introduced several different types of CSP packages. This is because each application has different requirements. Since almost every application varies, there are many considerations to take into account when selecting the best package for the application. Please refer to the "Package Usage" section of this chapter to review this in more detail.

Figure 15-1. CSP vs. SOP Size Comparisons



## 15.2 Package Dimensions & Attributes

**Note:** Please refer to the web-based mechanical Spec for up to date package dimensions at:

<http://www.intel.com/design/flash/packtech/index.htm>

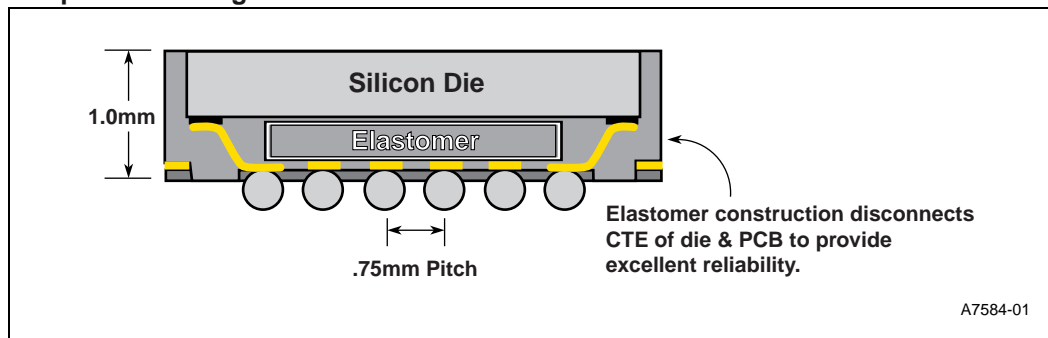
This section reviews CSP specific information such as various CSP construction, material sets, attributes, and dimensional examples. It also explains the use and construction of various mechanical samples referred to as Silicon Daisy Chain (SDC) samples to be used for mechanical /process equipment set-up and evaluation.

### 15.2.1 The μBGA Package

The μBGA package is a true chip size package. Because of this, the actual package dimensions are dependent on the size of the silicon die. This section will show general package dimensions for the μBGA package. Please refer to the mechanical specification document on Intel's website, or contact your Intel representative for the latest, complete package dimensions, pinouts, and schematics.

The μBGA package (Figure 15.2) is a .75mm and .5mm ball pitch package and takes full advantage of any reduction of silicon die size. This makes the μBGA package the smallest discrete Intel flash memory package. Its unique construction utilizes a layer of elastomer which decouples the stresses caused by the coefficient of thermal expansion (CTE) of the silicon die and the PCB material during temperature variations.

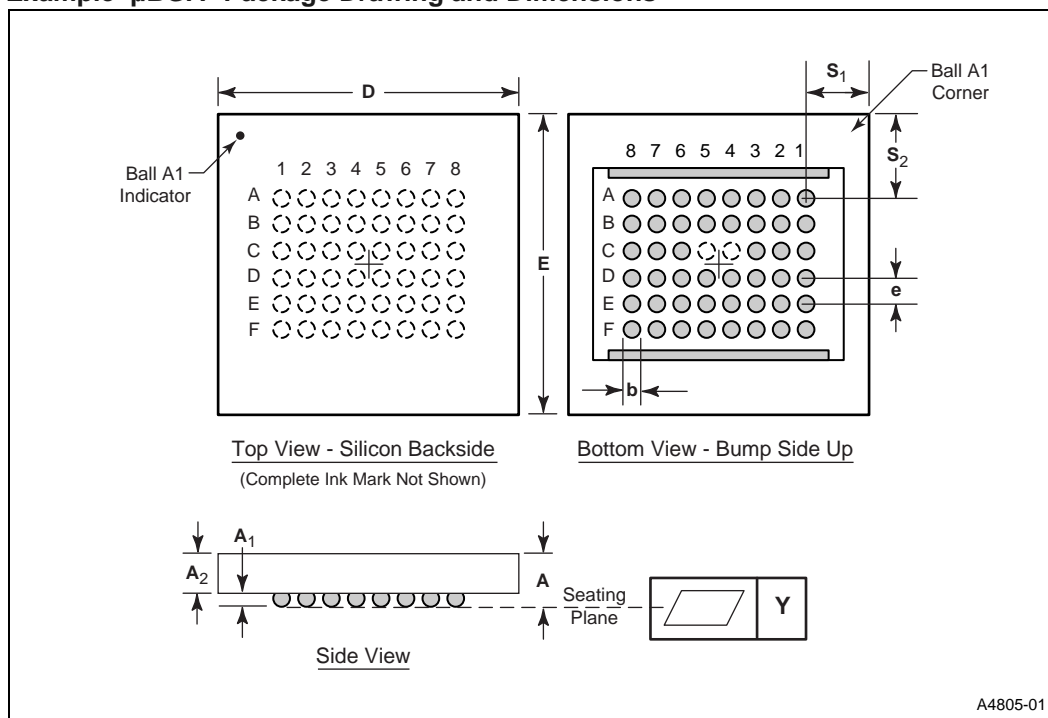
Figure 15-2. The  $\mu$ BGA\* Package



Since the size of the package equals the size of the die, as the die gets smaller due to fabrication lithography process reductions (die shrinks), so does the package. At a certain point, the associated ball pitch will get smaller as well, in order to accommodate the smaller size of the die. This eventually leads to ball pitches as small as .5mm and below. Currently the majority of  $\mu$ bga packages are in .75mm pitch.

## 15.2.2 $\mu$ BGA\* Package Drawing and Dimensions

Figure 15-3. Example  $\mu$ BGA\* Package Drawing and Dimensions



**Note:** The  $\mu$ BGA package is die-size dependent and may vary. Actual products vary with different levels of matrix ball depopulation. Refer to the  $\mu$ BGA\* Package Mechanical and Shipping Media Specifications for specific product/package dimensions/drawings and pinouts at:

<http://www.intel.com/design/flash/packtech/index.htm>

Table 15-1. Generic  $\mu$ BGA\* Package Dimensions

Symbol		Millimeters				Inches		
		Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A	0.850		1.000		0.0335		0.0394
Ball Height	A1	0.150				0.0059		
Package Body Thickness	A2	0.600	0.700	0.800		0.0236	0.0276	0.0315
Ball (Lead) Width (all .75mm pitch)	b	0.300	0.350	0.400		0.0118	0.0138	0.0157
Ball (Lead) Width (all .50mm pitch)	b	0.259	0.309	0.359		0.0102	0.0122	0.0141
Seating Plane Coplanarity	Y			0.100				0.0039
Package Body Width	D	See $\mu$ BGA Package Attribute Table						
Package Body Length	E							
Pitch	[e]							
ball (Lead) Count	N							
Corner to Ball A1 Distance Along D	S1							
Corner to Ball A1 Distance Along E	S2							

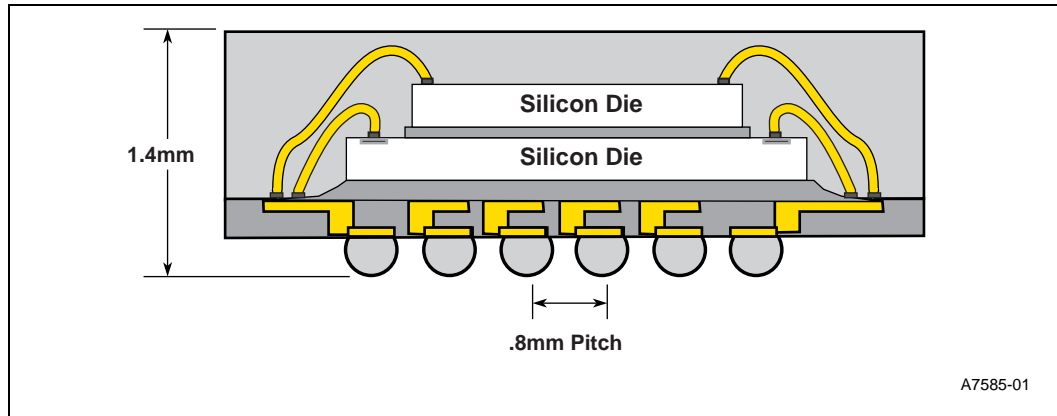
Table 15-2.  $\mu$ BGA Package Attributes

μBGA Product Name	Ball Pitch	Square/ Rect.	Package Weight (mg)	Matrix (active)	Actual Ball Count	D Nom	E Nom	S1	S2	SDC's <sup>2</sup>
GT28F008/800B3	.75	R	60	6x8	46	7.910	6.500	1.330	1.375	
GT28F016/160B3 GT28F160C3	.75	R	51	6x8	46	7.286	6.964	1.018	1.607	Y
GT28F320C3	.75	R	83	6x8	47	7.286	10.850	1.018	3.550	
GT28F160F3	.75	R	102	6x10	53	8.000	10.240	.625	3.245	
G28F640J5	.75	R	59	9x8	52	7.670	16.370	1.214	5.935	Y
BG28F160C18	.5	R	TBD	5x11	46	6.794	7.530	.897	2.765	Y
GT28F320D18	.75	R	TBD	7x8	58	7.520	13.420			
Shipping Media	All μBGA products are available in Tape & Reel or Trays									
Desiccant Pack <sup>1</sup>	All μBGA products are IPC Level 2									
1. Desiccant Pack levels relate to IPC Moisture Sensitivity Levels 2. SDC's represent the mechanical samples available in the various package size/type equivalents <b>NOTE:</b> All Dimensions in mm										

### 15.2.3 The Intel® Stacked CSP

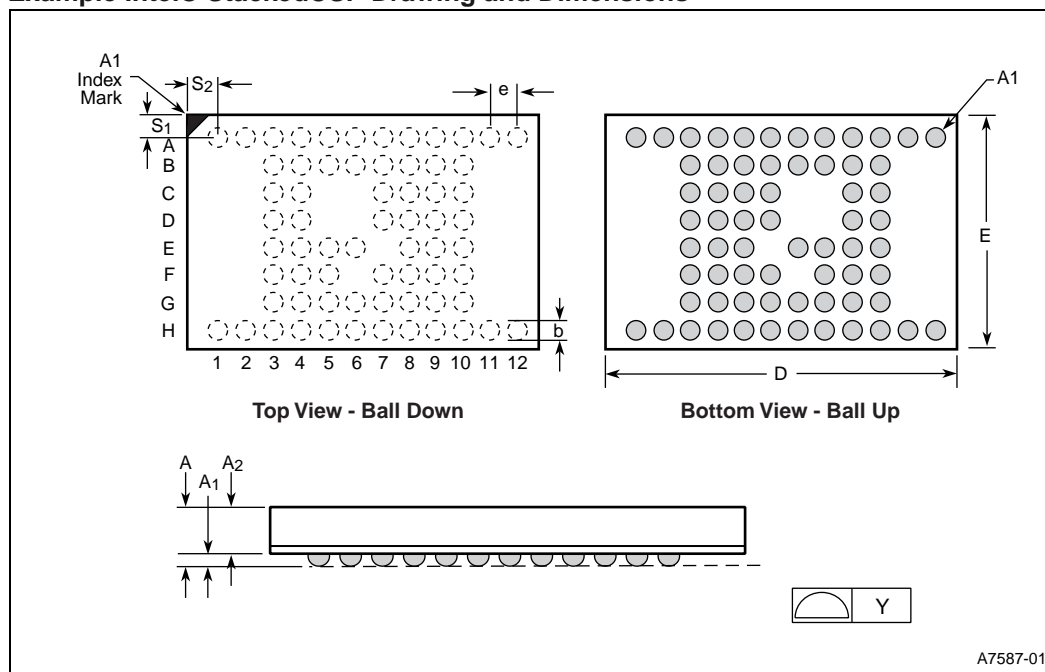
Another type of CSP gaining momentum in the industry is the "stacked" CSP (Intel® StackedCSP). These packages are taking advantage of multiple application requirements, such as SRAM and Flash, and combining both die into one package (see figure 3.3). However, instead of placing the individual die side by side (such as multi-chip modules), the Intel® StackedCSP stacks the two die on top of each other to get the maximum space savings advantage possible. Although the package may have a larger ball pitch as compared to the  $\mu$ BGA packages (.8mm vs. .75 & .5mm), the overall PCB area of the Intel® StackedCSP is smaller than the combined area of the two separate components.

Figure 15-4. Intel® Stacked CSP



## 15.2.4 Intel® Stacked CSP Package Drawings & Dimensions

Figure 15-5. Example Intel® StackedCSP Drawing and Dimensions



**Note:** Refer to the Intel® StackedCSP Package Mechanical and Shipping Media Specifications for specific product/package dimensions/drawings and pinouts at:

<http://www.intel.com/design/flash/packtech/index.htm>

Table 15-3. Generic Intel® StackedCSP Dimensions

	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Height	A	1.20	1.30	1.40	0.047	0.051	0.055
Ball Standoff	A1	0.30	0.35	0.40	0.012	0.014	0.016
Package Body Thickness	A2	0.92	0.97	1.02	0.036	0.038	0.040
Seating Plane Coplanarity	Y			0.1			0.004
Pitch	e		0.80			0.031	
Lead Count	N		72			72	
Package Body Width	D	See Intel® Stacked CSP Attributes Table					
Package Body Length	E						
Corner to First Bump Distance Along E	S1						
Corner to First Bump Distance Along D	S2						

**Table 15-4. Intel® Stacked CSP Package Attributes**

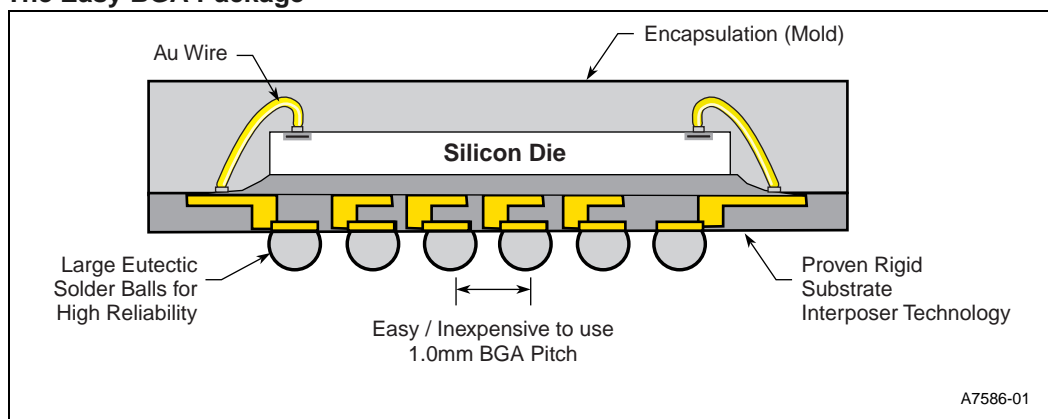
Intel® Stacked CSP Product Name	Square/ Rect.	Package Weight (mg)	Matrix (active)	D Nom	E Nom	S1	S2	SDC's <sup>2</sup>
RD28F1602C3	R	1803	8x8	10.00	8.00	1.20	.60	Y
RD28F1604C3	R	TBD	8x8	12.00	8.00	1.20	1.60	
RD28F3202C3	R	2316	8x8	12.00	8.00	1.20	1.60	
RD28F3204C3	R	2278	8x8	12.00	8.00	1.20	1.60	
Shipping media	All µBGA products are available in Tape & Reel or Trays							
Desiccant Pack <sup>1</sup>	All µBGA products are IPC Level 2							
1. Desiccant Pack levels relate to IPC Moisture Sensitivity Levels 2. SDC's represent the mechanical samples available in the various package size/type equivalents <b>NOTE:</b> All Dimensions in mm								

## 15.2.5 The Easy BGA Package

The Easy BGA package (fig 3.5) was designed to be the flash memory package of choice for embedded applications. While offering a larger ball pitch as compared to other CSPs, the Easy BGA package maintains the size benefits, measuring about  $\frac{3}{4}$  the size of its TSOP equivalent package.

Another advantage of the Easy BGA package is its constant package size/footprint in respect to memory density upgrades and die shrinks. A key element of embedded applications is the need for long product life cycles (5-7 years) that require the same package size/footprint. Not only does the package size/footprint need to stay constant over time; it does not change as a result of memory density upgrades or die process shrinks. This attribute is very beneficial because many embedded applications increase in memory density over time in order to incorporate additional functionality.

**Figure 15-6. The Easy BGA Package**

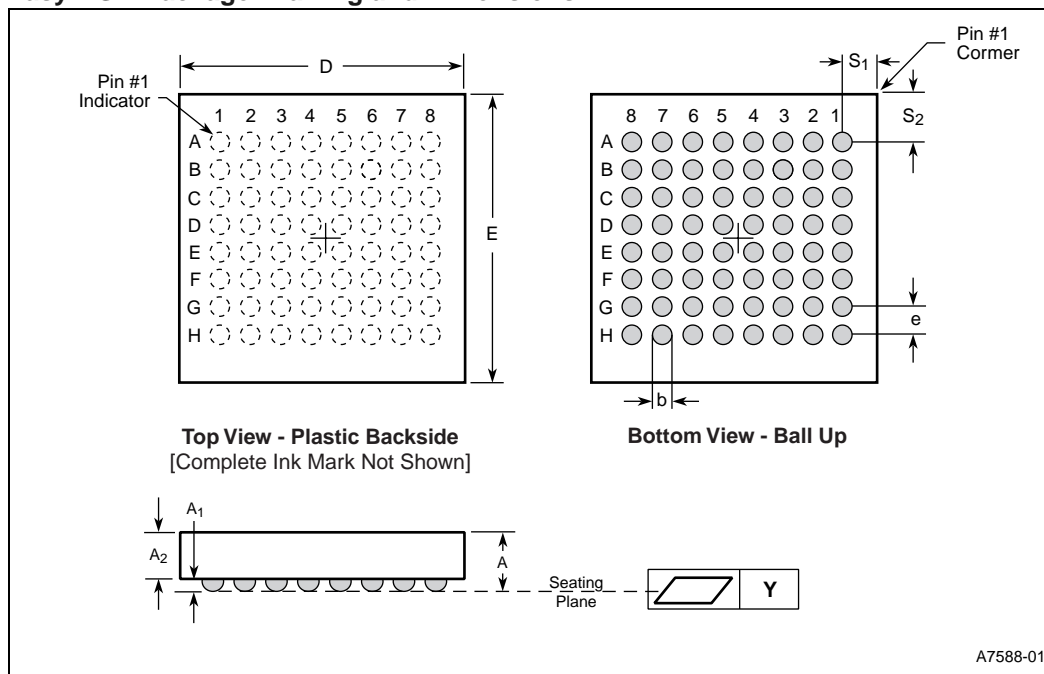


Many embedded applications require a high level of reliability due to the usage conditions of their environments. The Easy BGA package has been constructed specifically to address these types of requirements. The Easy BGA package construction incorporates many key features that

differentiate it from other CSP packages. Besides the wider ball pitch as previously discussed, the Easy BGA uses large diameter eutectic solder balls and a thick BT laminate rigid substrate. The combination of large solder balls and thick BT laminate substrate provide very good reliability by buffering and maximizing the separation between the silicon die and PCB surface to minimize the affects of CTE induced stresses.

## 15.2.6 Easy BGA Package Drawing and Dimensions

Figure 15-7. Easy BGA Package Drawing and Dimensions





**Table 15-5. Easy BGA Package Dimensions (all products)**

Symbol		Millimeters				Inches		
		Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.200				0.0472
Ball Height	A1	0.250				0.0098		
Package Body Thickness	A2	0.715	0.780	0.845		0.0281	0.0307	0.0333
Ball (Lead) Width	b	0.330	0.430	0.530		0.0130	0.0169	0.0209
Package Body Width	D	9.900	10.000	10.100		0.3898	0.3937	0.3976
Package Body Length	E	12.900	13.000	13.100		0.5079	0.5118	0.5157
Pitch	[e]		1.000				0.0394	
Ball (Lead) Count	N		64				64	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to First Ball Along D	S1	1.400	1.500	1.600		0.0551	0.0591	0.0630
Corner to First Ball Along E	S2	2.900	3.000	3.100		0.1142	0.1181	0.1220

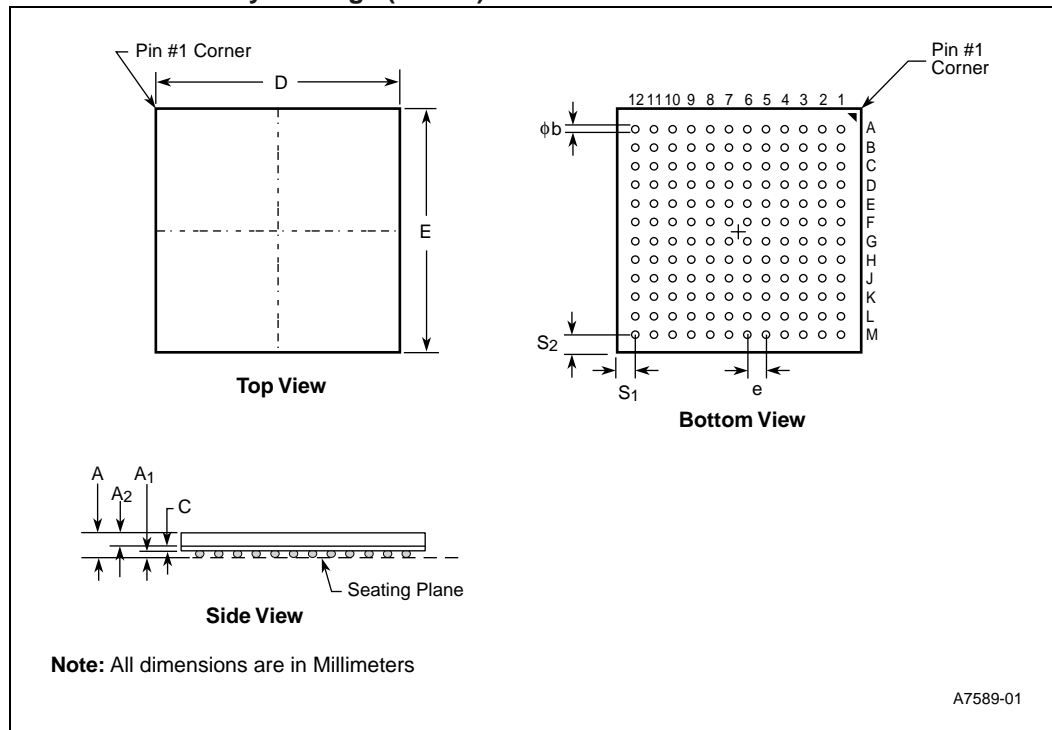
**Table 15-6. Easy BGA Package Attributes Table**

Easy BGA Product Name	Square/Rect.	package Weight	Matrix	SDC's <sup>2</sup>
RC28F800F3	R	213.8	8x8	
RC28F160F3	R	230.6	8x8	Y
RC28F800C3	R	198.9	8x8	
RC28F160C3	R	206.5	8x8	
RC28F320C3	R	214.5	8x8	
RC28F320J3	R	207.9	8x8	
RC28F640J3	R	220.9	8x8	
RC28F128J3	R	241.8	8x8	
Shipping Media	All products available in Tape & Reel or Trays			
Desiccant Pack <sup>1</sup>	Refer to moisture barrier bag label for specific IPC level			
1. Desiccant Pack levels relate to IPC Moisture Sensitivity Levels. Refer to the handling section of this guide for the complete moisture level table. 2. SDC's represent the mechanical samples available in the various package size/type equivalents <b>NOTE:</b> All Dimensions in mm				

## 15.2.7 Molded Matrix Array Package (MMAP) Package Drawings & Dimensions

**Note:** Unlike other chip scale packages included in this chapter, the MMAP packages are not Intel® Flash Memory Products. Any additional information for MMAP packages will be released in the future.

**Figure 15-8. Molded Matrix Array Package (MMAP) 144/225/256 ball count**



**Table 15-7. 144/225 Ball MMAP BGA Package Dimensions**

	Symbol	Millimeters				Inches		
		Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A	1.17		1.40		0.0461		0.0551
Ball Height	A1	0.30		0.36		0.0118		0.0142
Package Body Thickness	A2	0.87	0.96	1.05		0.0343	0.0378	0.0413
Ball (Lead) Width	b	0.35	0.40	0.45		0.0138	0.0157	0.0177
Package Body Width	D	12.90	13.00	13.10	1	0.5079	0.5118	0.5157
Package Body Length	E	12.90	13.00	13.10	1	0.5079	0.5118	0.5157
Pitch	[e]		1.00				0.0394	

**Table 15-7. 144/225 Ball MMAP BGA Package Dimensions**

Ball (Lead) Count	N		144/225				144/225	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to First Ball Along D	S1	0.90	1.00	1.10	1	0.0354	0.0394	0.0433
Corner to First Ball Along E	S2	0.90	1.00	1.10	1	0.0354	0.0394	0.0433
<b>NOTES:</b> 1. The tolerances above indicate projected production accuracy. This product is in the design phase. The minimal, nominal, and maximum package body width and length are subject to change dependent on final die size. Actual die size could shift these values by $\pm 0.008$ inches for the 28F320J5 product. 2. Some ball locations may not be populated on some products. See the specific product signal list for complete details.								

**Table 15-8. 256 Ball MMAP Package Dimensions**

		Millimeters				Inches		
		Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A	1.35	1.45	1.55		0.0531	0.0571	0.0610
Ball Height	A1	0.35	0.40	0.45		0.0138	0.0157	0.0177
Package Body Thickness	A2	0.65	0.70	0.75		0.0256	0.0276	0.0295
Ball (Lead) Width	b	0.40	0.50	0.60		0.0157	0.0197	0.0236
Package Body Width	D	16.80	17.00	17.20	1	0.6614	0.6693	0.6772
Package Body Length	E	16.80	17.00	17.20	1	0.6614	0.6693	0.6772
Pitch	[e]	0.90	1.00	1.10		0.0354	0.0394	0.0433
Ball (Lead) Count	N		256		2		256	
Seating Plane Coplanarity	Y			0.15				0.0039
Corner to First Ball Along D	S1	0.90	1.00	1.10	1	0.0354	0.0394	0.0433
Corner to First Ball Along E	S2	0.90	1.00	1.10	1	0.0354	0.0394	0.0433
<b>NOTES:</b> 1. The tolerances above indicate projected production accuracy. This product is in the design phase. The minimal, nominal, and maximum package body width and length are subject to change dependent on final die size. Actual die size could shift these values by $\pm 0.008$ inches for the 28F320J5 product. 2. Some ball locations may not be populated on some products. See the specific product signal list for complete details.								

## 15.3 Package Materials

### 15.3.1 CSP Construction Material Sets

Table 2 provides a listing of the package construction material sets for CSP packages.

**Table 15-9. CSP Material Sets**

CSP Type	μBGA	Easy BGA	Intel® Stacked-CSP
Sq/rect	R	R	R
Ball Material	63/37 SnPb		
Encapsulation Material	Elastomer	Epoxy Mold Compound	
Die Attach Material	Elastomer	Epoxy	
Substrate Material	Polyimide Tape	BT Laminate	
Substrate Trace Material	(Cu) Copper		
Substrate Finish Material	(Au) Gold		
Bond Material	(Cu) Copper	(Au) Gold Wire	
Bond Method	Thermosonic Lead Bond	Wire Bond	

## 15.4 Package Usage

Intel provides a full range of CSPs for your specific application. Each application has its own set of packaging requirements that may vary from the smallest possible size, reliability, long-term footprint/size compatibility, unit cost, total cost, or ease of use. The CSP of choice will vary depending on which packaging requirements are most important to your application.

If your application requires the smallest possible package, the μBGA\* package and the Intel Æ Stacked-CSP are the best package choice for your design. For the smallest size and highest reliability, the μBGA package remains the best single-die CSP for your design. For applications that use flash and SRAM, the Intel Æ Stacked-CSP adds value by integrating Flash and SRAM and stacking both individual die into one package. This unique packaging approach provides the ultimate in size reduction by eliminating a component from the board. These CSP's were designed to meet the demands of handheld applications such as cellular phones, pagers, personal digital assistants (PDA) and Global Positioning Systems (GPS) units.

Other embedded applications such as networking, automotive, set-top boxes, tele/data communications, and measurement equipment products have different packaging requirements. While size is still an important factor in these applications, lowest total-cost (such as PCB manufacturing) and long term size/footprint compatibility are highly valued. The Easy BGA package is the package of choice for these types of applications. The Easy BGA package has a relaxed 1.0mm ball pitch that allows for easy PCB routing using conventional PCB technology. In addition, the large .45mm ball diameter size and rigid BT laminate substrate package design allows for excellent solder joint reliability over a wide temperature range. While offering a larger ball pitch as compared to other CSPs, the Easy BGA package maintains the size benefits, measuring about ¾ the size of its TSOP equivalent package.



### 15.4.1 Silicon Daisy Chain (SDC) Evaluation Units

Intel also offers evaluation units that have been internally shorted together (to the silicon) in a "daisy chain" pattern. This ensures that the package's I/O path is complete through the ball, substrate, lead beam or bond wire, silicon, and back down through a separate I/O path. These units can be useful for set-up/evaluation of manufacturing equipment.

## 15.5 Handling: Shipping Media

Intel® Stacked-CSP's are shipped in either tape and reel or in mid-temperature thin matrix trays that comply to JEDEC standards. All JEDEC standard trays have the same 'x' and 'y' dimensions and are easily stacked for storage and manufacturing. For tape and reel or tray dimensions and quantities, refer to Chapter 10, "Transport Media and Packing" of this manual.

## 15.6 Preconditioning And Moisture Sensitivity

With most surface mount components, if the units are allowed to absorb moisture beyond a certain point, package damage may occur during the reflow process. Chapter 8, "Moisture Sensitivity/Desiccant Packaging/Handling of PSMCs" provides an in-depth view of package preconditioning and moisture sensitivity requirements. Specific moisture classification levels are defined on the box label for each product

## 15.7 Designing Boards for CSPs

In most cases, CSPs use the same PCB design and assembly processes as BGA packages. For general background information on these subjects, refer to chapter 14 which covers these similar processes for PBGA packages. Any CSP specific variations are listed below.

For additional detailed information about Intel® Flash memory CSPs, refer to the Intel Flash Memory CSP Users Guide located on the web at:

<http://developer.intel.com/design/flash/packtech/index.htm>

You will find extensive information on Intel® Flash memory CSPs covering a wide variety in topics such as:

- CSP assembly flow diagrams
- CSP package attributes
- CSP Materials, and packaging dimensions
- CSP shipping media and handling
- Printed Circuit Board (PCB) design considerations (trace/space, via, etc.)
- CSP to PCB assembly and manufacturing process recommendations
- CSP manufacturing support tools
- Intel's quality criteria
- CSP solutions for diverse applications

- CSP on-board programming
- CSP rework
- PCB surface tension and self centering of CSPs
- PCB solder stencils and process refinements
- PCB surface finishes

**Table 15-10. PCB Design Guidelines for .75mm mbga, Easy BGA, and Intel® Stacked-CSP**

Feature	.75mm $\mu$ BGA CSP	.8mm Stacked CSP	1.0mm Easy BGA
Land Pad Size	.30 (0.12)	.30 (0.12)	.30 (0.12)
Solder Mask Opening	.431 (.018)	.431 (.018)	.431 (.018)
Metal to Mask Clearance (Min)	.050 (.002)	.050 (.002)	.050 (.002)
Max Trace Width	.127 (.005)	.127 (.005)	.233 (.009)
Typical Spaces	.160 (.00625)	.187 (.0073)	.233 (.009)
Max Via Capture Pad	.51 (.020)	.51 (.020)	.711 (.028)
Max Via Drill Size	.25 (.010)	.25 (.010)	.457 (.018)
<b>NOTE:</b> All Dimensions in mm (inches)			

**Table 15-11. PCB Design Guidelines for .5mm pitch  $\mu$ BGA**

Feature	.5mm $\mu$ BGA* CSP
Land Pad Size	.279 (.011)
Solder Mask Opening	.356 (.014)
Typical Trace Width	.1016 (.004)
Reduce Trace Width Between Land Pads	.0737 (.0029)
Typical Micro Via (Via-in-Pad) Size	.1016 (.004)
<b>NOTE:</b> All Dimensions in mm (inches)	

**Table 15-12. Solder Stencil Design for  $\mu$ BGA, Easy BGA, and Intel® Stacked-CSP**

Feature	.5mm mBGA* CSP	.75mm mBGA* CSP	.8mm Stacked CSP	1.0mm Easy BGA
Top of Stencil Aperture	.279 (.011)	.33 (.013)	.33 (.013)	.33 (.013)
Bottom of Stencil Aperture	.30 (.012)	.356 (.014)	.356 (.014)	.356 (.014)
Stencil Thickness	.127 (.005)	.127 (.005)	.127 (.005)	.127 (.005)
<b>NOTE:</b> All Dimensions in mm (inches)				



## 15.8 Package to Board Assembly

In most cases, CSPs use the same PCB design and assembly processes as PBGA packages. For general background information on these subjects, refer to chapter 14 which covers these similar processes for PBGA packages.

For additional detailed information about Intel ® Flash memory CSPs, refer to the Intel Flash Memory CSP Users Guide located on the web at:

<http://developer.intel.com/design/flash/packtech/index.htm>

## 15.9 Revision Summary

- Complete revision of chapter
- Added MMAP

