



QUICKSWITCH® PRODUCTS
HIGH-SPEED CMOS
QUICKSWITCH
QUAD 2:1 MUX/DEMUX

IDTQS3257

FEATURES:

- Enhanced N channel FET with no inherent diode to Vcc
- 5Ω bidirectional switches connect inputs to outputs
- Pin compatible with the 74F257, 74FCT257, and 74FCT257T
- Zero propagation delay, zero ground bounce
- Undershoot clamp diodes on all switch and control inputs
- TTL-compatible control inputs
- Available in SOIC, QSOP, and S1 packages

APPLICATIONS:

- Logic replacement
- Video, audio, graphics switching, muxing
- Hot-swapping, hot-docking
- Voltage translation (5V to 3.3V)
- Bus funneling

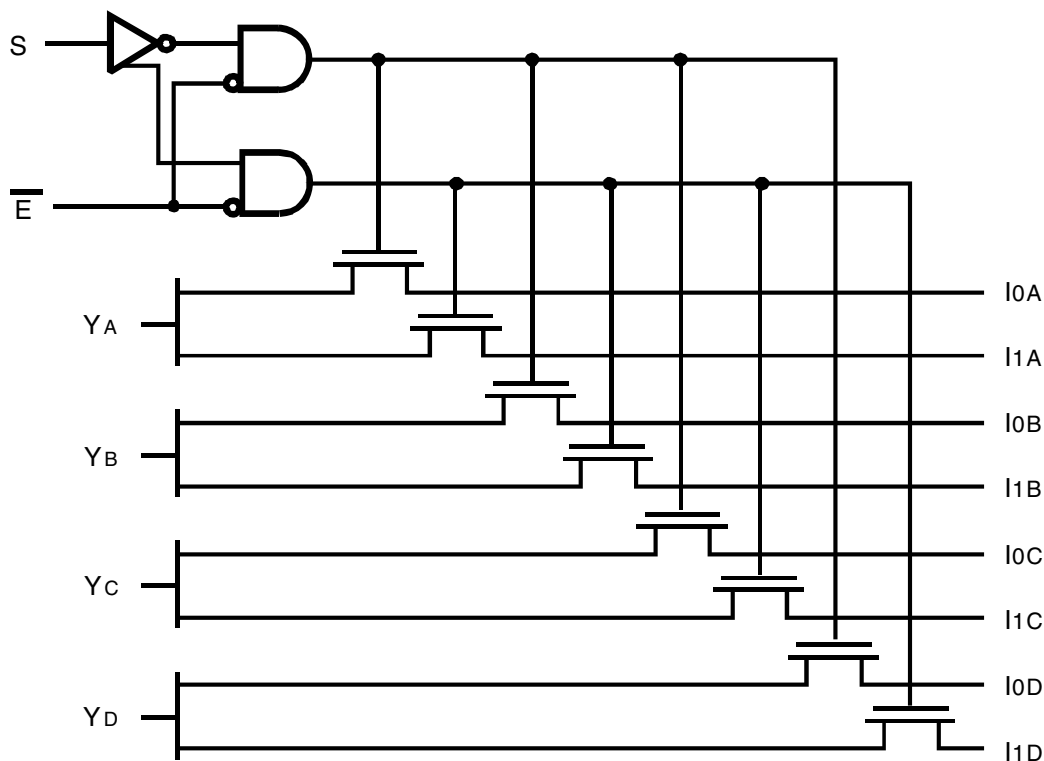
DESCRIPTION:

The QS3257 is a high-speed CMOS LVTTTL-compatible Quad 2:1 multiplexer/demultiplexer. The QS3257 is a function and pinout compatible QuickSwitch version of the 74F257, 74FCT257, and the 74ALS/AS/LS257 Quad 2:1 multiplexers. The low ON resistance of the QS3257 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise.

Mux/Demux devices provide an order of magnitude faster speed than equivalent logic devices.

The QS3257 is characterized for operation at -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

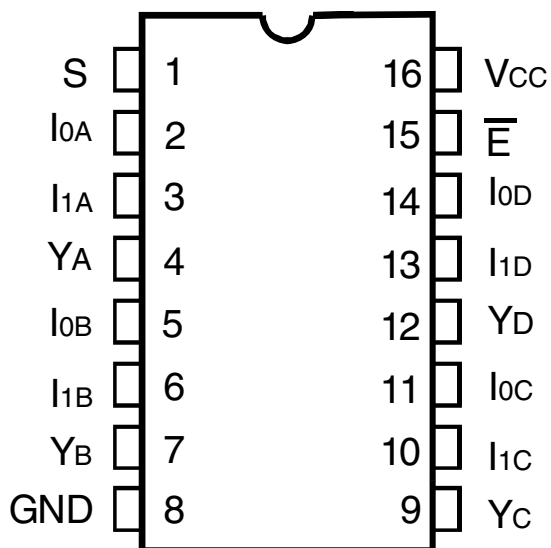


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INDUSTRIAL TEMPERATURE RANGE

FEBRUARY 2001

PIN CONFIGURATION



SOIC/ QSOP/ S1
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Supply Voltage to Ground	-0.5 to +7	V
VTERM ⁽³⁾	DC Switch Voltage Vs	-0.5 to +7	V
VTERM ⁽³⁾	DC Input Voltage VIN	-0.5 to +7	V
VAC	AC Input Voltage (pulse width ≤ 20ns)	-3	V
IOUT	DC Output Current	120	mA
PMAX	Maximum Power Dissipation (TA = 85°C)	0.5	W
TSTG	Storage Temperature	-65 to +150	°C

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- All terminals except VCC.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, VIN = 0V, VOUT = 0V)

Pins	Typ.	Max. ⁽¹⁾	Unit
Control Pins	4	5	pF
Quickswitch Channels (Switch OFF)	Demux	5	pF
	Mux	8	

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	I/O	Description
Ixx	I	Data Inputs
S	I	Select Input
E	I	Enable Input
YA - YD	O	Data Outputs

FUNCTION TABLE⁽¹⁾

Enable		Outputs				Function
E	S	YA	YB	YC	YD	
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disconnected
L	L	I0A	I0B	I0C	I0D	Select 0
L	H	I1A	I1B	I1C	I1D	Select 1

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

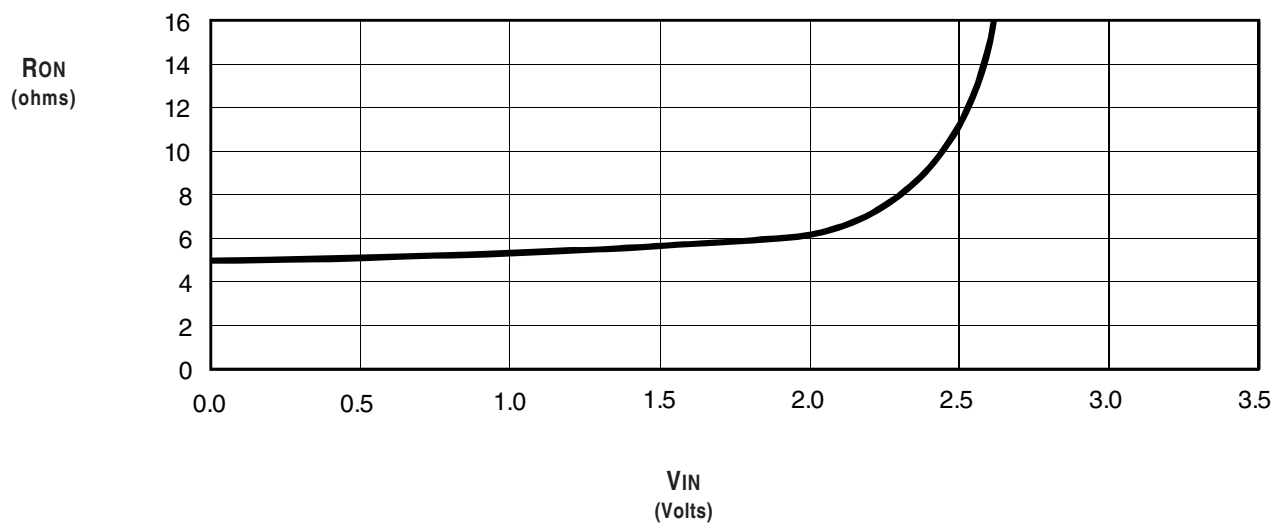
Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH for Control Pins	2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
I_{IN}	Input Leakage Current (Control Inputs) ⁽²⁾	$0\text{V} \leq V_{IN} \leq V_{CC}$	—	—	± 1	μA
I_{OZ}	Off-State Output Current (Hi-Z)	$0\text{V} \leq V_{OUT} \leq V_{CC}$	—	—	± 1	μA
R_{ON}	Switch ON Resistance	$V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 30\text{mA}$	—	5	7	Ω
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{mA}$	—	10	15	
V_P	Pass Voltage ⁽²⁾	$V_{IN} = V_{CC} = 5\text{V}, I_{OUT} = -5\mu\text{A}$	3.7	4	4.2	V

NOTES:

1. Typical values are at $V_{CC} = 5.0\text{V}$, $T_A = 25^{\circ}\text{C}$.

2. Pass Voltage is guaranteed but not production tested.

TYPICAL ON RESISTANCE vs V_{IN} AT $V_{CC} = 5\text{V}$



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Max.	Unit
I _{CCQ}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC} , f = 0	3	μA
ΔI _{CC}	Power Supply Current per Control Input HIGH ⁽²⁾	V _{CC} = Max., V _{IN} = 3.4V, f = 0	1.5	mA
I _{CCD}	Dynamic Power Supply Current per MHz ⁽³⁾	V _{CC} = Max., I and Y pins open Control Inputs Toggling at 50% Duty Cycle	0.25	mA/MHz

NOTES:

- For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
- Per TLL driven input (V_{IN} = 3.4V, control inputs only). I and Y pins do not contribute to ΔI_{CC}.
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The I and Y inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%;

C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Parameter	Min. ⁽¹⁾	Typ.	Max.	Unit
t _{PLH} t _{PHL}	Data Propagation Delay ^(2,3) I _x to Y	—	—	0.25 ⁽³⁾	ns
t _{PZH} t _{PZL}	Switch Turn-on Delay S _x to Y	0.5	—	5.2	ns
t _{PZH} t _{PZL}	Switch Turn-on Delay $\overline{E}x$ to Y	0.5	—	4.8	ns
t _{PHZ} t _{PLZ}	Switch Turn-off Delay ⁽²⁾ $\overline{E}x$ to Y, S _x to Y	0.5	—	5	ns

NOTES:

- Minimums are guaranteed but not production tested.
- This parameter is guaranteed but not production tested.
- The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

ORDERING INFORMATION

IDTQS	XXXXX	XX		
	Device Type	Package		
			SO	Small Outline IC
			Q	Quarter Size Outline Package
			QG	QSOP - Green
			S1	Small Outline IC
			S1G	SOIC - Green
			3257	High Speed CMOS Quickswitch Quad 2:1 Mux/Demux



CORPORATE HEADQUARTERS
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REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
62247	02	ADD 8 LD	07/10/99	T. VU
	03	ADDED TOPMARK TO TITLE	05/23/01	PKP
	04	CORRECTED X DIM	09/05/02	PKP
	05	ADD "GREEN" DCG NOMENCLATURE	10/12/04	TU VU

LAND PATTERN DIMENSIONS

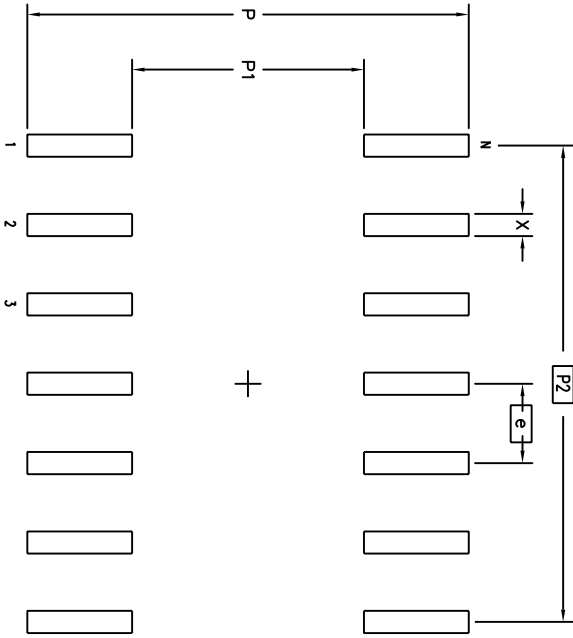
SYMBOL	JEDEC VARIATION			NOMINAL	TYPICAL	E
	AA					
	MIN	NOM	MAX			
A	.053	.064	.068			
A1	.004	.006	.010			
A2	.055	.058	.061	11		
D	.189	.194	.197	4.5		
E	.230	.236	.244	3		
E1	.150	.155	.157	4.6		
N	8					

	JEDEC VARIATION			NOMINAL	TYPICAL	E
	AB					
	MIN	NOM	MAX			
A	.053	.064	.068			
A1	.004	.006	.010			
A2	.055	.058	.061	11		
D	.337	.342	.344	4.5		
E	.230	.236	.244	3		
E1	.150	.155	.157	4.6		
N	14					

	JEDEC VARIATION			NOMINAL	TYPICAL	E
	AC					
	MIN	NOM	MAX			
A	.053	.064	.068			
A1	.004	.006	.010			
A2	.055	.058	.061	11		
D	.386	.391	.393	4.5		
E	.230	.236	.244	3		
E1	.150	.155	.157	4.6		
N	16					

NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- 2 DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- 3 DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- 4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- 5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- 6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
- 7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- 8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- 9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- 10 ALL DIMENSIONS ARE IN INCHES
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-012, VARIATION AA, AB & AC



	MIN	MAX	MIN	MAX	MIN	MAX
P	.274	.282	.274	.282	.274	.282
P1	.142	.150	.142	.150	.142	.150
P2	.150 BSC	.300 BSC	.150 BSC	.300 BSC	.150 BSC	.300 BSC
X	.015	.024	.015	.024	.015	.024
e	.050 BSC	.050 BSC	.050 BSC	.050 BSC	.050 BSC	.050 BSC
N	8		14		16	

TOLERANCES UNLESS SPECIFIED		IDT		2975 Slender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674	
DECIMAL	ANGULAR	XXX	XXX	XXX	XXX
DATE	DATE	DATE	DATE	DATE	DATE
08/25/98	08/25/98	08/25/98	08/25/98	08/25/98	08/25/98
CHECKED	CHECKED	CHECKED	CHECKED	CHECKED	CHECKED
SIZE	SIZE	SIZE	SIZE	SIZE	SIZE
C	C	C	C	C	C
PSC-4068	PSC-4068	PSC-4068	PSC-4068	PSC-4068	PSC-4068
REV	REV	REV	REV	REV	REV
05	05	05	05	05	05
DO NOT SCALE DRAWING	DO NOT SCALE DRAWING	DO NOT SCALE DRAWING	DO NOT SCALE DRAWING	DO NOT SCALE DRAWING	DO NOT SCALE DRAWING
SHEET 2 OF 2	SHEET 2 OF 2	SHEET 2 OF 2	SHEET 2 OF 2	SHEET 2 OF 2	SHEET 2 OF 2