



Integrated Device Technology, Inc.

FAST CMOS BUFFER/CLOCK DRIVER

IDT49FCT3805/A

FEATURES:

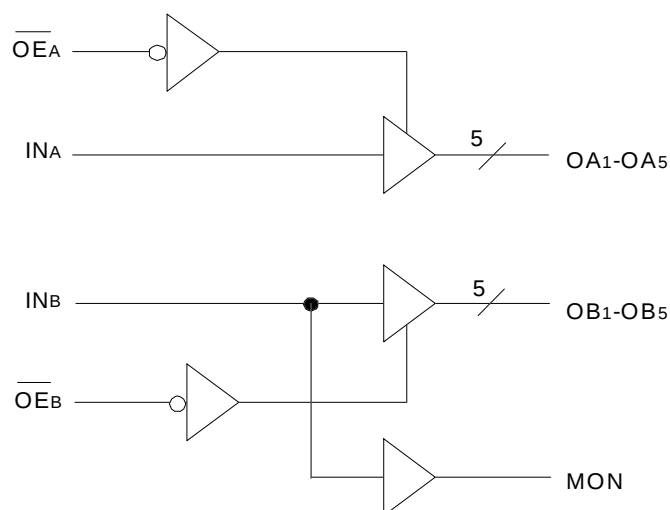
- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 500ps (max.)
- Very low duty cycle distortion < 1.0ns (max.)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- Inputs can be driven from 3.3V or 5V components
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- 'Heartbeat' monitor output
- Available in SOIC, SSOP, QSOP packages
- $V_{CC} = 3.3V \pm 0.3V$

DESCRIPTION:

The FCT3805/A is a 3.3 volt, non-inverting clock driver built using advanced dual metal CMOS technology. The device consists of two banks of drivers, each with a 1:5 fanout and its own output enable control. The device has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The FCT3805/A offers low capacitance inputs with hysteresis.

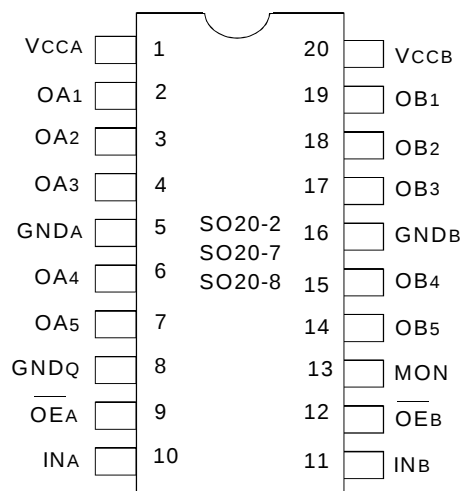
The FCT3805/A is designed for high speed clock distribution where signal quality and skew are critical. The FCT3805 also allows single point-to-point transmission line driving in applications such as address distribution, where one signal must be distributed to multiple receivers with low skew and high signal quality.

FUNCTIONAL BLOCK DIAGRAM



3102 drw 01

PIN CONFIGURATION



SOIC/SSOP/QSOP
TOP VIEW

3102 drw 02

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COMMERCIAL / INDUSTRIAL TEMPERATURE RANGE

OCTOBER 1998

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A, \overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_n, OB_n	Clock Outputs
MON	Monitor Output

3102 tbl 01

FUNCTION TABLE⁽¹⁾

Inputs		Outputs	
$\overline{OE}_A, \overline{OE}_B$	IN_A, IN_B	OA_n, OB_n	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

3102 tbl 02

NOTE:

- H = HIGH
L = LOW
Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to +7	V
$V_{TERM}^{(4)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	-60 to +60	mA

3102 lmk 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- Input terminals.
- Output and I/O terminals.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
$C_{I/O}$	I/O Capacitance	$V_{OUT} = 0V$	5.5	8	pF

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NOTE:

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2	—	5.5	V
	Input HIGH Level (I/O pins)			2	—	$V_{CC} + 0.5$	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = 5.5\text{V}$	—	—	± 1	μA
	Input HIGH Current (I/O pins)		$V_I = V_{CC}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins)		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins)		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		-36	-60	-110	mA
I_{ODL}	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		50	90	200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	—	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8\text{mA}$	$2.4^{(5)}$	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 0.1\text{mA}$	—	—	0.2	V
			$I_{OL} = 16\text{mA}$	—	0.2	0.4	
			$I_{OL} = 24\text{mA}$	—	0.3	0.50	
I_{OFF}	Input Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN} = 4.5\text{V}$		—	—	± 1	μA
I_{OS}	Short Circuit Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-135	-240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.},$ $V_{IN} = \text{GND or } V_{CC}$		—	0.1	10	μA

NOTES:

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1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. $V_{OH} = V_{CC} - 0.6\text{V}$ at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = V _{CC} -0.6V ⁽³⁾		—	2	30	μA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Per Output Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	0.035	0.06	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _o = 25MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = V_{CC}$ Mon. Output Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	0.9	1.6	mA
			V _{IN} = V _{CC} -0.6V V _{IN} = GND	—	0.9	1.6	
		V _{CC} = Max. Outputs Open f _o = 50MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Eleven Outputs Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	20	33 ⁽⁵⁾	
			V _{IN} = V _{CC} -0.6V V _{IN} = GND	—	20	33 ⁽⁵⁾	

NOTES:

3102 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input (V_{IN} = V_{CC} -0.6V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_o)$
I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} -0.6V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_o = Output Frequency
N_o = Number of Outputs at f_o
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL^(3,4)

Symbol	Parameter	Condition ⁽¹⁾	FCT3805		FCT3805A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay IN _A to OA _n , IN _B to OB _n	C _L = 50pF R _L = 500Ω	1.5	5.8	1.5	5	ns
t _R	Output Rise Time		—	2	—	2	ns
t _F	Output Fall Time		—	2	—	2	ns
tsk(o)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.5	—	0.5	ns
tsk(p)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})		—	1	—	1	ns
tsk(t)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.5	—	1.2	ns
t _{PZL} t _{PZH}	Output Enable Time OE _A to OA _n , OE _B to OB _n		1.5	6.5	1.5	6	ns
t _{PLZ} t _{PHZ}	Output Disable Time OE _A to OA _n , OE _B to OB _n		1.5	5.5	1.5	5	ns

NOTES:

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1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, tsk(t) are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL^(3,4)

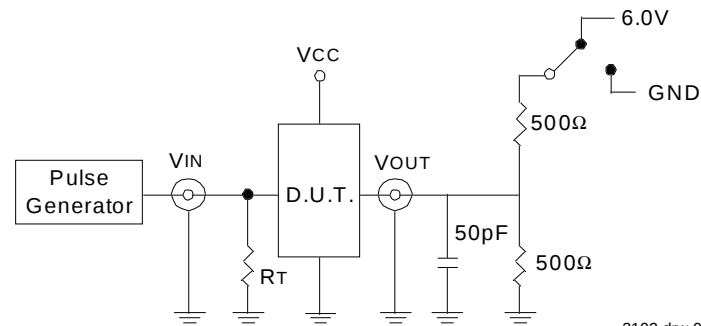
Symbol	Parameter	Condition ⁽¹⁾	FCT3805		FCT3805A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay IN _A to OA _n , IN _B to OB _n	C _L = 50pF R _L = 500Ω	1.5	5.8	1.5	5.2	ns
t _R	Output Rise Time		—	2	—	2	ns
t _F	Output Fall Time		—	2	—	2	ns
tsk(o)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.6	—	0.6	ns
tsk(p)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})		—	1	—	1	ns
tsk(t)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.5	—	1.2	ns
t _{PZL} t _{PZH}	Output Enable Time OE _A to OA _n , OE _B to OB _n		1.5	6.5	1.5	6	ns
t _{PLZ} t _{PHZ}	Output Disable Time OE _A to OA _n , OE _B to OB _n		1.5	5.5	1.5	5	ns

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, tsk(t) are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3102 drw 03

ENABLE AND DISABLE TIME

SWITCH POSITION

Test	Switch
Disable LOW Enable LOW	6.0V
Disable HIGH Enable HIGH	GND

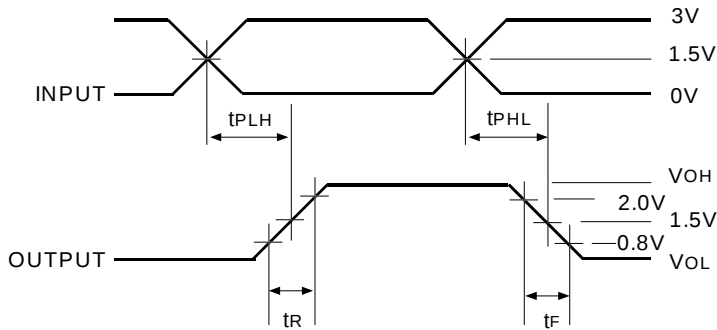
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

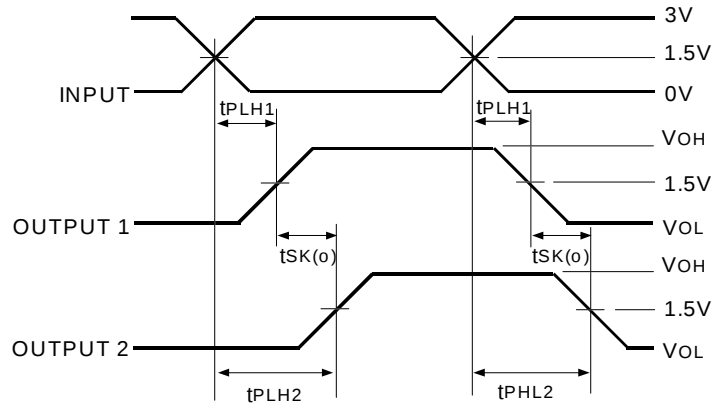
3102 Ink 08

PACKAGE DELAY



3102 drw 04

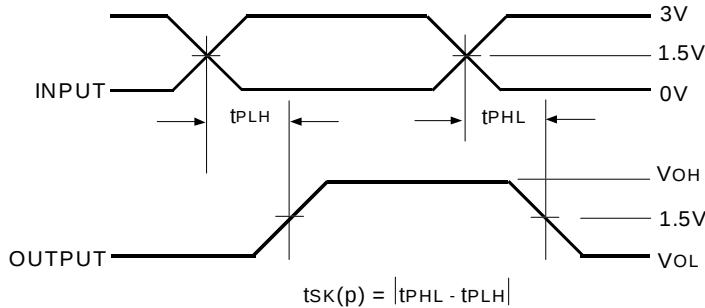
OUTPUT SKEW - $t_{SK}(o)$



$$t_{SK}(o) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

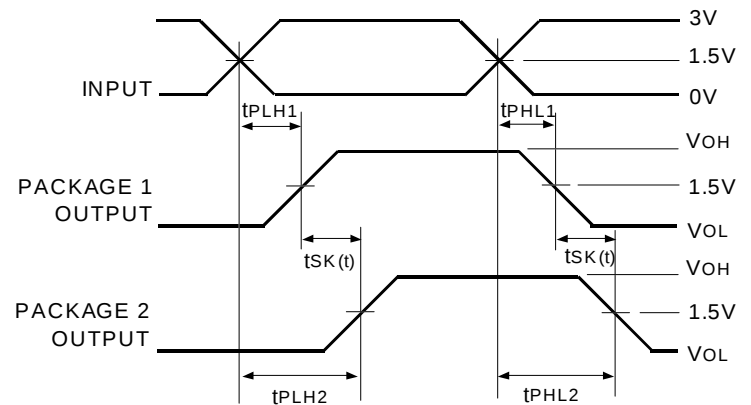
3102 drw 07

PULSE SKEW - $t_{SK}(p)$



3102 drw 05

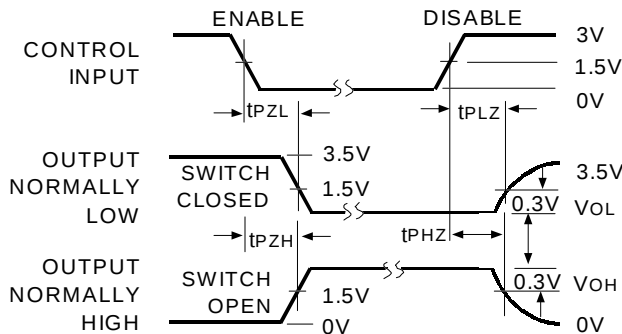
PACKAGE SKEW - $t_{SK}(t)$



$$t_{SK}(t) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

3102 drw 08

OUTPUT SKEW - $t_{SK}(x)$



3102 drw 06

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: $f \leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$

ORDERING INFORMATION

IDT49FCT	XXXX	X	X		
	Device Type	Package	Temp. Range		
				Blank	Commercial (0°C to +70°C)
				I	Industrial (-40°C to +85°C)
				SO	Small Outline IC (SO20-2)
				PY	Shrink Small Outline IC (SO20-7)
				Q	Quarter-size Small Outline Package (SO20-8)
				3805	Non-Inverting 3.3V Buffer/Clock Driver
				3805A	

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