DEVICE
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INCORPORATED

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DEI1026
Six Channel Discrete-to-Digital Interface Sensing Open/Ground Signals

Features:

- Senses six Open/Ground Inputs
- Inputs are lightning protected to DO-160D Level 3
- TTL/CMOS-Compatible Tri-State Outputs
- Package / Temperature Options:
  - 16 lead .150" SOIC, -55°C /+85°C
  - 16 lead Ceramic 300mil SOP, -55°C /+125°C
- 100% Final Testing

SOIC package option shown

Functional Description:

The DEI1026 is a six channel discrete-to-digital interface BiCMOS device. It senses six Open/Ground discrete signals of the type commonly found in avionic systems. The inverted 3-state outputs are TTL/CMOS compatible and are enabled by the $\overline{OE}$ and $\overline{CE}$ pins. The inputs are lightning protected to meet the requirements of DO160D Sec 22 Waveforms 3, 4, and 5, Level 3. See figures 5-7. The device is available in a 16 lead .150 SOIC and .300 Ceramic SOP.

With its reliability, low cost, operating range, and lightning protection, the DEI1026 meets a large variety of interface requirements for aerospace applications.

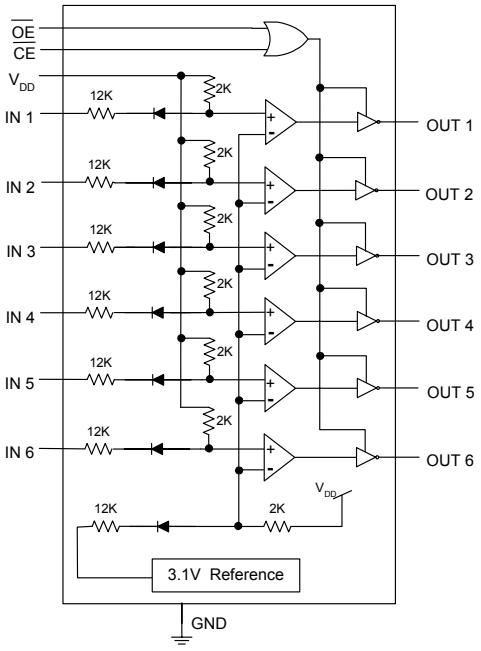


Figure 1: Concept Drawing

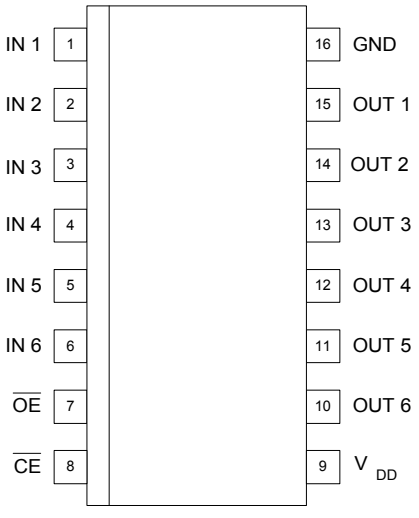


Figure 2: Pinout Diagram

DS-MP-01026 Rev. E
12/03/2002

Table 1: Absolute Maximum Ratings				
PARAMETER		**MIN**	**MAX**	**UNITS**
Supply Voltage V_{DD}		-0.3	7.0	V
Discrete Input Voltage (Pins 1-6)		-5	+40 *	V
Digital Input Voltage ($\overline{CE}$ and $\overline{OE}$)		V_{SS} - 0.3	V_{DD} + 0.3	V
Lightning Protection (Pins 1-6) DO160D, Waveform 3; Level 3 DO160D, Waveforms 4, and 5; Level 3		 -600 -300	 +600 +300	V
Storage Temperature	Plastic Ceramic	-55 -55	125 145	°C
Operating Free Air Temperature	Plastic Ceramic	-55 -55	85 125	°C
Lead Soldering Temperature (10 Seconds Max)		-	280	°C
Body Soldering Temperature (10 Seconds Max)		-	210	°C
The DEI1026 contains circuitry to protect inputs from damage due to electrostatic discharge. It has been characterized per JEDEC A114-A Human Body Model to Class 1. Observe precautions for handling and storing Electrostatic Sensitive Devices.				
* The DEI1026 will withstand the transient surge DC voltage step function loci limits for category B equipment per MIL-STD-704A.				

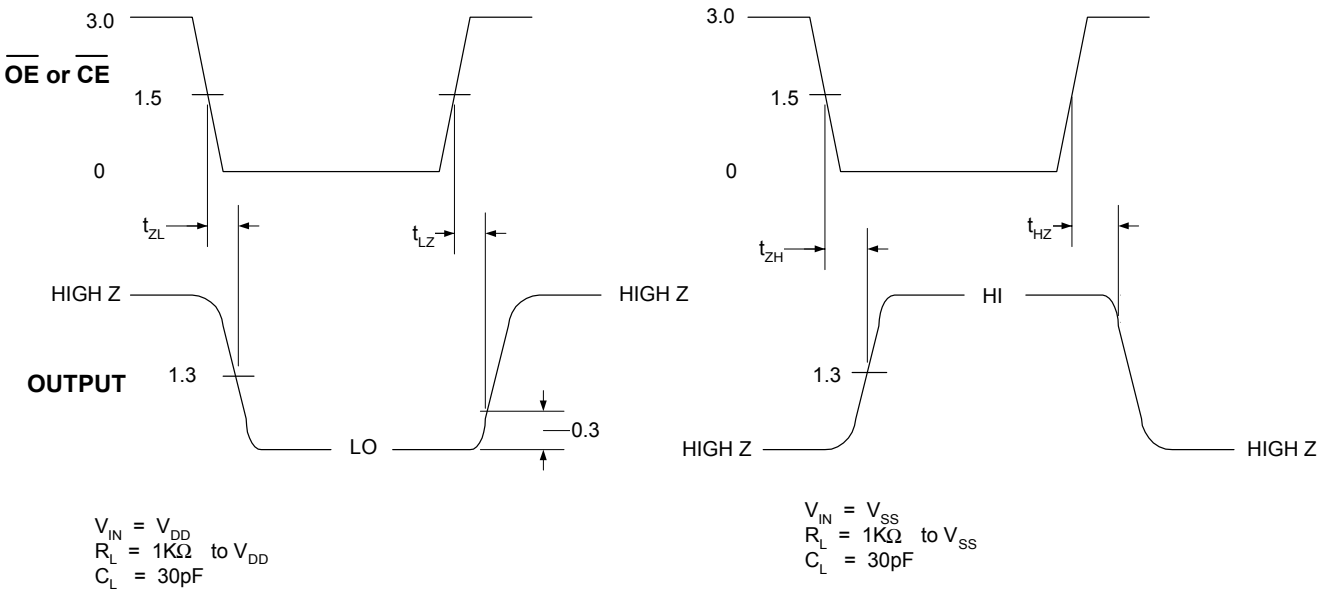
Table 2: DEI1026 Device Operating Characteristics						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Free Air Operating Temp.	T_A	V_{DD} = 4.5 – 5.5 V Plastic Ceramic	 -55 -55		 85 125	°C
Logic Output Sink Current	I_{OL}	V_{DD} = 4.5 – 5.5 V			5.0	mA
Logic Output Source Current	I_{OH}	V_{DD} = 4.5 – 5.5 V	-5.0			mA

Table 3: DEI1026 Logic Truth Table			
$\overline{CE}$ (Chip Enable)	**$\overline{OE}$ (Output Enable)**	**Discrete Input**	**Output**
0	0	Open	0
0	0	Ground	1
1	X	X	High Z
X	1	X	High Z

Table 4A: DEI1026 (Plastic) Electrical Characteristics (T_A = -55°C TO +85°C , V_{DD} = 4.5 TO 5.5 V, Unless otherwise noted)						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply and Thermal Data						
Supply Current	I_{DD}	V_{IN} = V_{DD} (all inputs) V_{DD} = 5.5 V		5	10	mA
Thermal Resistance	θ_{JA} θ_{JC}	Junction to Ambient (4 layer PCB) Junction to Case		74 24		°C/W
Max Junction Temperature	T_{Jmax}	Max. Junction Temperature			125	°C
Discrete Input Characteristics						
Ground state input voltage	V_{SG}	Voltage source from input terminal to ground for Logic High Output.			3.0	V
Open state input voltage	V_{SO}	Voltage source from input terminal to ground for Logic Low Output.	3.5			V
Ground state input resistor	R_{IG}	Resistor from input to ground to guarantee Logic High Output.	0		100	Ω
Open state input resistor	R_{IO}	Resistor from input to ground to guarantee Logic Low Output.	100k			Ω
Input source current	I_{IO}	Current sourced into 100 Ohm resistor to Ground.	-100	-330		µA
Reverse leakage current	I_{IR}	V_{IN} = 35 V, V_{DD} = 0 V			100	µA
Logic Input Characteristics						
$\overline{CE}$, $\overline{OE}$ input logic 1 level	V_{IH}		2.0			V
$\overline{CE}$, $\overline{OE}$ input logic 0 level	V_{IL}				0.8	V
DC Output Characteristics						
Output logic 1 level (TTL)	V_{OH}	I_{OH} = -5 mA.	2.4			V
Output logic 0 level (TTL)	V_{OL}	I_{OL} = 5 mA.			0.4	V
Output logic 1 level (CMOS)	V_{OH}	I_{OH} = -100 µA	V_{DD} – 50mV			V
Output logic 0 level (CMOS)	V_{OL}	I_{OL} = 100 µA			V_{SS} + 50mV	V
Off-state Output Current	I_{OZ}	$\overline{OE}$ = V_{DD} V_{DD} = 5.5 V V_{OUT} = 0 or V_{DD}			+/-10	µA
Switching Characteristics [1]						
I/O propagation delay	t_{HL}, t_{LH}	Refer to Figure 4.			150	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output low) to output HI-Z	t_{LZ}	Refer to Figure 3.			25	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output low	t_{ZL}	Refer to Figure 3.			25	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output high) to output HI -Z	t_{HZ}	Refer to Figure 3.			25	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output high	t_{ZH}	Refer to Figure 3.			25	ns

Table 4B: DEI1026-WM[ ] (Ceramic) Electrical Characteristics (T_A = -55°C TO +125°C, V_{DD} = 4.5 TO 5.5 V, Unless otherwise noted)						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply and Thermal Data						
Supply Current	I_{DD}	V_{IN} = V_{DD} (all inputs) V_{DD} = 5.5 V		5	10	mA
Thermal Resistance	θ_{JA} θ_{JC}	Junction to Ambient Junction to Case		tbd 23		°C/W
Max Junction Temperature	T_{Jmax}	Max. Junction Temperature			145	°C
Discrete Input Characteristics						
Ground state input voltage	V_{SG}	Voltage source from input terminal to ground for Logic High Output.			3.0	V
Open state input voltage	V_{SO}	Voltage source from input terminal to ground for Logic Low Output.	3.5			V
Ground state input resistor	R_{IG}	Resistor from input to ground to guarantee Logic High Output.	0		100	Ω
Open state input resistor	R_{IO}	Resistor from input to ground to guarantee Logic Low Output.	100k			Ω
Input source current	I_{IO}	Current sourced into 100 Ohm resistor to Ground.	-100	-330		µA
Reverse leakage current	I_{IR}	V_{IN} = 35 V, V_{DD} = 0 V			100	µA
Logic Input Characteristics						
$\overline{CE}$, $\overline{OE}$ input logic 1 level	V_{IH}		2.0			V
$\overline{CE}$, $\overline{OE}$ input logic 0 level	V_{IL}				0.8	V
DC Output Characteristics						
Output logic 1 level (TTL)	V_{OH}	I_{OH} = -5 mA.	2.4			V
Output logic 0 level (TTL)	V_{OL}	I_{OL} = 5 mA.			0.4	V
Output logic 1 level (CMOS)	V_{OH}	I_{OH} = -100 µA	V_{DD} – 50mV			V
Output logic 0 level (CMOS)	V_{OL}	I_{OL} = 100 µA			V_{SS} + 50mV	V
Off-state Output Current	I_{OZ}	$\overline{OE}$ = V_{DD} V_{DD} = 5.5 V V_{OUT} = 0 or V_{DD}			+/-10	µA
Switching Characteristics [1]						
I/O propagation delay	t_{HL}, t_{LH}	Refer to Figure 4.			170	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output low) to output HI-Z	t_{LZ}	Refer to Figure 3.			30	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output low	t_{ZL}	Refer to Figure 3.			30	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output high) to output HI -Z	t_{HZ}	Refer to Figure 3.			30	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output high	t_{ZH}	Refer to Figure 3.			30	ns

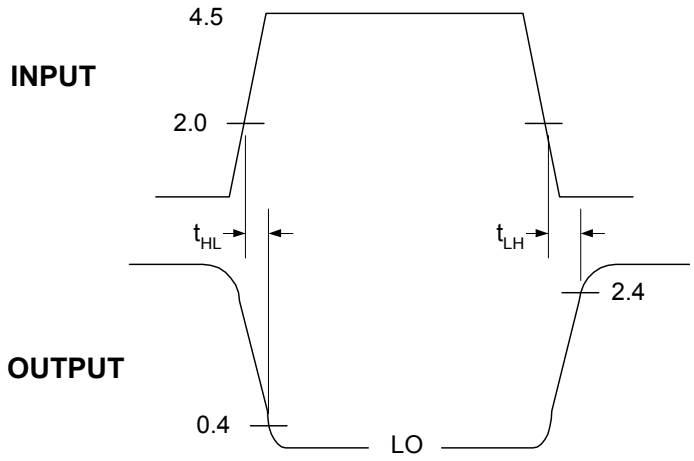
Notes:
1. Guaranteed by design and not production tested.



V_{IN} = V_{DD}
R_L = 1KΩ to V_{DD}
C_L = 30pF

V_{IN} = V_{SS}
R_L = 1KΩ to V_{SS}
C_L = 30pF

Figure 3: Enable to Output Propagation Delay



R_L = 1KΩ to V_{DD}
C_L = 30pF

Figure 4: Input to Output Propagation Delay

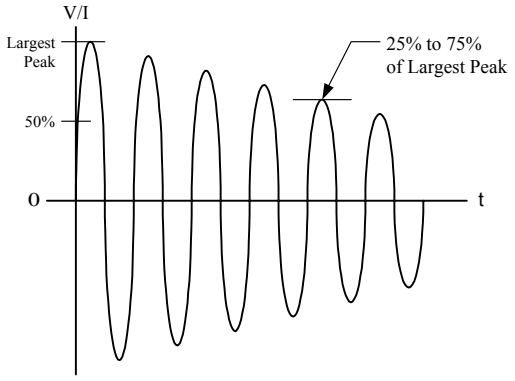


Figure 5: DO160D Voltage Waveform #3
V_{OC} = 600V, I_{SC} = 24A, Frequency = 1.0MHZ ±20%

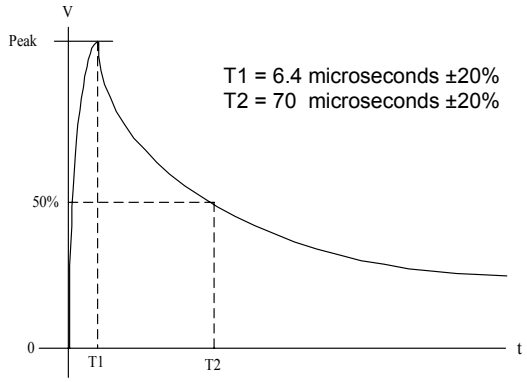


Figure 6: DO160D Voltage Waveform #4
V_{OC} = 300V, I_{SC} = 60A

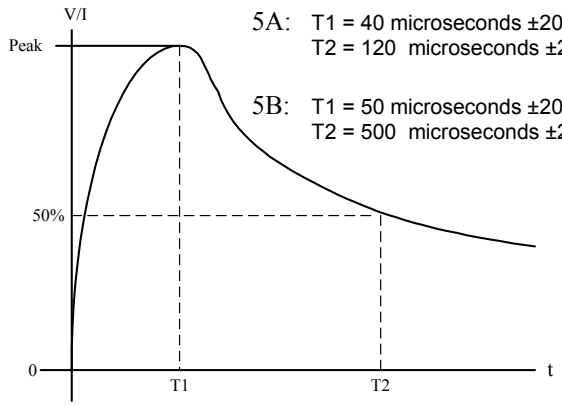


Figure 7: DO160D Voltage Waveform #5
V_{OC} = 300V, I_{SC} = 300A

Notes:
1. V_{OC} = Peak Open Circuit Voltage available at the calibration point.
2. I_{SC} = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%
4. The ratio of V_{OC} to I_{SC} is the generator source impedance to be used for generator calibration purposes.

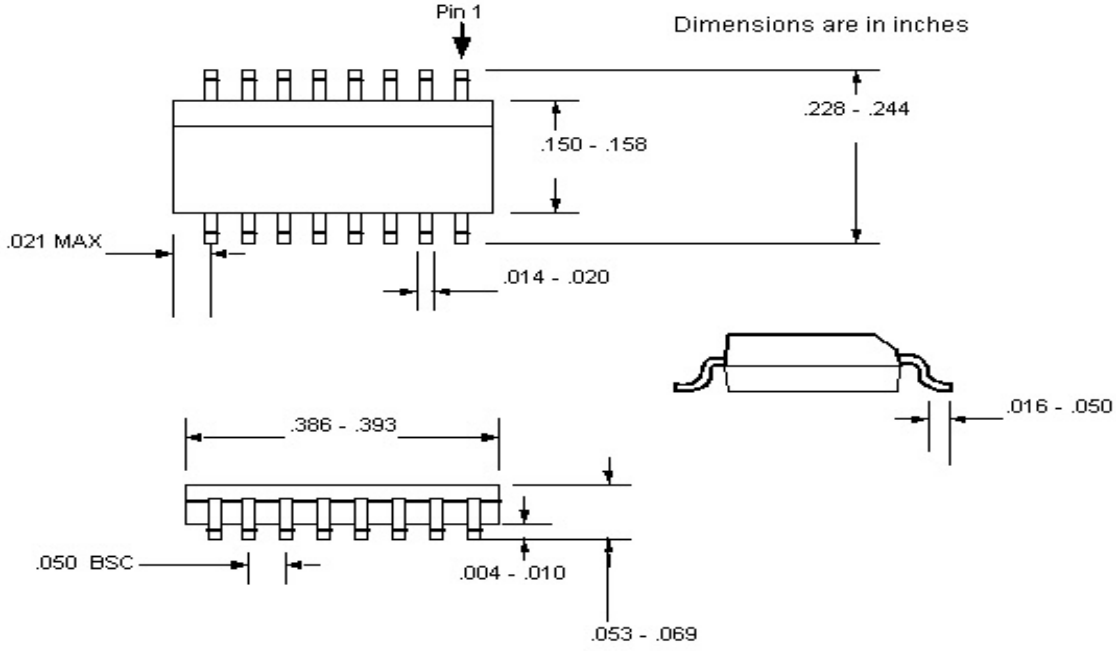


Figure 8: DEI1026 Mechanical Outline
16 lead 0.150" SOIC JEDEC MS-012-16

JEDEC Moisture Sensitive Rating: MSL 2

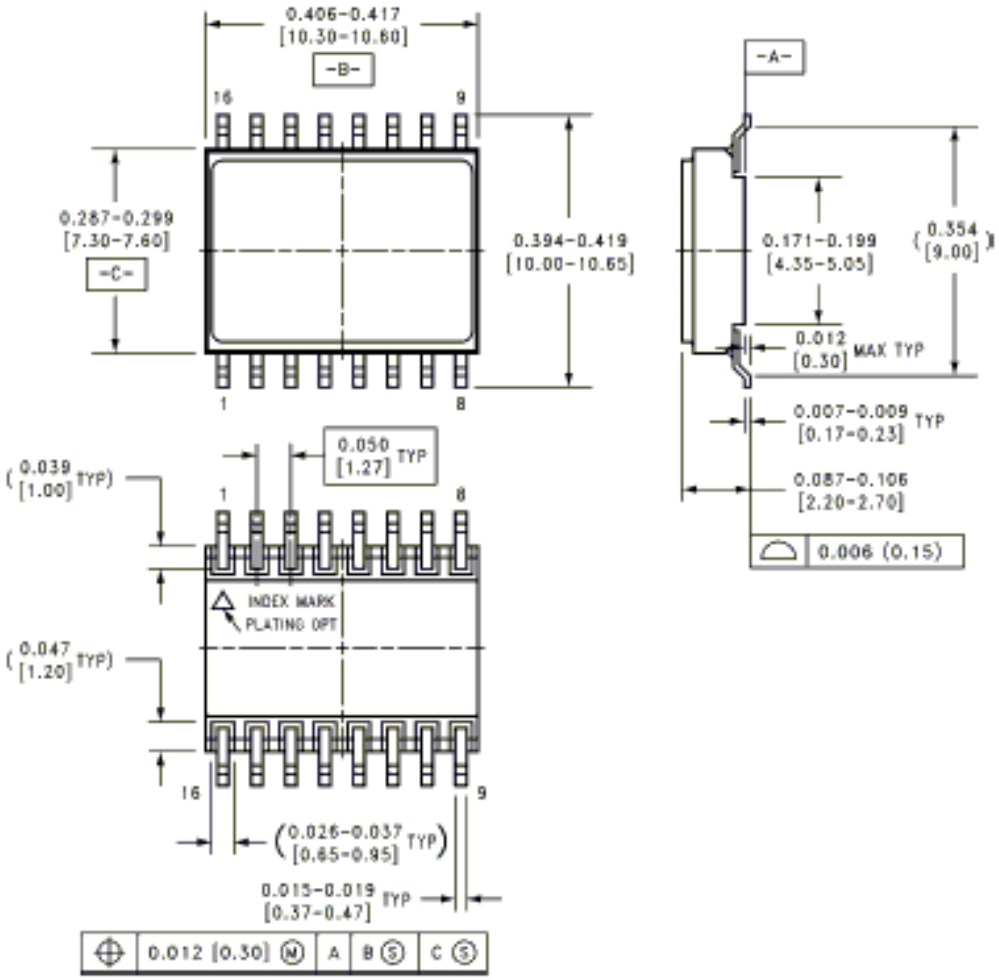


Figure 9: DEI1026-WM[ ] Mechanical Outline
16 lead Ceramic SOP

Table 5: Ordering Information

DEI PART NUMBER	PACKAGE	OP. TEMP. RANGE	PROCESSING
DEI1026	16 lead .150" SOIC	-55 / +85ºC	Standard
DEI1026-WMS	16 lead ceramic SOP	-55 / +125ºC	Standard
DEI1026-WMB	16 lead ceramic SOP	-55 / +125ºC	Burn In, 96 hr @125ºC

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