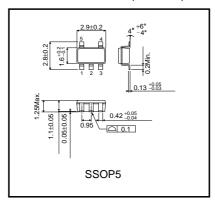
Single analog switch **BU4S66G2**

The BU4S66G2 is an ultra-compact IC with one circuit of the bi-directional analog switch BU4066B built into an SMP package. Setting the enable input (CONT) to the "H" level sets the impedance between the switch input and the output pins low (ON state) and setting CONT to the "L" level sets the impedance high (OFF state).

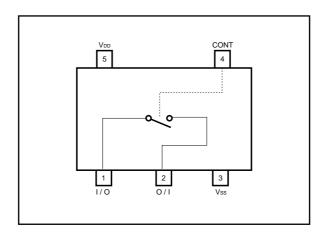
Features

- 1) Low current dissipation.
- 2) Super-mini mold package designed for surface mounting.
- 3) Wide range of operating power supply voltage.
- 4) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

●External dimensions (Unit : mm)



Block diagram



● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{DD}	Vss - 0.3 to Vss + 18	V
Power dissipation	Pd	540	mW
Input current	lin	± 10	mA
Operating temperature	Topr	- 40 to + 85	°C
Storage temperature	Tstg	- 55 to + 150	°C
Input voltage	Vin	Vss - 0.3 to $Vdd + 0.3$	V

^{\$1} These values indicate the range limits of the voltage that can be applied to each pin without destroying it. Operation is not guaranteed at these values.

*2 Reduced by 1.7mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta=25°C, Vss=0V)

Parameter	Symbol	Min.	Тур.	Max.	Unit
Power supply voltage	V _{DD}	3	_	16	V
Input voltage	Vin	0	_	V _{DD}	V

•Electrical characteristics

DC characteristics (unless otherwise noted, Vss = 0V, Ta = 25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	V _{DD} (V) Conditions		Measurement circuit	
Control input high level voltage	Vін	3.5	-	_	V	5			
		7.0	-	_	V	10	Current between input and output = 10µA	Fig.1	
		11.0	-	-	V	15			
		_	_	1.5	V	5			
Control input low level voltage	VIL	_	_	3.0	V	10	Current between input and output = 10µA		
vollago		_	_	4.0	V	15			
		_	290	950	Ω	5		Fig.2	
ON resistance	Ron	-	120	250	Ω	10	$0 \le V_{IN} \le V_{DD}$ RL= $10k\Omega$		
		_	85	160	Ω	15	TRE-TORSE		
OFF-channel			0.3	^	15	Vin = 15V, Vout = 0V			
leakage current	loff	_	_	-0.3	μΑ	15	VIN = 0V, VOUT = 15V	Fig.3	
		_	_	1.0		5		_	
Static current dissipation	IDD	_	_	2.0	μΑ	10	VIN = VDD or GND		
		_	_	4.0		15			
Input capacitance (control input)	Cc	-	8	_	pF	_	f = 1MHz	_	
Input capacitance (switch input)	Cs	-	10	_	pF	_	f = 1MHz	_	

•Switching characteristics (unless otherwise noted, VSS = 0V, Ta = 25°C)

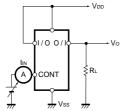
Parameter	Symbol	Min.	Тур.	Max.	Unit	V _{DD} (V)	Vss(V)	Conditions	Measuremen circuit
Propagation delay time (I / O→O / I)	tрын	_	15	-	ns	5		R _L = 10kΩ C _L = 50pF	- Fig.4
		-	8	-	ns	10	_		
		_	5	_	ns	15			
	t _{PHL}	-	15	-	ns	5		R _L = 10kΩ C _L = 50pF	
		_	8	_	ns	10	_		
		_	5	_	ns	15			
		_	100	_	ns	5		$R_L = 10k\Omega$ $C_L = 50pF$	Fig.5
	t PHZ	_	70	_	ns	10	-		
		_	65	-	ns	15			
	tplz	_	100	-	ns	5	_	R _L = 10kΩ C _L = 50pF	Fig.6
		_	70	-	ns	10			
Propagation delay time		_	65	-	ns	15			
(CONTROL→O / I)	tрzн	_	80	_	ns	5	_	R _L = 10kΩ C _L = 50pF	Fig.5
		-	35	-	ns	10			
		_	25	-	ns	15			
	t PZL	_	80	_	ns	5	_	R _L = 10kΩ C _L = 50pF	Fig.6
		_	35	_	ns	10			
		-	25	_	ns	15			
	f _{Max} .(C)	-	10	_	MHz	5	_	R _L = 1kΩ C _L = 50pF	-
Maximum control frequency		_	12	_	MHz	10			
		-	12	-	MHz	15			
Max. propagation frequency	f _{мах} . (I – О)* ¹	_	30	_	MHz	5	- 5	$R_L = 1k\Omega$ $C_L = 50pF$	_
Feedthrough attenuation	F.T.* ²	-	600	_	kHz	5	- 5	$R_L = 1k\Omega$ $R_L = 10k\Omega$ $C_L = 50pF$	Fig.7
Sinewave distortion (1kHz)	THD* ³	-	0.05	_	%	5	- 5		
		-	200	_	mV	5		$R_{\text{IN}} = 1k\Omega$ $R_{\text{OUT}} = 10k\Omega$ $C_{\text{L}} = 50\text{pF}$	
Crosstalk (CONTROL→O / I)	СТс	_	400	-	mV	10	_		Fig.8
		-	600	_	mV	15			

^{*1} Frequency that enables 20 log (Vout / VIN) = -3dB

^{*2} Frequency that enables 20 log (Vout / Vin) = -50 dB

^{*1 *2 *3} Use a $V_{IN} = \pm 2.5 V_{P-P}$ sine wave.

●Measurement circuits



 $V_{\text{IN}} = \frac{1}{2}V_{\text{DD}}$ $R_{\text{ON}} = 10\left(\frac{V_{\text{IN}}}{V_{\text{OUT}}} - 1\right)$ $R_{\text{L}} = 10k\Omega$

Fig. 1 Input voltage, current

Fig. 2 ON resistance

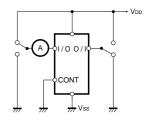
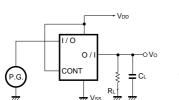


Fig. 3 Channel OFF leakage current



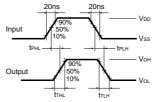


Fig. 4 Switching characteristic measurement circuit

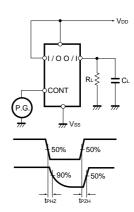


Fig. 5 Propagation delay time (CONT→ OUT)

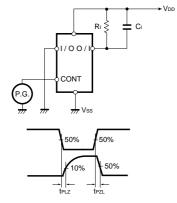


Fig. 6 Propagation delay time (CONT→OUT)

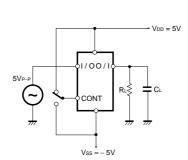


Fig. 7 Sine wave distortion, feedthrough attenuation

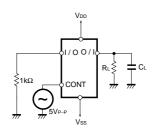


Fig. 8 Control IN \rightarrow OUT crosstalk

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