SILICON GATE CMOS

65,536 WORD x 16 BIT CMOS STATIC RAM

Description

The TC551664AJ is a 1,048,576 bits high speed static random access memory organized as 65,536 words by 16 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high

The TC551664AJ has low power feature with device control using Chip Enable (CE), and has Output Enable input (OE) for fast memory access. Also, it allows that lower and upper byte access by Data Byte Control (LB, UB). The TC551664AJ is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC551664AJ is packaged in a 44-pin SOJ with 400mil width for high density surface assembly.

Features

- Fast access time
 - TC551664AJ -15 15ns (max.)
 - TC551664AJ -20 20ns (max.)
- Low power dissipation

Cycle Time	15	20	25	30	50	ns
Operation (max.)	260	220	200	180	150	mA

- Standby: 1mA (max.)

- 5V single power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: OE
- LB (I/O1 ~ I/O8), UB (I/O9 ~ I/O16) • Data byte controls:
- SOJ44-P-400 • Package:

Pin Names

A0 ~ A15	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
CE	Chip Enable Input
WE	Write Enable Input
ŌĒ	Output Enable Input
LB, UB	Data Byte Control Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection
N.U.	Not Usable Input

Pin Connection (Top View)

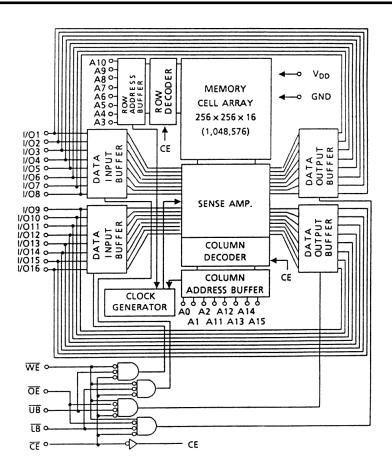
TC551664AJ				
A4	(TOP VIEW)	44 D A5 43 D A6 42 D A7 41 D OE 40 D UB 39 D LB 38 D I/O1 37 D I/O1 36 D I/O1 31 D I/O1 33 D I/O1 33 D I/O1 34 D GNU 33 D I/O1 34 D GNU 35 D I/O1 30	5 4 3 0 2 1 0 0 .	
(SOI	"		

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Block Diagram



Operating Mode

OPERATING MODE	CE	ŌĒ	WE	LB	ŪB	I/01 ~ I/08	I/09 ~ I/016	POWER
				L	L	Output	Output	I _{DDO}
Read	L	L	Н	Н	L	High Impedance	Output	I _{DDO}
				L	Н	Output	High Impedance	I _{DDO}
				L	L	Input	Input	I _{DDO}
Write	L	*	L	Н	L	High Impedance	Input	I _{DDO}
				L	Н	Input	High Impedance	I _{DDO}
Output Disable	L	Н	Н	*	*	High Impedance	High Impedance	I _{DDO}
Output Disable	L	*	*	Н	Н	Trigitimpedance	riigiriinpedance	I _{DDO}
Standby	Н	*	*	*	*	High Impedance	High Impedance	I _{DDS}

*H or L

Note:

N.U. pin must be kept open elctrically or pulled down to GND level or less than 0.8V. Applying a voltage more than 0.8V to N.U. pin is prohibited.

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Terminal Voltage	-2.0* ~ 7.0	V
V _{I/O}	Input/Output Terminal Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature (10s)	260	°C
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

^{*-3}V with a pulse width of 10ns

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DC Recommended Operating Conditions

SYMBOL	PARAMETER		TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	_	V _{DD} + 0.5	V
V _{IL}	Input Low Voltage	-0.5*	_	0.8	V

^{* -3}V with a pulse width of 10ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V \pm 10%)

SYMBOL	PARAMETER	TEST CONDITION			TYP.	MAX.	UNIT
ILI	Input Leakage Current (Except N.U. pin)	$V_{IN} = 0 \sim V_{DD}$			_	±10	μА
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH} \text{ or } \overline{WE} = V_{IL} \text{ or } \overline{OE} = V_{OUT} = 0 \sim V_{DD}$	V _{IH}	_	_	±10	μА
I _{I (N.U.)}	Input Current (N.U. pin)	$V_{IN} = 0 \sim 0.8V$		-1	ı	20	μΑ
I _{OH}	Output High Current	V _{OH} = 2.4V			_	_	mA
I _{OL}	Output Low Current	$V_{OL} = 0.4V$			_	_	mA
			t _{cycle} = 15ns	ı	-	260	
		OF V I O	t _{cycle} = 20ns	-	_	220	
I _{DDO}	Operating Current	$\overline{CE} = V_{IL}, I_{OUT} = 0mA,$ Other Inputs = V_{IH}/V_{II}	t _{cycle} = 25ns	-	_	200	mA
		Carrot in parts T _{[H} , T _]	t _{cycle} = 30ns	_	_	180	
		$t_{\text{cycle}} = 50 \text{ns}$		_	_	150	
I _{DDS1}	Standby Current	CE = V _{IH} , Other Inputs = V _{IH} /V _{IL}			_	30	mA
I _{DDS2}	Standby Current	$\overline{CE} = V_{DD} - 0.2V$, Other Inputs :	= V _{DD} - 0.2V or 0.2V	ı	_	1	IIIA

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	6	pF
C _{I/O}	Input/Output Capacitance	V _{I/O} = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

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AC Characteristics (Ta = 0 ~ 70° C⁽¹⁾, V_{DD} = $5V\pm10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55160	64AJ -15	TC551664AJ -20		UNIT
STWIDGE	FARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT
t _{RC}	Read Cycle Time	15	-	20	_	
t _{ACC}	Address Access Time	-	15	_	20	
t _{CO}	CE Access Time	_	15	_	20	
t _{OE}	OE Access Time	_	8	_	10	
t _{BA}	UB, LB Access Time	-	8	_	10	
t _{OH}	Output Data Hold Time from Address Change	5	-	5	_	ns
t _{COE}	Output Enable Time from CE	5	-	5	_	115
t _{OEE}	Output Enable Time from OE	1	-	1	_	
t _{BE}	Output Enable Time from UB, LB	1	_	1	_	
t _{COD}	Output Disable Time from CE	-	8	_	8	
t _{ODO}	Output Disable Time from OE	_	8	_	8]
t _{BD}	Output Disable Time from UB, LB	_	8	_	8	

Write Cycle

CVMDOL	DADAMETED	TC551664AJ -15	64AJ -15	TC55160	64AJ -20	LIMIT
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT
t _{WC}	Write Cycle Time	15	_	20	_	
t _{WP}	Write Pulse Width	9	_	10	_	
t _{CW}	Chip Enable to End of Write	12	_	13	_	
t _{BW}	UB, LB Enable to End of Write	12	_	12	_	
t _{AW}	Address Valid to End of Write	12	_	12	_	
t _{AS}	Address Setup Time	0	_	0	_	ns
t _{WR}	Write Recovery Time	0	_	0	_	
t _{DS}	Data Setup Time	8	_	10	_	
t _{DH}	Data Hold Time	0	_	0	_	
t _{OEW}	Output Enable Time from WE	1	_	1	_	1
t _{ODW}	Output Disable Time from WE	_	8	_	8	1

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

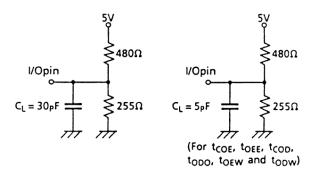


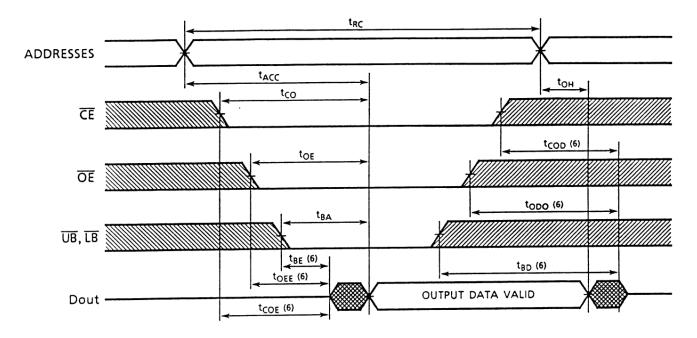
Figure 1.

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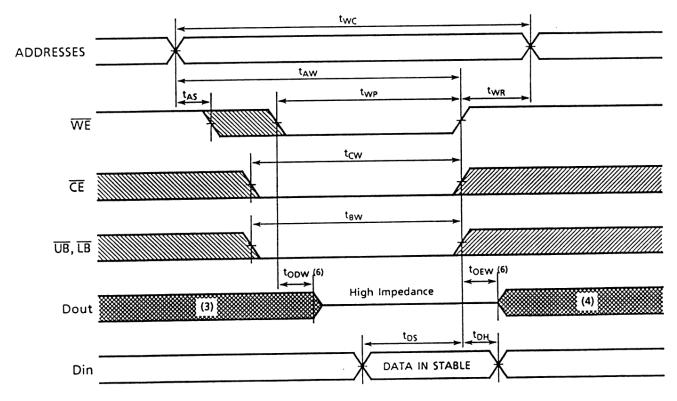
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Timing Waveforms

Read Cycle (2)

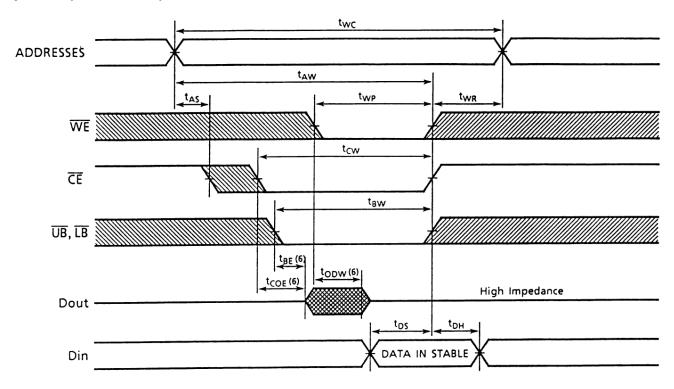


Write Cycle 1 (5) (WE Controlled)



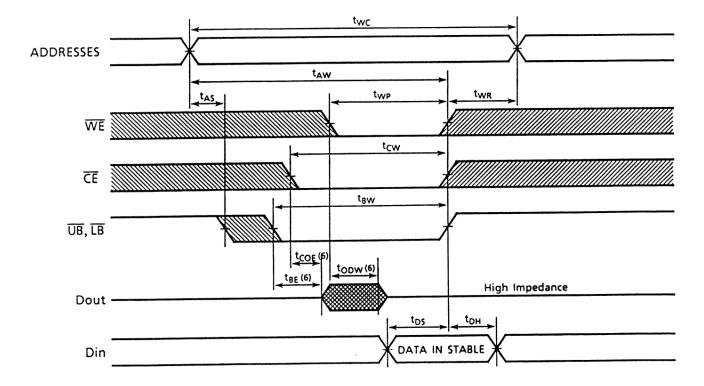
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Write Cycle 2 (5) (CE Controlled)



Write Cycle 3 (5) (UB, LB Controlled)

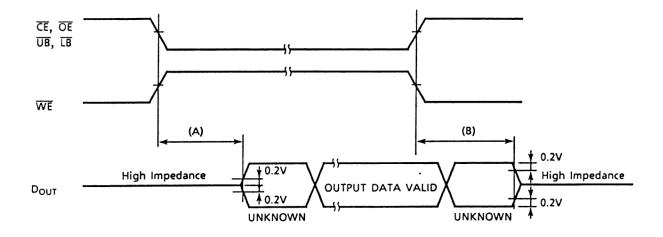
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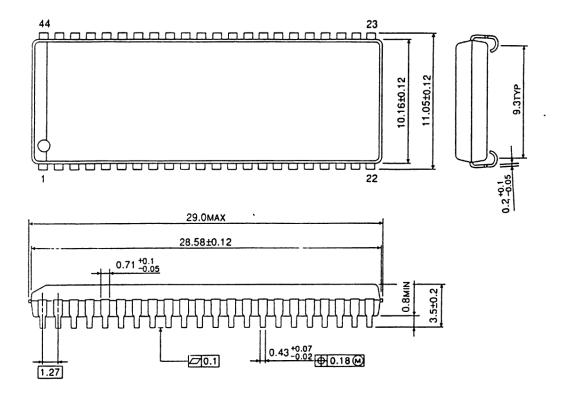
Notes:

- 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
- 2. WE is High for Read Cycle.
- 3. Assuming that $\overline{\text{CE}}$ Low transition occurs coincident with or after the $\overline{\text{WE}}$ Low transition, Outputs remain in a high impedance state.
- 4. Assuming that $\overline{\text{CE}}$ High transition occurs coincident with or prior to the $\overline{\text{WE}}$ High transition, Outputs remain in a high impedance state.
- 5. Assuming that \overline{OE} is High for Write Cycle, the Outputs are in a high impedance state during this period.
- 6. These parameters are specified and measured by using the load shown in Figure 1.
 - (A) $t_{\text{COE}},\,t_{\text{OEE}},\,t_{\text{OEW}}\dots$. Output Enable Time
 - (B) t_{COD} , t_{ODO} , t_{ODW} Output Disable Time



Outline Drawings Unit in mm

Plastic SOJ (SOJ44-P-400)



Weight: 1.64g (Typ.)

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