TOSHIBA

UTOPIA Multiplexer/ De-Multiplexer

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D A T A B O O K

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1 PHY Interface Functional Description

The TC35885TB is a full-duplex 4:1 ATM Cell multiplexer/de-multiplexer with built in FIFO buffering per port.

It enables connection of several Physical layer devices (8 or 16-bit mode) to a single ATM layer device (16-bit) using the ATM-FORUM UTOPIA Level 2 specification. Each port has a built in FIFO capable of storing up to 30 ATM cells in the receive direction and up to 16 ATM cells in the transmit direction. This configuration allows four full duplex ATM cell streams to be multiplexed/de-multiplexed into a data stream of up to 800Mbps. When two 8-bit ports are configured in 16-bit mode, the receive and transmit FIFO port storage can be increased to 60 cells and 32 cells storage respectively.

One of the key features of TC35885TB is that it has been designed to operate in stand-alone mode, capable of handling Idle/Unassigned/SOC-error condition, and has a self-learning mechanism in order to detect the active UTOPIA ports. The TC35885TB has a timeout mechanism to detect if a logical Utopia port is disabled or re-configured thus preventing Head of Line blocking.

Its main goals are:

- Standalone operation, no microprocessor required.
- Low cost, low power, using a space saving T-BGA 256 package.
- Fast time to market
- ATM-Forum UTOPIA Level 1/2 compliant
- Physical layer port fan-out expansion and concentration.
- 8-bit to 16-bit bridging to multi-PHY.
- Applications include Switches, Access Concentrators and DSLAM.

1.1 Conventions

Nomenclature selected to describe interfaces is as follows:

Logical UTOPIA Port – LUP: logical Utopia address range from 0-30

Physical UTOPIA Port – PUP: Physical side Utopia port number 0-3

ATM UTOPIA Port – AUP: ATM side Utopia port

PHYn – refers to Physical Layer ports where n = 0, 1, 2 or 3.

2 TC35885TB Features

The full feature set supported by the TC35885TB is described in the following section:

2.1 Full-duplex 4:1 ATM Cell Mux/Demux

Capable of multiplexing four UTOPIA level 1/level 2 ports to one UTOPIA level 2 port and demultiplexing of one UTOPIA level 2 port to four UTOPIA level 1/level 2 ports

2.2 Up to 400mbps transfer rate at each PHY layer interface

Each PUP is capable of running at 50MHz with an 8-bit interface, thus supporting a 400Mbps transfer rate.

2.3 Up to 800mbps transfer rate at the ATM layer interface

The AUP side is capable of running at 50MHz with a 16-bit interface, thus supporting 800Mbps transfer rate

2.4 Idle/Unassigned cell discard

Idle and Unassigned cells are discarded in PHY-to-ATM direction and forwarded in the ATM-to-PHY direction. This allows backward compatibility with existing systems.

2.5 Per port buffering on chip

In 8-bit mode it is possible to store up to 30 cells in the Receive direction and up to 16-cells in the Transmit direction. In 16-bit mode the storage capability is doubled to 60 and 30 respectively.

2.6 Selectable 8/16 bit UTOPIA level1/level 2 ports on PHY side

It is possible to configure the PUP side to 8-bit or 16-bit mode by using the PHYUTOPCONFIG pins.

2.7 16 bit wide UTOPIA level 2 interface on ATM layer side.

The AUP side is fixed at 16 bit.

2.8 Independent PHY UTOPIA clocks per port

Each PUP supports it own CLK for both Transmit and Receive directions.

2.9 Standalone operation without microprocessor

One of the main advantages of TC35885TB is that there is no microprocessor interface required.

2.10 Built-in timeout mechanism to detect disabled ports

The built-in timeout mechanism is used to detect when LUPs have been de-activated. Once the system Software disables a LUP, the TC35885TB will detect the inactive LUP and remove it

from the internal LUP status tables.

2.11 Weighted round robin algorithm to poll LUPs

This allows the system designer to assign some priority to specific LUPs to ensure they are serviced as often as possible.

2.12 JTAG port for boundary scan testing

The JTAG implementation compliant with to IEEE1149.1 and supports the following functions:

EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS and IDCODE

2.13 Low cost

The TC35885TB uses advanced low power 0.3-micron CMOS operating at 3.3V. It uses a space saving T-BGA 256 package with 5V tolerant inputs.

3 Functional Description

A functional overview of the TC35885TB is given here. The architecture is essentially divided into two sections: the Transmit UTOPIA and the Receive UTOPIA. See Figure 3-1.

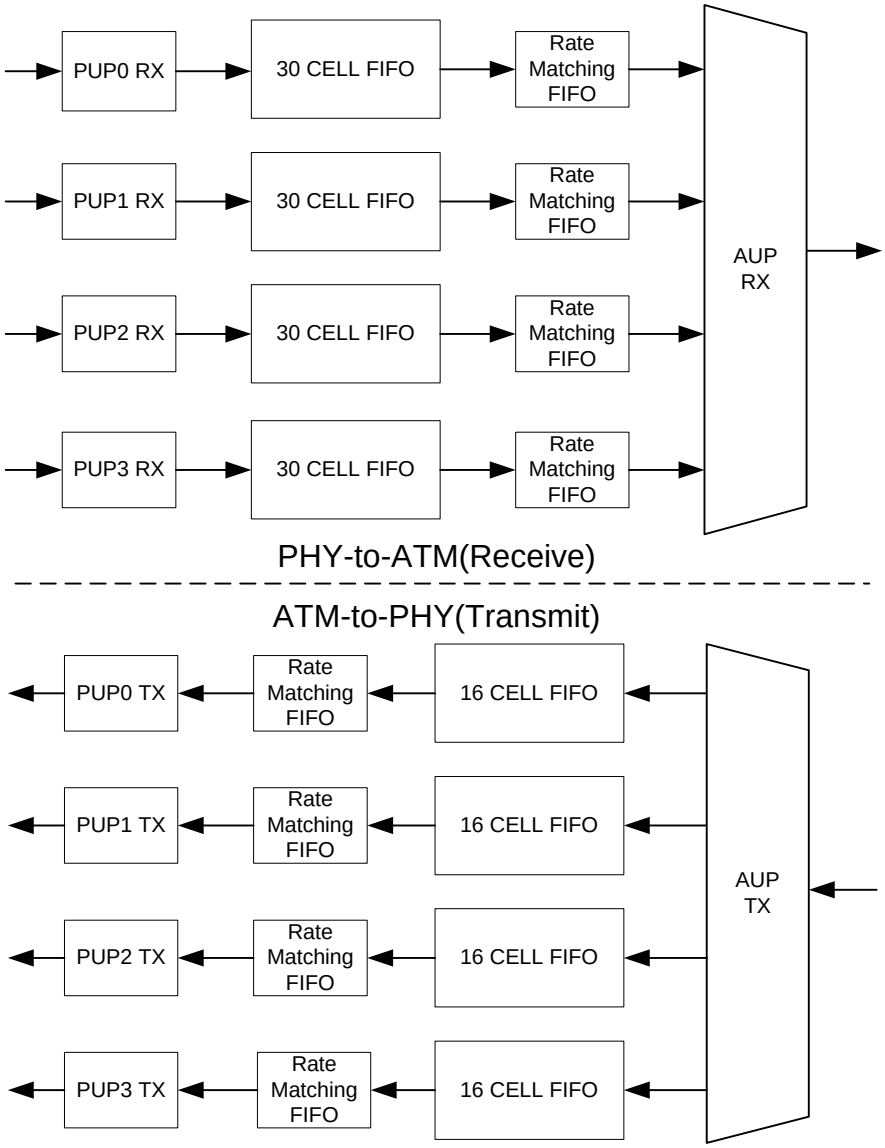


Figure 3-1 Functional Overview

All ports have common interfaces, so it is sufficient to describe only data flow for one PHY interface.

The functional description will be outlined as follows:

(a) PHY-to-ATM Data Flow (Receive)

(b) ATM-to-PHY Data Flow (Transmit)

(c) PUP functional description

(d) AUP functional description

(e) Transmit Cell Timeout

3.1 PHY-to-ATM layer data flow overview (receive)

(1) Operating in 8-bit or 16-bit mode, all PHY ports are polled independently in a weighted round robin scheme defined in 3.3.2. PHYn_RXCLAVs associated with each LUP are stored in a RxClav Status Register.

(2) If PHYn_RXCLAV is asserted and the FIFO is not full, the cell is processed. This means PHYn_RXENB_L is asserted and a complete cell is transferred into the FIFO using the cell level handshaking mechanism in [1].

(3) An error detect mechanism is included to detect missing PHYn_RXSOC. Idle cells and Unassigned cells are detected and discarded. All other cells are stored in the FIFO together with their associated LUP address.

(4) To ensure backward compatibility between 8-bit and 16-bit modes, UDF2 field is automatically inserted in the internal data structure in accordance with [1].

(5) The “Head of Line” cells within each FIFO indicate the LUP address to the AUP. The ATM layer polls the internal RxClav Status Register and detects which LUP needs to be serviced. The source LUP address is transferred to the ATM_RXADDR[4:0] of the AUP. The ATM layer device selects the LUP, asserts ATM_RXENB_L and transfers a complete cell as defined in [1].

3.2 ATM-to-PHY layer data flow overview (transmit)

(1) The AUP contains a TxClav Status Register, which represents the active LUPs from the PUP side. This is essentially a mirror image of all active LUPs from the four PUPs.

(2) The ATM layer polls the TxClav Status Register on the AUP side and detects which port can be serviced. The ATM layer device selects the LUP, asserts ATM_TXENB_L and transfers a complete cell to the AUP using the scheme defined in [1].

(3) The cells are then transferred to the corresponding PUP FIFO together with a destination LUP address. If the same LUP address occurs, which may happen during re-configuration, the cell is not sent to any port.

(4) Automatic byte extraction of UDF2 field is performed for 16-bit to 8-bit compliance as defined in [1].

(5) The PHY's are polled independently using the same weighted round robin scheme defined in 3.3.2. The internal PUPn TxClav Status Registers are updated. If the PUPn TxClav Status Register bit is asserted and its corresponding FIFO is not HALF_FULL, then a flag is set in the AUP TxClav Status Register.

(6) The LUP number of the "head of line" cells within each FIFO is used to select the LUP interface. Before the head of line cell is processed, the PUPn interface verifies that the PHYn_TXCLAV is asserted. If it is, then PHYn_TXENB_L is asserted and a complete cell is transferred according to cell-level hand-shaking scheme defined in [1].

NOTE: no cell is transferred from the ATM layer to the AUP if the PHY cannot accept a cell. This avoids head of line blocking within the FIFO. Also, cells are discarded if they are not sent within a certain period of time. See 3.5 Transmit Cell Timeout.

In order to be backward compatible with other systems and products, Idle/unassigned cells will be forwarded in the transmit direction.

3.3 PUP interface functional description

Each PUP operates completely independently in 8-bit Master UTOPIA Level 2 mode with a clock running up to 50MHz. On any one PUP, the clock is common and is defined for both Transmit and Receive data flows. In order to simplify operation on the Master side, the cell level handshaking mechanism defined in [1] is used to handle cell transfer.

No Parity is included on this interface.

Each PUP can be individually enabled/disabled using the PHYnUTOPEN pin.

PHYnUTOPEN = 1: Enable PUPn

PHYnUTOPEN = 0: Disable PUPn

When PUPn is disabled, the PHYn_TXDAT[7:0] are tri-stated.

The three main features of the PUP interfaces are:

i) PUP configuration options for selecting 8-bit or 16-bit interface

ii) Weighted Round Robin algorithm for prioritising LUPs

iii) Cell transfer operation for Receive and Transmit path

3.3.1 PUP Configuration Options

It is possible to configure (PUP0&PUP1) and (PUP2&PUP3) interfaces in 16-bit mode using PHYUTOPCONFIG0 and PHYUTOPCONFIG2 configuration pins respectively. This allows connection of two 8-bit interfaces to provide a 16-bit interface. In this mode the FIFO storage capability is increased to 60-cell storage in the receive direction and 32-cell storage in the transmit direction. When two interfaces are combined to form one 16-bit, one of the two 8-bit interfaces shall be designated master.

Combining two 8-bit interfaces into one 16-bit interface is possible using a configuration pin as follows:

MODE 1: PHYUTOPCONFIG0 = 0 and PHYUTOPCONFIG2 = 0

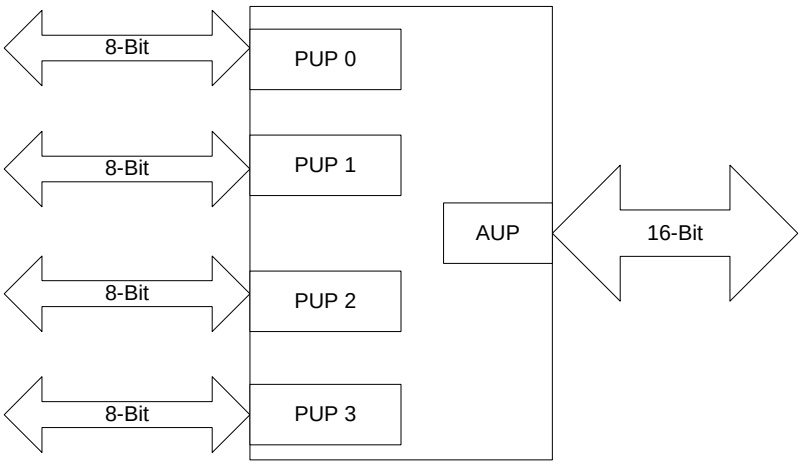


Figure 3-2 Configuration Mode 1

All PUPs are independently functional.

To enable the ports the following settings are required PHYn_UTOPEN = 1.

PHY0_UTOPEN = 1,

PHY1_UTOPEN = 1

PHY2_UTOPEN = 1,

PHY3_UTOPEN = 1

MODE 2: PHYUTOPCONFIG0 = 1 and PHYUTOPCONFIG2 = 0

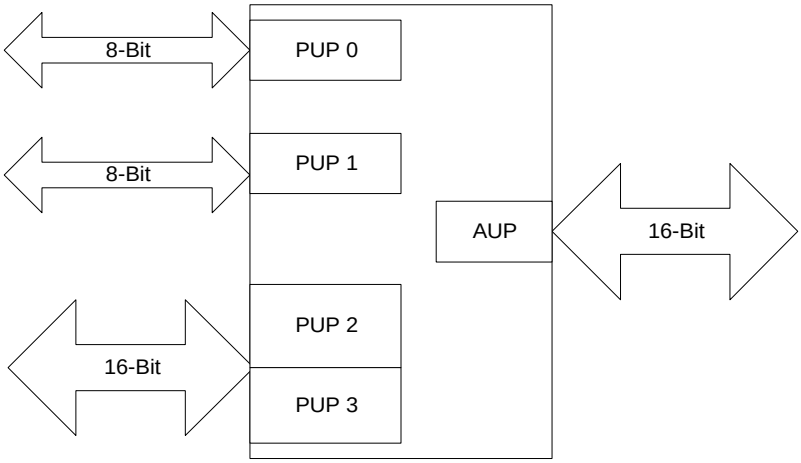


Figure 3-3 Configuration Mode 2

To enable the ports the following settings are required

PHY0_UTOPEN = 1, PHY1_UTOPEN = 0,

PHY2_UTOPEN = 1, PHY3_UTOPEN = 1

In this configuration PUP0 and PUP1 are configured in 16-bit mode, signal activity is defined as follows:

PHY1_RXDAT[7:0] becomes PHY0_RXDAT[15:8]

PHY1_TXDAT[7:0] becomes PHY0_TXDAT[15:8]

PHY1_TXSOC – tristate, not used

PHY1_TXENB_L – tristate, not used

PHY1_TXADDR[4:0] – tristate, not used

PHY1_RXENB_L – tristate, not used

PHY1_RXADDR[4:0] – tristate, not used

MODE 3: PHYUTOPCONFIG0 = 0 and PHYUTOPCONFIG2 = 1

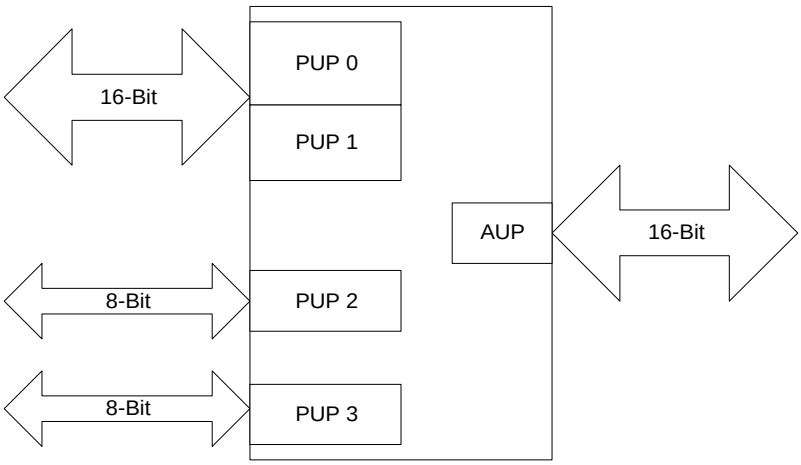


Figure 3-4 Configuration Mode 3

To enable the ports the following settings are required

PHY0_UTOPEN = 1, PHY1_UTOPEN = 1,

PHY2_UTOPEN = 1, PHY3_UTOPEN = 0

In this configuration PUP2 and PUP3 are configured in 16-bit mode, signal activity is defined as follows:

PHY3_RXDAT[7:0] becomes PHY2_RXDAT[15:8]

PHY3_TXDAT[7:0] becomes PHY2_TXDAT[15:8]

PHY3_TXSOC – tristate, not used

PHY3_TXENB_L – tristate, not used

PHY3_TXADDR[4:0] – tristate, not used

PHY3_RXADDR[4:0] – tristate, not used

PHY3_RXENB_L – tristate, not used

MODE 4: PHYUTOPCONFIG0 = 1 and PHYUTOPCONFIG2 = 1

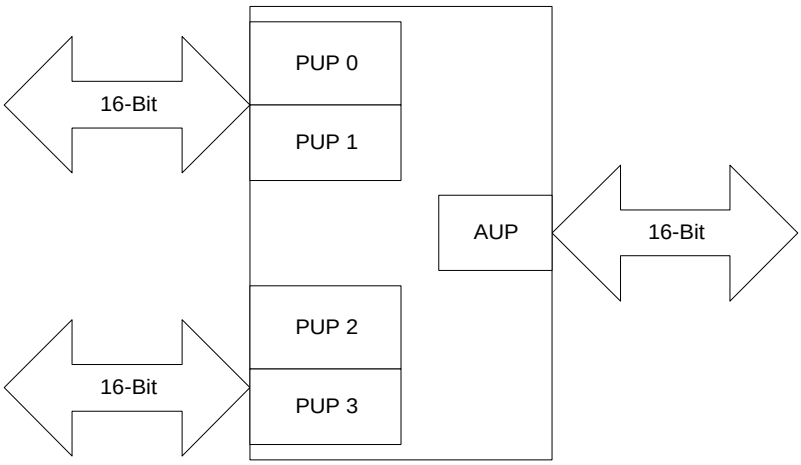


Figure 3-5 Configuration Mode 4

To enable the ports the following settings are required

PHY0_UTOPEN = 1, PHY1_UTOPEN = 0,

PHY2_UTOPEN = 1, PHY3_UTOPEN = 0

In this configuration PUP0, PUP1 and PUP2, PUP3 are configured in 16-bit mode, signal activity is defined as follows:

PHY1_RXDAT[7:0] becomes PHY0_RXDAT[15:8]

PHY1_TXDAT[7:0] becomes PHY0_TXDAT[15:8]

PHY1_TXSOC – tristate, not used

PHY1_TXENB_L – tristate, not used

PHY1_RXENB_L – tristate, not used

PHY1_TXADDR[4:0] – tristate, not used

PHY1_RXADDR[4:0] – tristate, not used

PHY3_RXDAT[7:0] becomes PHY2_RXDAT[15:8]

PHY3_TXDAT[7:0] becomes PHY2_TXDAT[15:8]

PHY3_TXSOC – tristate, not used

PHY3_TXENB_L – tristate, not used

PHY3_RXENB_L – tristate, not used

PHY3_TXADDR[4:0] – tristate, not used

PHY3_RXADDR[4:0] – tristate, not used

3.3.2 Weighted Round Robin Algorithm

In order to give some priority to LUP, a weighted round robin algorithm is used. This will ensure high priority connections are serviced as frequently as possible. The Weighted round robin algorithm is defined separately for 8-bit mode and 16-bit modes in both receive and transmit paths.

3.3.2.1 Weighted Round Robin Algorithm Receive – 8bit Mode

The basic concept is to apply some selection order of the LUP defined as follows:

Cycle n – LUP 0 – 20 (high priority) and 21 – 25 (low priority).

Cycle n+1 – LUP 0 – 20 (high priority) and 26 – 30 (low priority).

The following figures in [1] indicate modes supported:

Figure 4.4: with a one clock cycle gap between cells

Figure 4.5: with a gap equal to one cell transfer time

The following figures in [1] indicate modes NOT supported:

Figure 4.6, 4.7 and 4.8

3.3.2.2 Weighted Round Robin Algorithm Transmit – 8bit mode

The basic concept is to apply some selection order of the LUP defined as follows:

Cycle n – LUP 0 – 18 (high priority) and 19 – 24 (low priority).

Cycle n+1 – LUP 0 – 18 (high priority) and 25 – 30 (low priority).

The following figures in [1] indicate mode supported:

Figure 4.1: with a one clock cycle gap between cells

Figure 4.2: with a gap equal to one cell transfer time

The following figure in [1] indicates mode NOT supported:

Figure 4.3

3.3.2.3 Weighted Round Robin Algorithm Receive – 16bit mode

The basic concept is to apply some selection order of the LUP defined as follows:

Cycle n – LUP 16 – 26 (high priority) and 27 – 28 (low priority).

Cycle n+1 – LUP 16 – 26 (high priority) and 29 – 30 (low priority).

The following figures in [1] indicate modes supported:

Figure 4.4: with a one clock cycle gap between cells

Figure 4.5: with a gap equal to one cell transfer time

The following figures in [1] indicate modes NOT supported:

Figure 4.6, 4.7 and 4.8

3.3.2.4 Weighted Round Robin Algorithm Transmit – 16bit mode

The basic concept is to apply some selection order of the LUP defined as follows:

Cycle n – LUP 16 – 24 (high priority) and 25 – 27 (low priority).

Cycle n+1 – LUP 16 – 24 (high priority) and 28 – 30 (low priority).

The following figures in [1] indicate modes supported:

Figure 4.1: with a one clock cycle gap between cells

Figure 4.2: with a gap equal to one cell transfer time

The following figure in [1] indicates mode NOT supported:

Figure 4.3

3.3.3 PUP Receive Operation

Operating in 8-bit or 16-bit mode, all PHY ports are polled independently in a weighted round robin scheme defined in 3.1.2. CLAVs associated with each LUP are stored internally in a Status Register.

There are three possible scenarios for cell transfer:

(i) If only one LUP is connected to the interface, the current port is always polled and the fastest cell transfer rate is 1 cell in 56 clock cycles. i.e. a 3 clock cycle gap between cells.

(ii) If more than one LUP is connected and there are some pending CLAVs in the internal Status Register, then the fastest cell transfer rate is 54 clock cycles. i.e. a 1 clock cycle gap between cells.

(iii) If more than one LUP is connected and there are no pending CLAVs in the internal Status Register, then the fastest cell transfer rate is 56 clock cycles. i.e. a 3 clock cycle gap between cells.

As there are more addresses to be polled than the time available for one complete cell transfer, there is a 2 cell cycle poll sequence. This allows for polling of high priority LUPs every cell cycle period and polling of low priority LUPs every other cell cycle period. The polling sequence is described as follows:

8 Bit Mode

Cycle 1: LUP 0 to 20, 21 to 25

Cycle 2: LUP 0 to 20, 26 to 30

16 Bit Mode

Cycle 1: LUP 16 to 26, 27 to 28

Cycle 2: LUP 16 to 26, 29 to 30

During cell transfer, two conditions may occur, which result in cells being discarded. All other cells are stored in the FIFO together with their associated LUP address.

The conditions are described as follows:

(i) **SOC Error**. This may occur during system start-up or reset, when PHY-Layer device FIFO's are not fully cleared, this could result in a missing SOC in the first byte or illegal SOC at any other time in the cell. Reception is stopped over the UTOPIA interface immediately, though due to the 1 clock delay between PHYn_RXENB_L and PHYn_RXDAT[7:0] there will always be at least 2 bytes/words transferred over the utopia interface. If the PHYn_RXSOC error has occurred as a result of the PHY device containing part of a cell, the 2 transfers should result in the fragment being pulled from the PHY device eventually. As a cell is 53 bytes in 8-bit mode and 27 words in 16-bit mode (both odd numbers), the maximum time to resynchronize to the correct cell boundary should be 2 cells. The elapsed time is likely to be considerably longer however, as other

ports will be selected for data transfers in between the partial transfers from the errored port.

(ii) **Idle cells and unassigned cells**. These are detected and discarded in the receive path. They have the following format:

Idle Cell Header (H1-H4) = 00, 00, 00, 01h

Unassigned Cell Header (H1-H4) = 00, 00, 00h, 0000xxx0b

To ensure backward compatibility between 8-bit and 16-bit modes, UDF2 field is automatically inserted in the internal data structure in accordance with [1].

3.3.3.1 PUP Receive Cell Transfer Timings

The Figure below shows the poll-select mechanism during the start of a cell transfer, then the selection of a new port and subsequent cell transfer with 1 clock gap between cells. The Poll sequence length is fixed such that the SEL+1 address (address of port to be selected) appears on the PHY_RXADDR[4:0] output at the correct time relative to the PHY_RXENB_L signal.

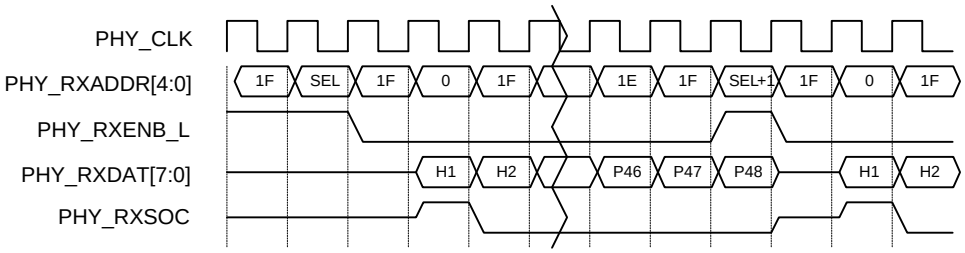


Figure 3-6 Cell transfer with 1 clock gap between cells

Figure 3-7 shows the polling mechanism when the current port is repolled and reselected. The current port (CUR) is polled during the P48 byte, if PHY_RXCLAV is detected high the same port is selected for cell transfer (SEL). This adds 2 clocks to the cell transfer period resulting in a 3 clock gap between cells (56 clock cell transfer in 8 bit mode, 30 clocks in 16 bit mode).

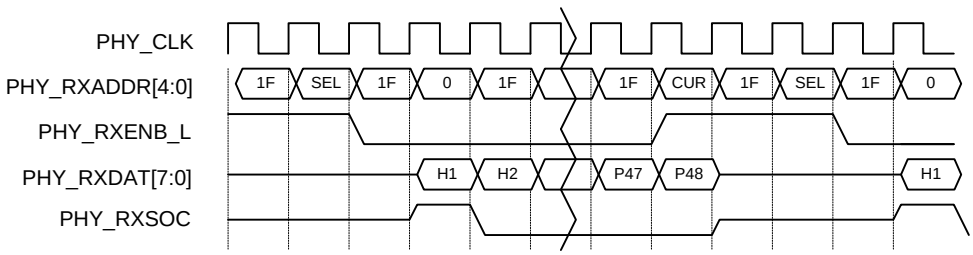


Figure 3-7 Cell transfer with 3 clock gap between cells

3.3.4 PUP Transmit Operation

Operating in 8-bit or 16-bit mode, all PHY ports are polled independently in a weighted round robin scheme defined in 3.1.2. CLAVs associated with each LUP are stored internally in a Status Register.

There are three possible scenarios for cell transfer:

(i) The time to complete a poll cycle is chosen such that there is a two clock poll of the current port and a two clock select cycle. This gives a 1 clock gap between cells (Figure 4.4 in [1]).

(ii) If there is no current port to poll (i.e. no cell was being transferred), address 1Fh is output on PHYn_TXADDR[4:0].

(iii) If there is no port to select, address 1Fh is output on PHYn_TXADDR[4:0] and no data is transferred for one cell time (54 or 28 clocks for 8/16 bit interfaces respectively).

As there are more addresses to be polled than the time available to complete one cell transfer, there is a 2 cycle poll sequence where some addresses are polled every poll cycle (high priority) and some every other poll cycle (low priority). The poll sequences are:

8 bit mode:

Cycle 1: 0 to 18, 19 - 24

Cycle 2: 0 to 18, 25 - 30

16 bit mode:

Cycle 1: 16 to 24, 25 - 27

Cycle 2: 16 to 24, 28 – 30

The internal Status register consists of a 31-bit register representing the PHYn_TXCLAV status of each of the possible 31 attached LUPs. After each poll the Status register bit corresponding to the polled address is updated with the value of the PHYn_TXCLAV input. When a port is selected for data transfer, its status bit is cleared. When the active port is polled, (as part of the normal sequence) the status register is not updated, as a poll during a data transfer may not indicate availability of a further cell in the PHY device. The active port is polled at the end of the poll sequence, during byte P47 of the transfer (the PHYn_TXCLAV response is obtained on the following cycle). The PHY device should indicate its ability to accept a further cell from byte P44 onwards, and may indicate it earlier, but to retain compatibility with UTOPIA Level 1 devices, any earlier polled response is ignored.

3.3.4.1 PUP Transmit Cell Transfer Timings

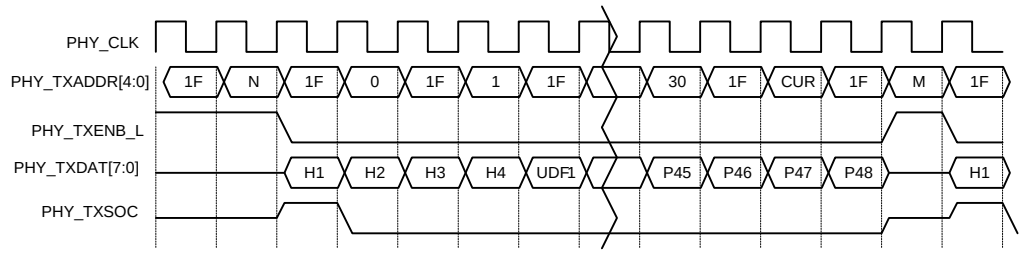


Figure 3-8 Cell transfer with 1 clock gap between cells in 8-bit mode

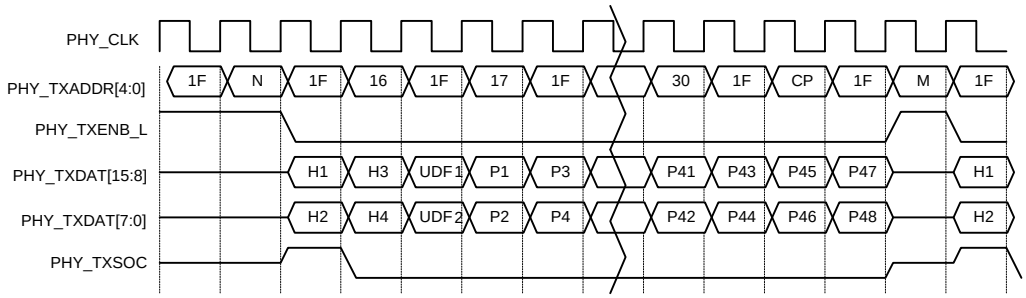


Figure 3-9 Cell transfer with 1 clock gap between cells in 16-bit mode

3.4 aup interface functional description

The AUP supports 16-bit Slave UTOPIA Level 2 mode with a clock running up to 50MHz and is capable of polling up to 31 LUPs .The ATM_CLK is common and is defined for both Transmit and Receive data flows.

NOTE: it is assumed that the PUP device addresses have been set up such that the same address does not come from more than one PUP. Thus back to back transfers can only occur from the same PUP.

3.4.1 AUP Receive Operation

The AUP polls an internal status register and detects which LUP needs to be serviced. The source LUP number is transferred to the ATM_RXADDR[4:0] of the AUP. The ATM layer device selects the LUP, asserts ATM_RXENB_L and transfers a complete cell as defined in [1].

No parity is included on this interface.

The following figures in [1] indicate modes supported:

Figure 4.4 (1 clock gap between cells)

Figure 4.5 (attempted back to back transfer, no cell)

Figure 4.7 (successful back to back transfer)

Figure 4.8 (gaps in a cell transfer)

The following figure in [1] indicates mode NOT supported:

Figure 4.6

The address range supported depends on the PUP interface:

(i) 8-bit PUP interface: 0 to 30,

(ii) 16-bit PUP interface 16-30.

3.4.1.1 Back-to-Back Cell Transfer Operation

The back to back cell transfer operation checks that at the end of a cell ATM_RXENB_L is still active and the same address on ATM_RXADDR[4:0] is selected. If this is the case, then a further cell is transferred. If the addresses do not match, then no further data is transferred. The ATM_RXSOC pin is driven low and ATM_RXDAT[15:0] is invalid (this should be ignored by the ATM layer device). The next cell transfer cannot start until ATM_RXENB_L is taken inactive and a new port selected.

3.4.1.2 Reselect Cell Transfer Operation

When an incorrect reselect address occurs after a gap in a cell transfer, we have the following two conditions:

(i) If the reselect address is recognized then invalid data is driven out on ATM_RXDAT[15:0] and ATM_RXSOC is driven inactive out to the AUP interface until ATM_RXENB_L goes inactive.

(ii) If the reselect address is not recognized, ATM_RXDAT[15:0] and ATM_RXSOC are not driven, in case the address is recognized by another TC35885TB on the same UTOPIA interface and that chip drives the bus. As ATM_RXSOC is not driven for the new address selected, the ATM layer device should detect this and interrupt the cell transfer and start again.

3.4.1.3 AUP Receive Cell Transfer Timings

The following timing diagrams show various scenarios of cell transfers from the AUP-RX interface.

Figure 3-10 shows two cells from different LUP addresses from the same PUP FIFO with a 1 clock gap between cells.

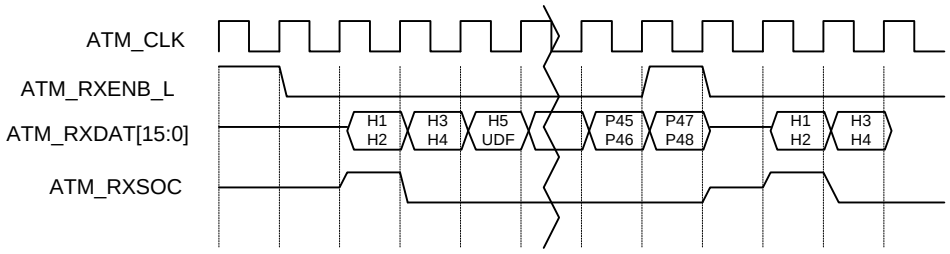


Figure 3-10 Cell transfer with 1 clock gap between cells

Figure 3-11 shows two back to back cells from the same LUP address and PUP FIFO.

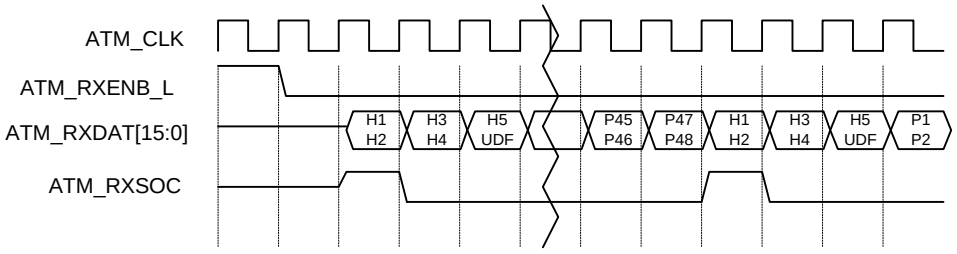


Figure 3-11 Successful back to back transfer of 2 cells

Figure 3-12 shows a failed attempt at back to back cell transfer.

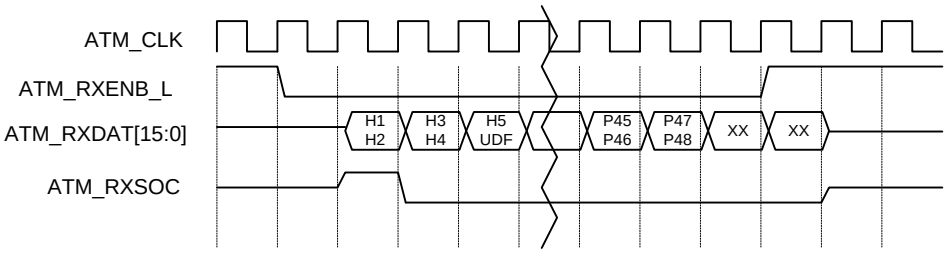


Figure 3-12 Unsuccessful back to back attempt

Figure 3-13 shows a cell transfer with a gap and a correct reselect address. Outputs are tri-stated during the gap.

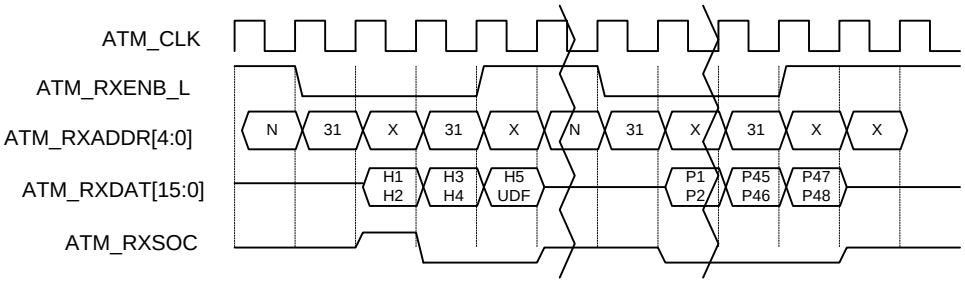


Figure 3-13 Correct reselect address after gap in cell transfer

Figure 3-14 shows a gap in the cell transfer with an incorrect reselect address. In this instance the reselect address is not recognized, so ATM_RXDAT[15:0] and ATM_RXSOC are tri-stated.

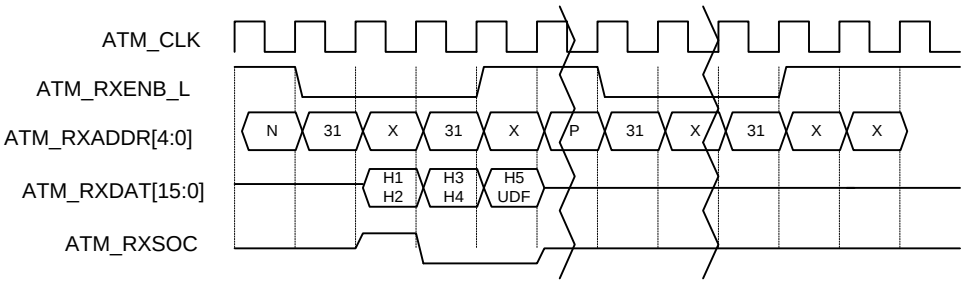


Figure 3-14 Incorrect reselect address after gap in cell transfer

3.4.2 AUP Transmit Operation

The PHYn_TXCLAV status register information from PUPn, is transferred to the AUP interface in order that the ATM layer device can perform polling. Once an active TXCLAV is detected, a cell is transferred according to [1].

No parity is included on this interface.

The following figures in [1] indicate modes supported:

Figure 4.1 (1 clock gap between cells)

Figure 4.2 (more than 1 clock gap between cells)

Figure 4.3 (gaps in a cell transfer)

Back to Back cell transfer (no figure mentioned in [1] page section 4.2.1.2)

The address range supported depends on the PUP interface:

(iii) 8-bit PUP interface: 0 to 30,

(iv) 16-bit PUP interface 16-30.

Discards cells with a SOC error i.e. Missing SOC or SOC during a cell transfer.

Discard cells with a gap if an incorrect UTOPIA address is reselected.

There is a mechanism built into the AUP side which detects which PHY side LUPs are active, this is used to select to which LUP an incoming cell should be sent. It also provides capability of timing out inactive or disabled LUPs (due to address reconfiguration perhaps).

3.4.2.1 AUP Transmit Cell Transfer Timings

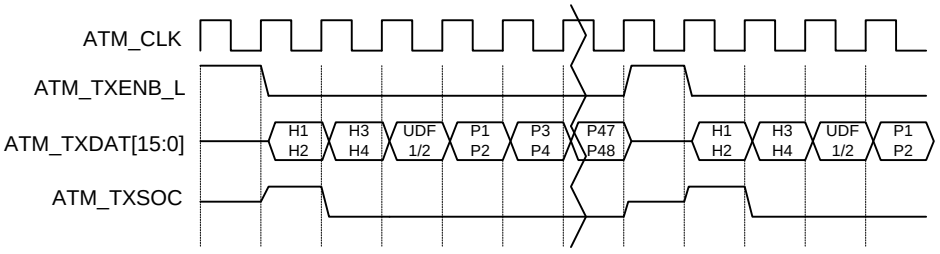


Figure 3-15 Cell transfer with 1 clock gap

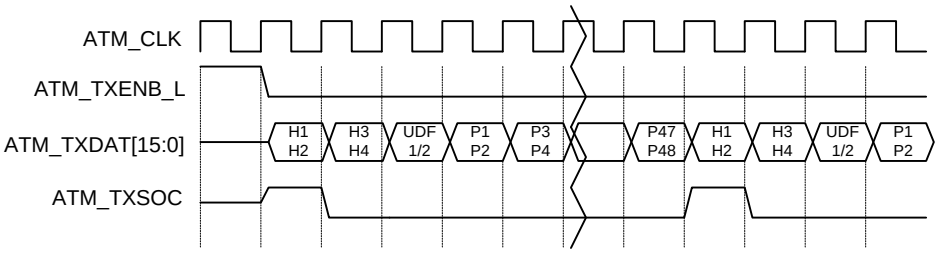


Figure 3-16 Back to Back Cell transfer

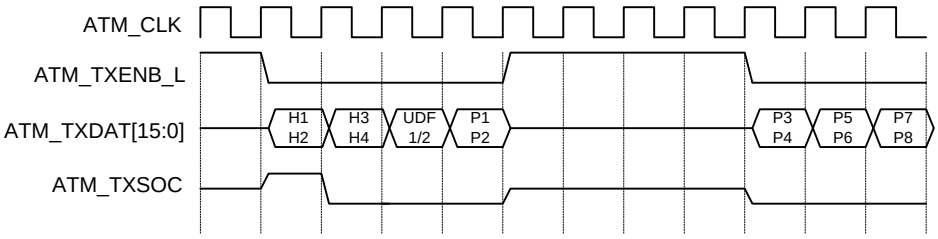


Figure 3-17 Correct reselect address after gap in cell transfer

3.5 Transmit Cell Timeout

The main purpose of the timeout mechanism is the following:

(1) Avoid the internal CLAV status registers becoming set forever after re-configuration.

(2) Avoid the theoretical head-of-line blocking of the Transmit FIFO occurring

If a PHY device has been reconfigured or disabled such that it cannot accept a cell (i.e. PHYn_TXCLAV=0) all further cell transfers may be held up (i.e. head of line blocking may occur). To prevent the cell blocking the internal FIFO for too long, there is a timeout period after which the cell is removed from the FIFO. This is done by reading the cell out as normal, but not sending it to the PUP interface (no port is selected and PHYn_TXENB_L stays inactive).

The timeout period is dependent on the clock frequency at the AUP interface and the PUP interface. Assuming a clock range of 20MHz to 50MHz on the AUP interface, the PUP logic gives a minimum timeout period of 16msec in 8-bit mode and a maximum timeout period of 128usec in 16-bit mode. These times may vary depending on when the disabled PHY is detected.

Total timeouts with PUP and AUP clock frequencies of 20MHz and 50MHz are shown in the table below:

Atm Clk	20MHz		50MHz	
Phy Clk	20MHz	50MHz	20Mhz	50MHz
8 bit mode	40ms-40.035ms	40ms-40.033ms	16ms-16.016ms	16ms-16.014ms
16 bit mode	96us - 129.4us	96us - 128.5us	38.4us - 49.4us	38.4us - 48.6us

Table 3-1 Table of timout values

3.6 Timing and Delay

Additional information to be included based on latency through TC35885TB.

4 Reset and Initialization

As long as the RESET_L is asserted, the TC35885TB asynchronously clears all internal registers and defaults state machines to idle.

The port specific PHYn_UTOPEN signal tristates and disables each port separately.

After reset, the user is only required to enable each port. No other initialization is necessary.

Signal Name	*Value after Reset*
PHYn_TXDAT[7:0]	***High-Z***
PHYn_TXSOC	***High-Z***
PHYn_TXADDR[4:0]	***High-Z***
PHYn_TXENB_L	***High-Z***
PHYn_RXENB_L	***High-Z***
PHYn_RXADDR[4:0]	***High-Z***
ATM_TXCLAV	***High-Z***
ATM_RXDAT[15:0]	***High-Z***
ATM_RXSOC	***High-Z***
ATM_RXCLAV	***High-Z***
TDO	***High-Z***

Table 4-1 Table of values after reset

5 Pin Definition and Description

5.1 Signal type definition

The following signal types are used. The convention "_L" is used to denote active low signals.

Signal Type	Definition
TI	5V tolerant LVTTL Level input
TO	LVTTL Level output Tristate Output
TIPU	5V tolerant LVTTL Level input with internal Pull Up
TIPD	5V tolerant LVTTL Level input with internal Pull Down

Table 5-1 Table of pin definitions

5.2 Pin Description

Pin description is categorized into the following categories:

(a) PHY Layer Interfaces

(b) ATM Layer Interface

(c) General and Test

(d) Power and Ground

5.2.1 PHY 0 UTOPIA Interface

Pin	Ball No	Typ	Function
PHY0_TXDAT_7	U15	TO	Transmit data PUP0 bit 7
PHY0_TXDAT_6	W17	TO	Transmit data PUP0 bit 6
PHY0_TXDAT_5	Y17	TO	Transmit data PUP0 bit 5
PHY0_TXDAT_4	V15	TO	Transmit data PUP0 bit 4
PHY0_TXDAT_3	W16	TO	Transmit data PUP0 bit 3
PHY0_TXDAT_2	Y16	TO	Transmit data PUP0 bit 2
PHY0_TXDAT_1	W15	TO	Transmit data PUP0 bit 1
PHY0_TXDAT_0	Y15	TO	Transmit data PUP0 bit 0
PHY0_TXSOC	V13	TO	Start of cell PUP0
PHY0_TXENB_L	U13	TO	Transmit enable PUP0
PHY0_TXCLAV	W14	TI	Transmit Cell Available PUP0
PHY0_TXADDR_4	U12	TO	Transmit select address PUP0 bit 4
PHY0_TXADDR_3	V12	TO	Transmit select address PUP0 bit 3
PHY0_TXADDR_2	Y13	TO	Transmit select address PUP0 bit 2
PHY0_TXADDR_1	W12	TO	Transmit select address PUP0 bit 1
PHY0_TXADDR_0	Y12	TO	Transmit select address PUP0 bit 0
PHY0_RXDAT_7	U10	TI	Receive data PUP0 bit 7
PHY0_RXDAT_6	V10	TI	Receive data PUP0 bit 6
PHY0_RXDAT_5	W10	TI	Receive data PUP0 bit 5
PHY0_RXDAT_4	U9	TI	Receive data PUP0 bit 4
PHY0_RXDAT_3	W9	TI	Receive data PUP0 bit 3
PHY0_RXDAT_2	Y9	TI	Receive data PUP0 bit 2
PHY0_RXDAT_1	W8	TI	Receive data PUP0 bit 1
PHY0_RXDAT_0	V8	TI	Receive data PUP0 bit 0
PHY0_RXSOC	U8	TI	Start of cell PUP0
PHY0_RXENB_L	Y7	TO	Receive enable PUP0
PHY0_RXCLAV	Y8	TI	Receive Cell Available PUP0
PHY0_RXADDR_4	W7	TO	Receive select address PUP0 bit 4
PHY0_RXADDR_3	Y6	TO	Receive select address PUP0 bit 3
PHY0_RXADDR_2	W6	TO	Receive select address PUP0 bit 2
PHY0_RXADDR_1	Y5	TO	Receive select address PUP0 bit 1
PHY0_RXADDR_0	V6	TO	Receive select address PUP0 bit 0
PHY0_CLK	W11	TI	Clock at Utopia interface of PUP0
PHY0_UTOPEN	Y11	TI	enables PUP0 0: PUP0 tristated/disabled 1: PUP0 enabled
Total	34 pins		

5.2.2 PHY 1 UTOPIA Interface

Pin	Ball No	Typ	Function
PHY1_TXDAT_7	J19	TO	Transmit data PUP1 bit 7 16 bit mode: PHY0_TxDAT <15:8> bit 15
PHY1_TXDAT_6	J20	TO	Transmit data PUP1 bit 6 16 bit mode: PHY0_TxDAT <15:8> bit 14
PHY1_TXDAT_5	K19	TO	Transmit data PUP1 bit 5 16 bit mode: PHY0_TxDAT <15:8> bit 13
PHY1_TXDAT_4	K20	TO	Transmit data PUP1 bit 4 16 bit mode: PHY0_TxDAT <15:8> bit 12
PHY1_TXDAT_3	L17	TO	Transmit data PUP1 bit 3 16 bit mode: PHY0_TxDAT <15:8> bit 11
PHY1_TXDAT_2	L18	TO	Transmit data PUP1 bit 2 16 bit mode: PHY0_TxDAT <15:8> bit 10
PHY1_TXDAT_1	L19	TO	Transmit data PUP1 bit 1 16 bit mode: PHY0_TxDAT <15:8> bit 9
PHY1_TXDAT_0	L20	TO	Transmit data PUP1 bit 0 16 bit mode: PHY0_TxDAT <15:8> bit 8
PHY1_TXSOC	M18	TO	Start of cell PUP1 16 bit mode: not used
PHY1_TXENB_L	M17	TO	Transmit enable PUP1 16 bit mode: not used
PHY1_TXCLAV	M19	TI	Transmit Cell Available PUP1 16 bit mode: not used
PHY1_TXADDR_4	N18	TO	Transmit select address PUP1 bit 4 16 bit mode: not used
PHY1_TXADDR_3	N17	TO	Transmit select address PUP1 bit 3 16 bit mode: not used
PHY1_TXADDR_2	N20	TO	Transmit select address PUP1 bit 2 16 bit mode: not used
PHY1_TXADDR_1	P20	TO	Transmit select address PUP1 bit 1 16 bit mode: not used
PHY1_TXADDR_0	P19	TO	Transmit select address PUP1 bit 0 16 bit mode: not used

Pin	Ball No	Typ	Function
PHY1_RXDAT_7	T20	TI	Receive data PUP1 bit 7 16 bit mode: PHY0_RXDAT<15..8> bit 15
PHY1_RXDAT_6	R18	TI	Receive data PUP1 bit 6 16 bit mode: PHY0_RXDAT<15..8> bit 14
PHY1_RXDAT_5	R17	TI	Receive data PUP1 bit 5 16 bit mode: PHY0_RXDAT<15..8> bit 13
PHY1_RXDAT_4	T19	TI	Receive data PUP1 bit 4 16 bit mode: PHY0_RXDAT<15..8> bit 12
PHY1_RXDAT_3	U20	TI	Receive data PUP1 bit 3 16 bit mode: PHY0_RXDAT<15..8> bit 11
PHY1_RXDAT_2	T17	TI	Receive data PUP1 bit 2 16 bit mode: PHY0_RXDAT<15..8> bit 10
PHY1_RXDAT_1	V20	TI	Receive data PUP1 bit 1 16 bit mode: PHY0_RXDAT<15..8> bit 9
PHY1_RXDAT_0	U18	TI	Receive data PUP1 bit 0 16 bit mode: PHY0_RXDAT<15..8> bit 8
PHY1_RXSOC	V19	TI	Start of cell PUP1 16 bit mode: not used
PHY1_RXENB_L	W19	TO	Receive enable PUP1 16 bit mode: not used
PHY1_RXCLAV	W20	TI	Receive Cell Available PUP1 16 bit mode: not used
PHY1_RXADDR_4	Y20	TO	Receive select address PUP1 bit 4 16 bit mode: not used
PHY1_RXADDR_3	V17	TO	Receive select address PUP1 bit 3 16 bit mode: not used
PHY1_RXADDR_2	U16	TO	Receive select address PUP1 bit 2 16 bit mode: not used
PHY1_RXADDR_1	W18	TO	Receive select address PUP1 bit 1 16 bit mode: not used
PHY1_RXADDR_0	Y19	TO	Receive select address PUP1 bit 0 16 bit mode: not used
PHY1_CLK	R20	TI	Clock at Utopia interface of PUP1
PHY1_UTOPEN	R19	TI	enables PUP1 0: PUP1 tristated/disabled 1: PUP1 enabled 16 bit mode: not used
Total	34pins		

5.2.3 PHY 2 UTOPIA Interface

Pin	Ball No	Typ	Function
PHY2_TXDAT_7	A14	TO	Transmit data PUP2 bit 7
PHY2_TXDAT_6	B14	TO	Transmit data PUP2 bit 6
PHY2_TXDAT_5	A15	TO	Transmit data PUP2 bit 5
PHY2_TXDAT_4	B15	TO	Transmit data PUP2 bit 4
PHY2_TXDAT_3	A16	TO	Transmit data PUP2 bit 3
PHY2_TXDAT_2	C15	TO	Transmit data PUP2 bit 2
PHY2_TXDAT_1	D15	TO	Transmit data PUP2 bit 1
PHY2_TXDAT_0	B16	TO	Transmit data PUP2 bit 0
PHY2_TXSOC	A17	TO	Start of cell PUP2
PHY2_TXENB_L	D16	TO	Transmit enable PUP2
PHY2_TXCLAV	A18	TI	Transmit Cell Available PUP2
PHY2_TXADDR_4	C17	TO	Transmit select address PUP2 bit 4
PHY2_TXADDR_3	B18	TO	Transmit select address PUP2 bit 3
PHY2_TXADDR_2	A19	TO	Transmit select address PUP2 bit 2
PHY2_TXADDR_1	B19	TO	Transmit select address PUP2 bit 1
PHY2_TXADDR_0	E17	TO	Transmit select address PUP2 bit 0
PHY2_RXDAT_7	C20	TI	Receive data PUP2 bit 7
PHY2_RXDAT_6	E18	TI	Receive data PUP2 bit 6
PHY2_RXDAT_5	F17	TI	Receive data PUP2 bit 5
PHY2_RXDAT_4	D19	TI	Receive data PUP2 bit 4
PHY2_RXDAT_3	D20	TI	Receive data PUP2 bit 3
PHY2_RXDAT_2	F18	TI	Receive data PUP2 bit 2
PHY2_RXDAT_1	E19	TI	Receive data PUP2 bit 1
PHY2_RXDAT_0	E20	TI	Receive data PUP2 bit 0
PHY2_RXSOC	F19	TI	Start of cell PUP2
PHY2_RXENB_L	H17	TO	Receive enable PUP2
PHY2_RXCLAV	F20	TI	Receive Cell Available PUP2
PHY2_RXADDR_4	H18	TO	Receive select address PUP2 bit 4
PHY2_RXADDR_3	G19	TO	Receive select address PUP2 bit 3
PHY2_RXADDR_2	G20	TO	Receive select address PUP2 bit 2
PHY2_RXADDR_1	J18	TO	Receive select address PUP2 bit 1
PHY2_RXADDR_0	H20	TO	Receive select address PUP2 bit 0
PHY2_CLK	C19	TI	Clock at Utopia interface of PUP2
PHY2_UTOPEN	B20	TI	enables PUP2 0: PUP1 tristated/disabled 1: PUP1 enabled
Total	34pins		

5.2.4 PHY 3 UTOPIA Interface

Pin	Ball No	Typ	Function
PHY3_TXDAT_7	B2	TO	Transmit data PUP3 bit 7 16 bit mode: PHY2_TxDAT <15:8> bit 15
PHY3_TXDAT_6	A1	TO	Transmit data PUP3 bit 6 16 bit mode: PHY2_TxDAT <15:8> bit 14
PHY3_TXDAT_5	C4	TO	Transmit data PUP3 bit 5 16 bit mode: PHY2_TxDAT <15:8> bit 13
PHY3_TXDAT_4	D5	TO	Transmit data PUP3 bit 4 16 bit mode: PHY2_TxDAT <15:8> bit 12
PHY3_TXDAT_3	B3	TO	Transmit data PUP3 bit 3 16 bit mode: PHY2_TxDAT <15:8> bit 11
PHY3_TXDAT_2	C5	TO	Transmit data PUP3 bit 2 16 bit mode: PHY2_TxDAT <15:8> bit 10
PHY3_TXDAT_1	D6	TO	Transmit data PUP3 bit 1 16 bit mode: PHY2_TxDAT <15:8> bit 9
PHY3_TXDAT_0	B4	TO	Transmit data PUP3 bit 0 16 bit mode: PHY2_TxDAT <15:8> bit 8
PHY3_TXSOC	A4	TO	Start of cell PUP3 16 bit mode: not used
PHY3_TXENB_L	C6	TO	Transmit enable PUP3 16 bit mode: not used
PHY3_TXCLAV	B5	TI	Transmit Cell Available PUP3 16 bit mode: not used
PHY3_TXADDR_4	A5	TO	Transmit select address PUP3 bit 4 16 bit mode: not used
PHY3_TXADDR_3	B6	TO	Transmit select address PUP3 bit 3 16 bit mode: not used
PHY3_TXADDR_2	A6	TO	Transmit select address PUP3 bit 2 16 bit mode: not used
PHY3_TXADDR_1	D8	TO	Transmit select address PUP3 bit 1 16 bit mode: not used
PHY3_TXADDR_0	C8	TO	Transmit select address PUP3 bit 0 16 bit mode: not used

Pin	Ball No	Typ	Function
PHY3_RXDAT_7	C9	TI	Receive data PUP3 bit 7 16 bit mode: PHY0_RXDAT<15..8> bit 15
PHY3_RXDAT_6	A8	TI	Receive data PUP3 bit 6 16 bit mode: PHY0_RXDAT<15..8> bit 14
PHY3_RXDAT_5	B9	TI	Receive data PUP3 bit 5 16 bit mode: PHY0_RXDAT<15..8> bit 13
PHY3_RXDAT_4	A9	TI	Receive data PUP3 bit 4 16 bit mode: PHY0_RXDAT<15..8> bit 12
PHY3_RXDAT_3	B10	TI	Receive data PUP3 bit 3 16 bit mode: PHY0_RXDAT<15..8> bit 11
PHY3_RXDAT_2	A10	TI	Receive data PUP3 bit 2 16 bit mode: PHY0_RXDAT<15..8> bit 10
PHY3_RXDAT_1	D11	TI	Receive data PUP3 bit 1 16 bit mode: PHY0_RXDAT<15..8> bit 9
PHY3_RXDAT_0	C11	TI	Receive data PUP3 bit 0 16 bit mode: PHY0_RXDAT<15..8> bit 8
PHY3_RXSOC	A11	TI	Start of cell PUP3 16 bit mode: not used
PHY3_RXENB_L	C12	TO	Receive enable PUP3 16 bit mode: not used
PHY3_RXCLAV	B11	TI	Receive Cell Available PUP3 16 bit mode: not used
PHY3_RXADDR_4	D12	TO	Receive select address PUP3 bit 4 16 bit mode: not used
PHY3_RXADDR_3	B12	TO	Receive select address PUP3 bit 3 16 bit mode: not used
PHY3_RXADDR_2	C13	TO	Receive select address PUP3 bit 2 16 bit mode: not used
PHY3_RXADDR_1	D13	TO	Receive select address PUP3 bit 1 16 bit mode: not used
PHY3_RXADDR_0	A13	TO	Receive select address PUP3 bit 0 16 bit mode: not used
PHY3_CLK	B8	TI	Clock at Utopia interface of PUP3
PHY3_UTOPEN	D9	TI	enables PUP3 0: PUP3 tristated/disabled 1: PUP3 enabled 16 bit mode: not used
Total	34pins		

5.2.5 ATM UTOPIA Interface

Pin	Ball No	Typ	Function
ATM_TXDAT_15	M4	TI	Transmit data AUP bit 15
ATM_TXDAT_14	M3	TI	Transmit data AUP bit 14
ATM_TXDAT_13	N1	TI	Transmit data AUP bit 13
ATM_TXDAT_12	M2	TI	Transmit data AUP bit 12
ATM_TXDAT_11	M1	TI	Transmit data AUP bit 11
ATM_TXDAT_10	L2	TI	Transmit data AUP bit 10
ATM_TXDAT_9	L1	TI	Transmit data AUP bit 9
ATM_TXDAT_8	K4	TI	Transmit data AUP bit 8
ATM_TXDAT_7	K3	TI	Transmit data AUP bit 7
ATM_TXDAT_6	K2	TI	Transmit data AUP bit 6
ATM_TXDAT_5	K1	TI	Transmit data AUP bit 5
ATM_TXDAT_4	J3	TI	Transmit data AUP bit 4
ATM_TXDAT_3	J1	TI	Transmit data AUP bit 3
ATM_TXDAT_2	H2	TI	Transmit data AUP bit 2
ATM_TXDAT_1	H3	TI	Transmit data AUP bit 1
ATM_TXDAT_0	H4	TI	Transmit data AUP bit 0
ATM_TXSOC	H1	TI	Transmit start of cell for AUP
ATM_TXENB_L	G1	TI	Transmit enable AUP
ATM_TXCLAV	G2	TO	Transmit Cell Available AUP
ATM_TXADDR_4	F1	TI	Transmit select address AUP bit 4
ATM_TXADDR_3	F2	TI	Transmit select address AUP bit 3
ATM_TXADDR_2	E1	TI	Transmit select address AUP bit 2
ATM_TXADDR_1	F3	TI	Transmit select address AUP bit 1
ATM_TXADDR_0	F4	TI	Transmit select address AUP bit 0

Pin	Ball No	Typ	Function
ATM_RXDAT_15	U6	TO	Receive data AUP bit 15
ATM_RXDAT_14	W5	TO	Receive data AUP bit 14
ATM_RXDAT_13	Y4	TO	Receive data AUP bit 13
ATM_RXDAT_12	U5	TO	Receive data AUP bit 12
ATM_RXDAT_11	Y3	TO	Receive data AUP bit 11
ATM_RXDAT_10	V4	TO	Receive data AUP bit 10
ATM_RXDAT_9	W3	TO	Receive data AUP bit 9
ATM_RXDAT_8	Y2	TO	Receive data AUP bit 8
ATM_RXDAT_7	W2	TO	Receive data AUP bit 7
ATM_RXDAT_6	Y1	TO	Receive data AUP bit 6
ATM_RXDAT_5	U3	TO	Receive data AUP bit 5
ATM_RXDAT_4	T4	TO	Receive data AUP bit 4
ATM_RXDAT_3	V2	TO	Receive data AUP bit 3
ATM_RXDAT_2	W1	TO	Receive data AUP bit 2
ATM_RXDAT_1	V1	TO	Receive data AUP bit 1
ATM_RXDAT_0	T3	TO	Receive data AUP bit 0
ATM_RXSOC	R4	TO	Start of cell AUP
ATM_RXENB_L	U1	TI	Receive enable AUP
ATM_RXCLAV	U2	TO	Receive Cell Available AUP
ATM_RXADDR_4	T1	TI	Receive select address AUP bit 4
ATM_RXADDR_3	R2	TI	Receive select address AUP bit 3
ATM_RXADDR_2	R1	TI	Receive select address AUP bit 2
ATM_RXADDR_1	N4	TI	Receive select address AUP bit 1
ATM_RXADDR_0	N3	TI	Receive select address AUP bit 0
ATM_CLK	P2	TI	Clock at the Utopia interface of AUP
Total	49pins		

5.2.6 General and Test

Pin	Ball No	Typ	Function
RESET_L	E3	TI	Reset active low
PHYUTOPCONFIG0	E2	TI	selects 8 or 16 bit mode of PUP 0 & PUP1 0: Utopia port 0 & 1 operate in 8 bit mode 1: Utopia port 0 & 1 build one 16 bit interface
PHYUTOPCONFIG2	D1	TI	selects 8 or 16 bit mode of PUP 2 & PUP 3 0: Utopia port 2 & 3 operate in 8 bit mode 1: Utopia port 2 & 3 build one 16 bit interface
TEST_MODE	M20	TIPD	Internal Testmode, tie to ground
RAM_TEST	D2	TIPD	Internal RAM Testmode, tie to ground
TDI	E4	TIPU	JTAG serial data input
TDO	C1	TO	JTAG serial data output
TCK	D3	TI	JTAG data clock
TMS	C2	TIPU	JTAG mode select
TRST_L	B1	TIPU	JTAG reset
Total	10pins		

5.2.7 Power and Ground

Pin	Ball No	Typ	Function
VDD	A3, A7, B13, B17, C3, C7, C10, C14, C18, D18, G3, G18, J2, J17, K18, L3, N2, P3, P18, U19, V3, V5, V7, V9, V11, V14, V16, V18, W13	VDD	Power
Total	29 pins		
VSS	A2, A12, A20, B7, C16, D4, D7, D10, D14, D17, G4, G17, H19, J4, K17, L4, **N19***, P1, P4, P17, R3, **T2***, T18, U4, U7, U11, U14, U17, W4, Y10, Y14, Y18	VSS	Ground
Total	32pins		

***ATTENTION**: ES parts have the following:

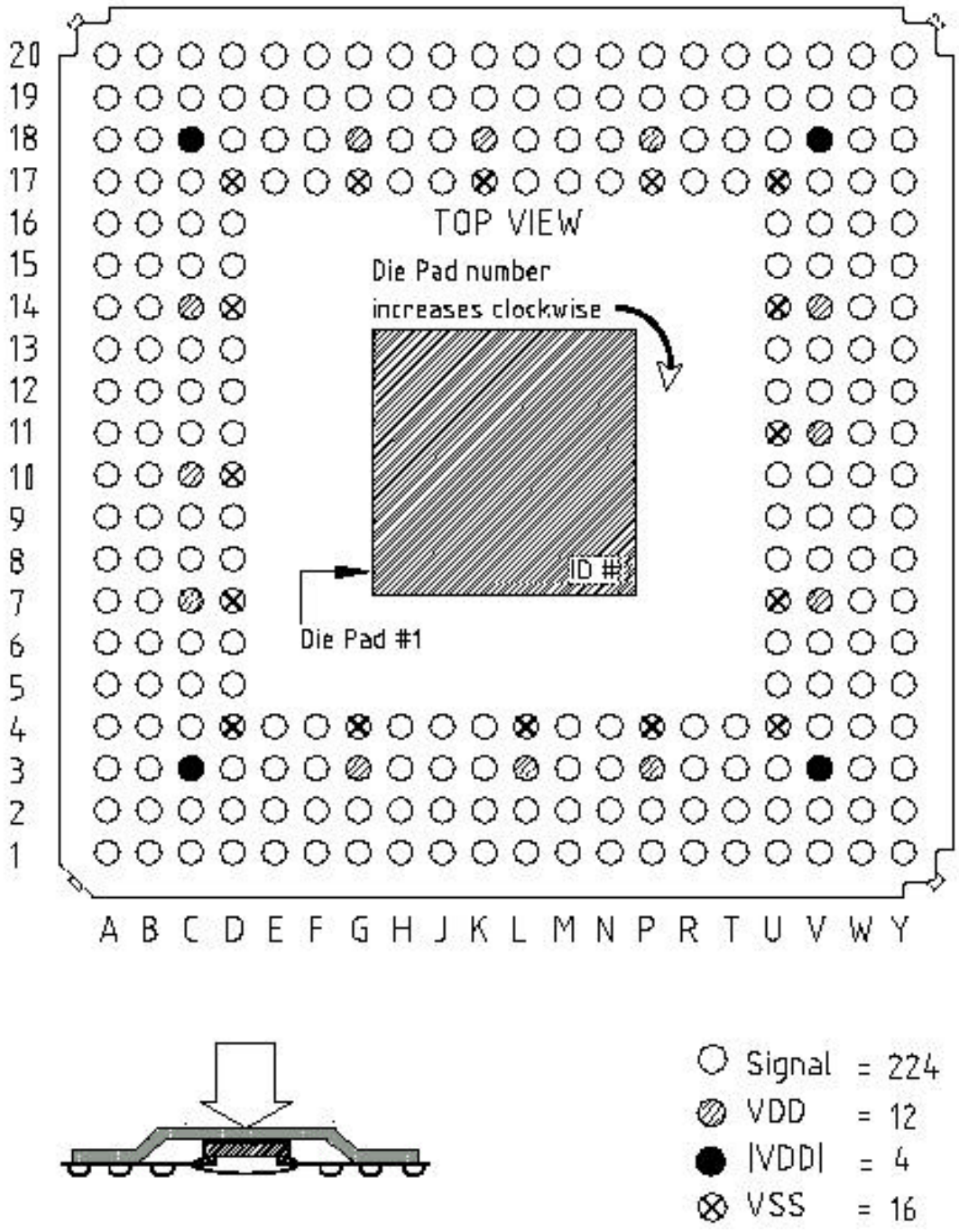
N19 and **T2** should be VSS but on the samples they appear as VDD pins.

Please contact Toshiba for advice.

This will be corrected in the next version.

5.3 TC35885TB pinout

256 TBGA Ball A1 Location



Note: Solder balls are not visible on this side (Top View) of the package.

Figure 5-1 Power and Ground placement and Lead orientation

6 JTAG TEST SUPPORT

JTAG Boundary Scan addresses the issues of board-level testability. The boundary scan technique associates register cells with the IO pads of IC's. These register cells are connected to form a long shift register chain called the Boundary Scan Path. Since the boundary scan path is comprised of the input and output pads of an IC, they can be used for applying and sampling data after the chip is mounted onto a PCB.

The main objectives of boundary scan are checking interconnections between IC s for shorts, opens and solder bridges; and in checking for misloaded components, including wrong, or missing chips. Refer to the "IEEE Standard Test Access Port and Boundary Scan Architecture" for more details.

It is assumed that the reader is familiar with both JTAG architectures, and TAP controllers.

The JTAG test port on the TC35885TB, allows access to the TAP (Test Access Port) controller which is used to load JTAG instructions as defined by the IEEE1149.1 JTAG standard. The TAP controller is the JTAG interface between the chip and the external environment. The following instructions are supported:

(i) EXTEST

(ii) SAMPLE/PRELOAD

(iii) BYPASS

(iv) INTEST

(v) IDCODE

The TAP controller users a five-bit instruction register and the codes associated to the above functions are shown below:

Instruction Code	Instruction	Selected Register
00000	EXTEST	Boundary Scan
00001	SAMPLE/PRELOAD	Boundary Scan
00010	INTEST	Boundary Scan
00011	IDCODE	Device Identification
10001 to 11110	BYPASS	Bypass

The length of the Boundary Scan register is 205 bits, and serial input to both this and the Instruction register are made through the TDI pin, and should be shifted in LSB first.

6.1 jtag instructions

6.1.1 Sample/Preload

The instruction bit pattern “00001” decodes to SAMPLE/PRELOAD, and this instruction targets all the boundary scan registers between TDI and TDO.

The SAMPLE allows the input and output pads of the device to be monitored, taking a snapshot of the activity of IO pins in order to verify interaction between components during the devices normal operation.

The PRELOAD allows the boundary scan register to be initialized before execution of another instruction. To preload, the instruction “00001” must be entered, and then when in the Shift-DR state, the data pattern is entered onto the TDI pin. A total of 205 bits must be entered in order to fill the boundary scan register. Once all bits of the boundary scan register have had a bit shifted into them, the scan output pin of each register will contain the one-bit valid data ready for transfer according to the next instruction chosen.

6.1.2 Extest

EXTEST, instruction pattern “00000”, is used to check external interconnections. It allows boundary scan registers at output pins to shift out test patterns in the Update-DR state, and allows boundary scan registers at input pins to capture test results in the Capture-DR state.

Typical execution sequence follows:

1. Initialize TAP controller to Test-Logic-Reset state;
2. Load instruction register with SAMPLE/PRELOAD instruction code (“00001”);
3. Initialize boundary scan register with a determinate sequence;
4. Load initial test data into the boundary scan register;
5. Load instruction register with EXTEST instruction code (“00000”);
6. Capture the data applied to the input pin into the boundary scan register;
7. Shift data from the boundary scan register to the output pin, TDO.

6.1.3 Bypass

This instruction targets the bypass register between TDI and TDO. The Bypass register provides a minimum length serial path between TDI and TDO when the device is not required for the current test. The length of the bypass register is 1-Bit, and hence there is a 1 TCK period delay between shifting data on TDI and TDO.

6.1.4 Intest

The INTEST instruction targets the boundary scan register between TDI and TDO for internal logic testing. Typically, a set of data is loaded into the boundary scan register using the SAMPLE/PRELOAD instruction, and then system clock cycles are used to cause activity of internal logic. The result of this internal activity is captured into the boundary scan register at

the output pins, and can be shifted out through TDO for examination.

Typical execution sequence as follows:

1. Initialize TAP controller to Test-Logic-Reset state;
2. Load instruction register with SAMPLE/PRELOAD instruction code(“00001”);
3. Initialize boundary scan register with a determinate sequence;
4. Load initial test data into the boundary scan register;
5. Load instruction register with INTEST instruction code (“00010”);
6. Pulse the system clocks;
7. Capture the response pattern into the shift portion of the boundary scan register;
8. Shift out the captured response (also next test pattern can be shifted in at the same time if desired);

6.1.5 ID Code

This instruction targets the Identification Register between TDI and TDO. The ID Register is a 32-Bit register, which is hard wired with the device ID code. The ID code for the TC35885TB is: 08C08131H, or 0000-1000-1100-0000-0100-0001-0011-0001. In order to extract the ID-code from the device, enter the instruction code “00011”, and then in the Shift-DR state, shift in 32 arbitrary bits on TDI in order to shift out the 32 bits of the ID register through TDO.

7 ELECTRICAL CHARACTERISTICS

7.1 absolute maximum ratings

Vdd	Supply Voltage	-0.3V to 5.0V
Vin(3.3V)	Input Voltage(3.3V)	-0.3V to Vdd + 0.3V
Vin(5V)	Input Voltage(5V tolerant)	-0.3V to 7.0V
Pd	Power Dissipation	2.1W
Tsolder	Soldering Temperature (10sec)	240°C
Tstg	Storage Temperature	-40°C to 125°C
Topr	Operating Temperature	-5°C to 85°C * 85°C with air flow 70°C without air flow

* Temperature range will be confirmed

7.2 DC characteristics

		Min.	Typ.	Max.	Unit
Vdd	Supply Voltage		3.300		V
Iddd	Operating Current	N.A	0.27	0.67	A
Iih	Input High Current, no pull-down		-	10	μA
	Input High Current with pull-down	10	-	200	μA
Iil	Input Low Current without pull-up	-10	-	10	μA
	Input Low Current with pull-up	-200	-	10	μA

5V Tol. Input

		Min.	Typ.	Max.	Unit
Vih	Input High Voltage	2.0	-	-	V
Vil	Input Low Voltage	-		0.8	V

3.3V Input

		Min.	Typ.	Max.	Unit
Vih	Input High Voltage	2.0	-	-	V
Vil	Input Low Voltage	-		0.8	V

3.3V Output

			Min.	Typ.	Max.	Unit
Voh	Output High Voltage	IOH= 0 mA	-	-	Vdd(3V)	V
		IOH= -2.5mA	2.4	-	-	
Vol	Output Low Voltage	IOL= 2.5mA	-	-	0.4	V

UTOPIA I/F Input/Output

		Min.	Typ.	Max.	Unit
Vih	Input High Voltage	2.0	-	-	V
Vil	Input Low Voltage			0.8	V
Voh	Output High Voltage (IOH=-4.0mA)	2.4	-	-	V
Vol	Output Low Voltage (IOL=4.0mA)	-	-	0.4	V

8 AC CHARACTERISTICS

8.1 utopia interface timing

Preliminary

No.	Parameter	Min	Typ.	Max	Unit
F1	Clk (PHYn_CLK and ATM_CLK) frequency		-	50	MHz
T2	Clk Duty Cycle	40%	-	60%	
T3	Clk – peak to peak jitter	-	-	5%	
T4	Clk – rise/fall time	-	-	2	Ns

No.	Parameter	Signal	Min	Typ.	Max	Unit
1	UTOPIA output data valid delay from PHYn_CLK↑	PhyN_RxEnb_L	2.0		12.0	ns
		PhyN_RxAddr(4:0)	2.0		12.0	ns
		PhyN_TxDat(7:0)	2.0		12.0	ns
		PhyN_TxSoc	2.0		12.0	ns
		PhyN_TxAddr(4:0)	2.0		12.0	ns
		PhyN_TxEnb_L	2.0		12.0	
2	UTOPIA input data setup time from PHYn/ATM_CLK↑		4.0		-	ns
3	UTOPIA input data hold time from PHYn/ATM_CLK↑		1.0		-	ns
4	UTOPIA output data Hi-Z delay from ATM_CLK↑	Atm_RxDat(15:0)	2.0		12.0	ns
		Atm_RxSoc	2.0		12.0	ns
		Atm_RxClav	2.0		12.0	ns
		Atm_TxClav	2.0		12 0	ns

NOTE: All timing requirements are preliminary and subject to change upon production release. The output load for PUP and AUP is 40pF.

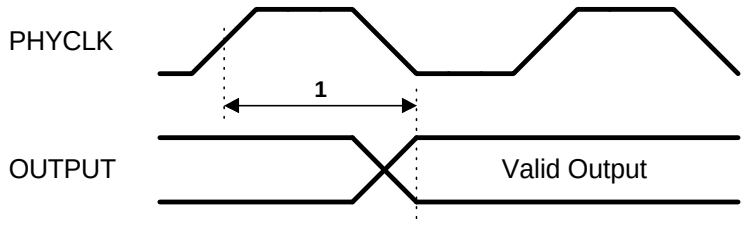


Figure 8-1 Utopia I/f Output Timing

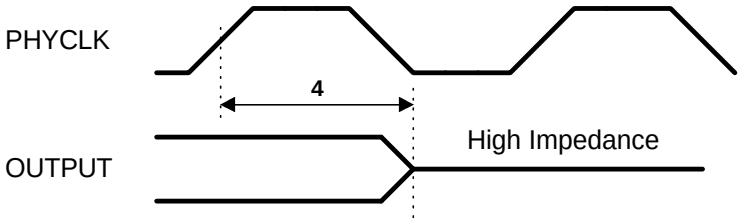


Figure 8-2 Utopia I/f Output Timing (High-Z)

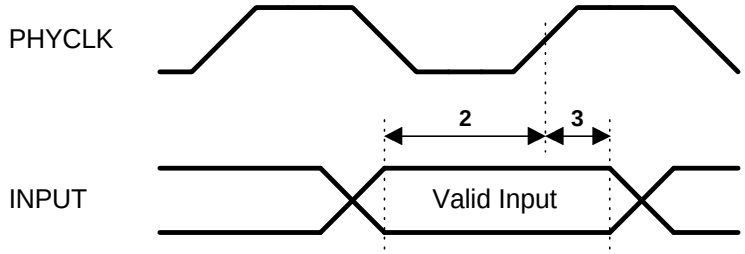


Figure 8-3 Utopia I/f Input Timing

8.2 jtag interface timing

Additional information will be provided.

9 PACKAGE OUTLINE DRAWING

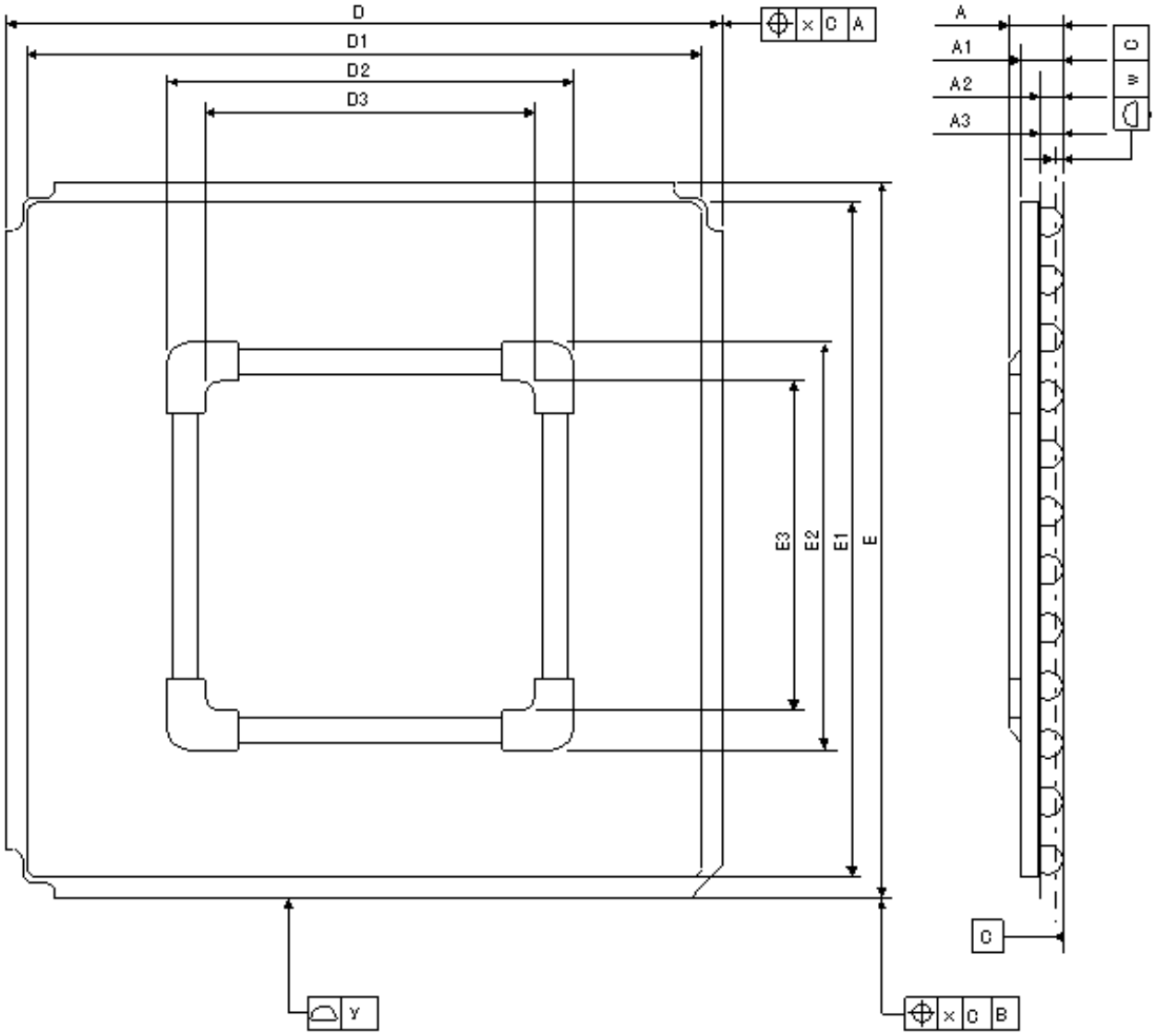


Figure 9-1 T-BGA256 Outline Dimensions Top view

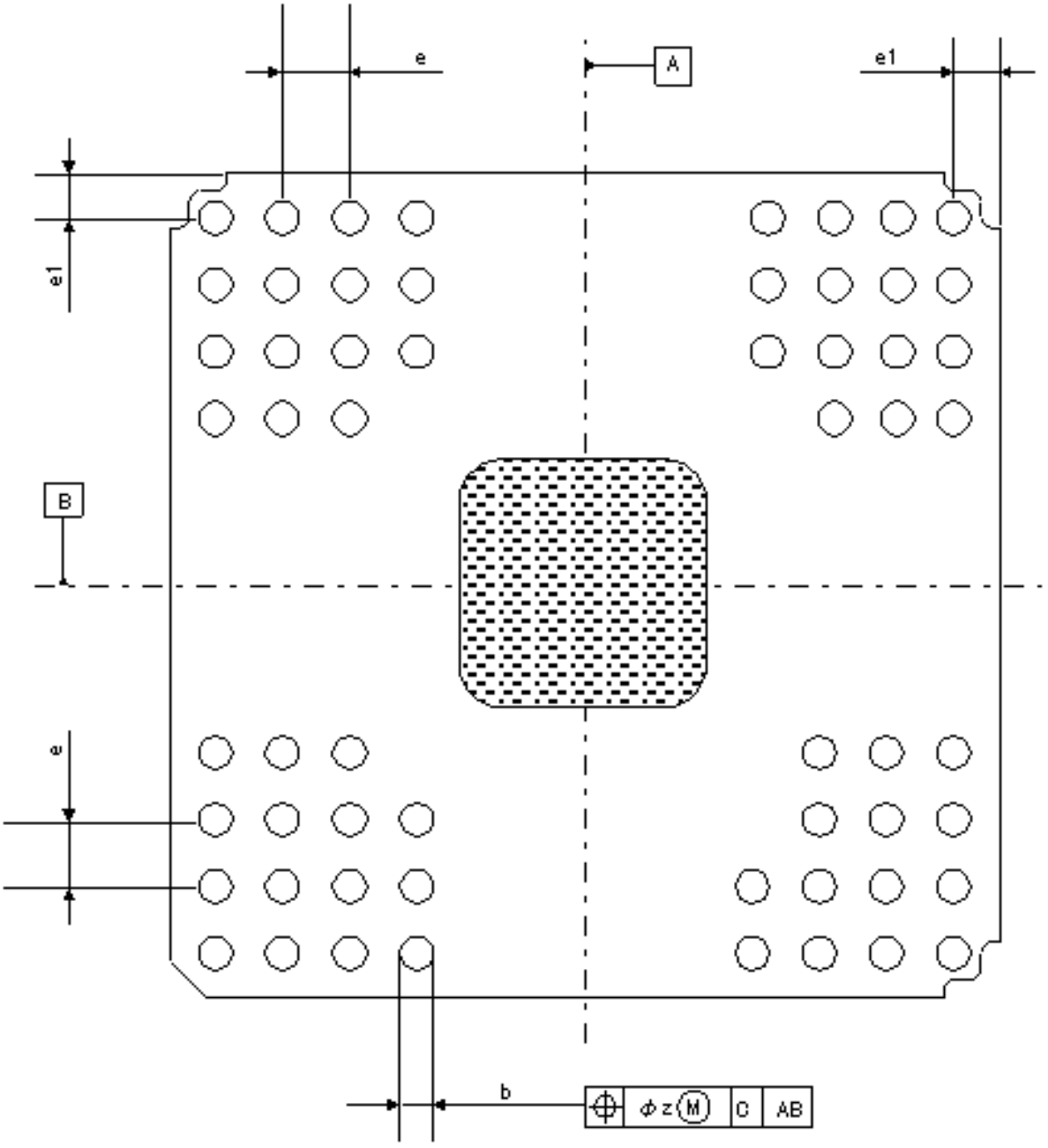


Figure 9-2 T-BGA256 Outline Dimensions Bottom view

Package Type (Package Code)	256TBGA T-BGA256-2727-1.27B4 Non Tie-Bar		
Symbol	millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0.5	0.6	0.7
A2	-	-	1.0
b	0.6	0.75	0.90
D	27.0 BSC		
D1	24.13 BSC		
D2	25.4	25.6	25.8
D3	14.8	15.0	15.2
D4	12.4	12.6	12.8
E	27.0 BSC		
E1	24.13 BSC		
E2	25.4	25.6	25.8
E3	14.8	15.0	15.2
E4	12.4	12.6	12.8
e	1.27 BSC		
s	0.635		
aaa	0.15		

10 REFERENCES

[1] ATM Forum UTOPIA Level 2 v1.0. Af-Phy-0039.000 June 1995

Appendix A. Revision

Rev	No	Section	Comment
1.0			Initial Draft
1.1		All	Reformatting and additional UTOPIA timing data

