TOSHIBA

TC220 Series CMOS ASIC Family

0.3µm, 3.3V ASICs

The 0.3µm drawn TC220 3.3V ASIC technology provides the density and performance needed for System IC designs.

Benefits

- 1.9M usable gates provide 2.6x density of previous generation technologies for applications where density is critical to survival.
- 111ps loaded nand gate delay for high performance systems
- High level cores for System IC implementation
- 3 ranges of macrocells for speed power optimization
- Technology libraries compatible with TC200 series ASIC family for ease of migration
- New accurate delay modeling ensuring system predictability
- Commercial EDA sign-off for flexibility
- Advanced 62µm TAB inner lead bonding provides double the I/O pads available on a die
- A wide range of packaging options available including BGA, TAB-BGA, heatspreader plastic, QFP, TAB-QFP, and others to suit all applications

Applications

The TC220 has been targeted at high end markets where density is critical to survival; set top boxes, handheld systems, high end workstation/servers, communications and advanced graphics.

NOTE 1: Family is available as: TC220G Gate Array, TC220E Embedded Array and TC190C Standard Cell.

TC220 Gate Array Product Summary

Reference	Usable Gates		I/O Pads		
	DLM	TLM	Wirebond Pads	TAB 62µm	TAB 83µm
TC220G06/56	82,000	144,000	128	248	184
TC220G08/58	103,000	182,000	144	288	212
TC220G10/60	125,000	220,000	160	316	236
TC220G12/62	152,000	267,000	176	348	260
TC220G14/64	181,000	315,000	192	380	284
TC220G16/66	211,000	385,000	208	420	312
TC220G20/70	266,000	462,000	240	—	360
TC220G24/74	342,000	593,000	272	—	408
TC220G32/82	485,000	846,000	336	—	504
TC220G36/86	625,000	1,070,000	384	—	576
TC220G40/90	791,000	1,378,000	432	—	648
TC220G42/92	1,110,000	1,934,000	512	—	768

Note: DLM=Double Layer Metal, TLM=Triple Layer Metal

System IC Application Support

The TC220 offers the ability to design System ICs with previously unabtainable levels of integration. With this density everything is effected. System architectures are not bound by the same physical constratints as before, cache may become just a memory and time to market gets ever smaller.

With 1.7M gates available there can be a paradigm shift in how designs are done; more than 1M gates is probably beyond the complexity of a mainframe computer design.

System level cores including an R3900 MIPS microprocssor, 8/16 bit CISC embedded controller, high density DRAM, MPEG and ATM. These advanced customized solutions are available through partnership designs.

Optimized Macrocell Performance

TC220 family has three ranges of macrocells for speed power optimization.

	Cell Type*		
	Normal	High Speed	Ultra Speed
Delay	225ps	151ps	111ps
Power	1.42W/MHz	1.86μW/MHz	2.73μW/MHz

* 2-input NAND, fanout = 2 plus typical interconnect load

High Performance I/O

TC220 is supported by a range of high performance I/O options including Analog PLL, PCI, high performance GTL, 3V failsafe and low undershot buffers,etc.

Accurate Models

TC220 series incorporates the new Toshiba highly accurate delay model which includes the following new features:

- Pin to pin type
- State Dependent Delay
- Table Look Up Delay
- Input Slew
- Non-Linear Equation

Delay model also includes effect of via resistance and inter-wire capacitance.

Commerical EDA Sign-off

TC220 series is supported by Toshiba's open EDA Strategy that is based on sign-off on multiple commercial EDA tools. This leads to the following benefits:

- Sign-off convenience at designer's site
- Shorter design cycle time
- Higher design efficiency
- Highly accurate simulation model
- Faster time-to-market

Initial support will be for Verilog-XL.

EDA Support

EDA support is available for most of the commercial EDA tools. For System IC designs Toshiba engineering will work with the customer to develop the EDA flow required for a given design.

In addition, Toshiba has a range of DFT suport including SCAN, Partial SCAN, BIST and boundary SCAN available.

Technology Resource Centers provide technical support and design expertise

Toshiba ASIC Technology Resource Centers are located throughout the U.S. and provide a high level of technical expertise for support before, during, and after the design of a Toshiba ASIC. This includes support issues dealing with EDA environments and design kits, Toshiba design methodologies, Toshiba ASIC technologies, and Toshiba ASIC design implementation. They are also available for design consultation.

In addition, Toshiba's North America Semiconductor Engineering Development Center based in San Jose, CA is staffed with system, technology and EDA design expertise to work with their partners on advanced System IC applications.

High quality, high volume manufacturing capability

Toshiba's ASIC manufacturing plants are among the largest and most advanced in the world. They are all certified to ISO9000. Rigorous production quality control and monitoring coupled with a sophisticated batch tracking system provides Toshiba with the ability to meet the requirements of fast ramping, high volume markets.

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