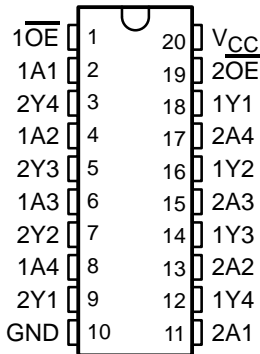


SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

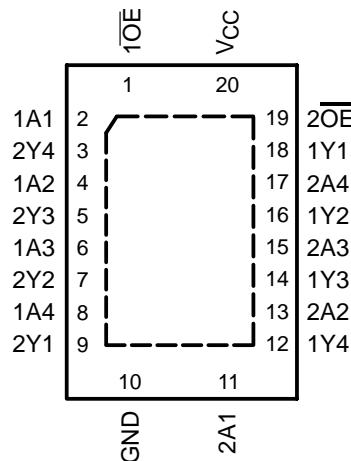
SCAS586I – DECEMBER 1996 – REVISED MAY 2003

- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Unregulated Battery Operation Down to 2.7 V
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

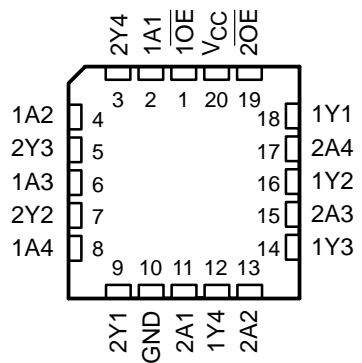
SN54LVTH244A . . . J OR W PACKAGE
SN74LVTH244A . . . DB, DW, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVTH244A . . . RGY PACKAGE
(TOP VIEW)



SN54LVTH244A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74LVTH244ARGYR	LXH244A
	SOIC – DW	Tube	SN74LVTH244ADW	LVTH244A
		Tape and reel	SN74LVTH244ADWR	
	SOP – NS	Tape and reel	SN74LVTH244ANSR	LVTH244A
	SSOP – DB	Tape and reel	SN74LVTH244ADBR	LXH244A
	TSSOP – PW	Tape and reel	SN74LVTH244APWR	LXH244A
-55°C to 125°C	VFBGA – GQN	Tape and reel	SN74LVTH244AGQNR	LXH244A
	CDIP – J	Tube	SNJ54LVTH244AJ	SNJ54LVTH244AJ
	CFP – W	Tube	SNJ54LVTH244AW	SNJ54LVTH244AW
	LCCC – FK	Tube	SNJ54LVTH244AFK	SNJ54LVTH244AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH244A, SN74LVTH244A
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCAS586I – DECEMBER 1996 – REVISED MAY 2003

description/ordering information (continued)

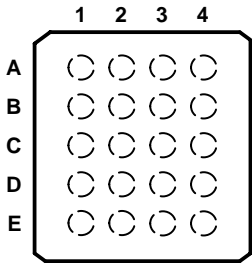
The 'LVTH244A devices are organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the devices pass data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

SN74LVTH244A . . . GQN PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4
A	1A1	$1\overline{OE}$	V_{CC}	$2\overline{OE}$
B	1A2	2A4	2Y4	1Y1
C	1A3	2Y3	2A3	1Y2
D	1A4	2A2	2Y2	1Y3
E	GND	2Y1	2A1	1Y4

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

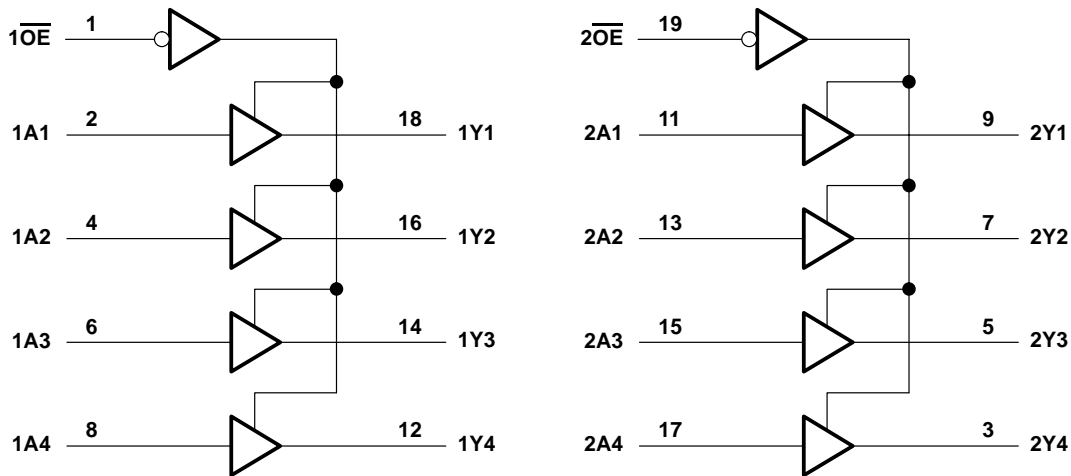
SN54LVTH244A, SN74LVTH244A

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCAS586I – DECEMBER 1996 – REVISED MAY 2003

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH244A	96 mA
SN74LVTH244A	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH244A	48 mA
SN74LVTH244A	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
(see Note 3): DW package	58°C/W
(see Note 3): GQN package	78°C/W
(see Note 3): NS package	60°C/W
(see Note 3): PW package	83°C/W
(see Note 4): RGY package	37°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LVTH244A, SN74LVTH244A

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCAS586I – DECEMBER 1996 – REVISED MAY 2003

recommended operating conditions (see Note 5)

			SN54LVTH244A		SN74LVTH244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μ s/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 5: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LVTH244A, SN74LVTH244A

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCAS586I – DECEMBER 1996 – REVISED MAY 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH244A			SN74LVTH244A			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}		V _{CC} = 2.7 V, I _I = −18 mA		−1.2			−1.2			V	
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = −100 μA		V _{CC} −0.2			V _{CC} −0.2			V	
		V _{CC} = 2.7 V, I _{OH} = −8 mA		2.4			2.4				
		V _{CC} = 3 V		I _{OH} = −24 mA							
				I _{OH} = −32 mA			2				
V _{OL}		V _{CC} = 2.7 V		I _{OL} = 100 μA		0.2			0.2		V
				I _{OL} = 24 mA		0.5			0.5		
		V _{CC} = 3 V		I _{OL} = 16 mA		0.4			0.4		
				I _{OL} = 32 mA		0.5			0.5		
				I _{OL} = 48 mA		0.55					
				I _{OL} = 64 mA					0.55		
I _I	Control inputs	V _{CC} = 0 or 3.6 V, V _I = 5.5 V		50			10			μA	
		V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1			±1				
	Data inputs	V _{CC} = 3.6 V		V _I = V _{CC}		1			1		
				V _I = 0		−5			−5		
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100			μA	
I _I (hold)	Data inputs	V _{CC} = 3 V		V _I = 0.8 V		75			75		μA
				V _I = 2 V		−75			−75		
		V _{CC} = 3.6 V‡, V _I = 0 to 3.6 V					500 −750				
I _{OZH}		V _{CC} = 3.6 V, V _O = 3 V		5			5			μA	
I _{OZL}		V _{CC} = 3.6 V, V _O = 0.5 V		−5			−5			μA	
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care		±100*			±100			μA	
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care		±100*			±100			μA	
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.39			0.19		mA
				Outputs low		14			5		
				Outputs disabled		0.39			0.19		
ΔI _{CC} §		V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.2			0.2			mA	
C _i		V _I = 3 V or 0		3			3			pF	
C _O		V _O = 3 V or 0		7			7			pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



SN54LVTH244A, SN74LVTH244A

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

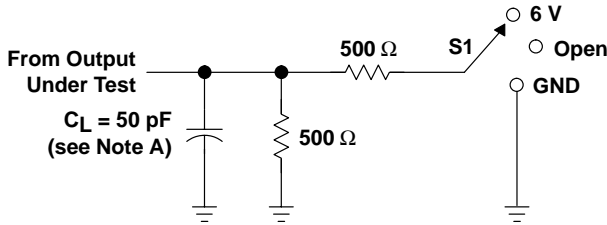
SCAS586I – DECEMBER 1996 – REVISED MAY 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

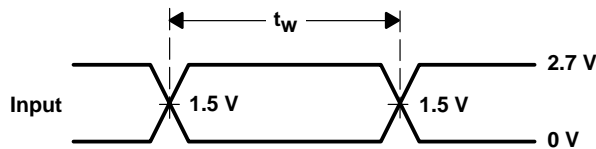
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH244A				SN74LVTH244A				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A	Y	0.5	3.8	4.1		1.1	2.3	3.5	3.8		ns
t _{PHL}			0.5	3.8	3.9		1.3	2.1	3.3	3.6		
t _{PZH}	OE	Y	0.8	5	6		1.1	2.5	4.5	5.3		ns
t _{PZL}			0.8	5	5.4		1.4	2.7	4.4	4.9		
t _{PHZ}	OE	Y	1.3	5.5	5.8		1.9	2.8	4.4	4.5		ns
t _{PLZ}			1.2	4.7	4.8		1.8	2.9	4.4	4.4		

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

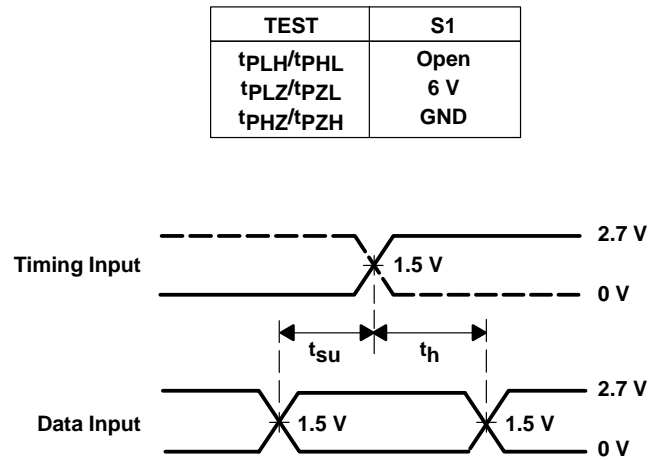
PARAMETER MEASUREMENT INFORMATION



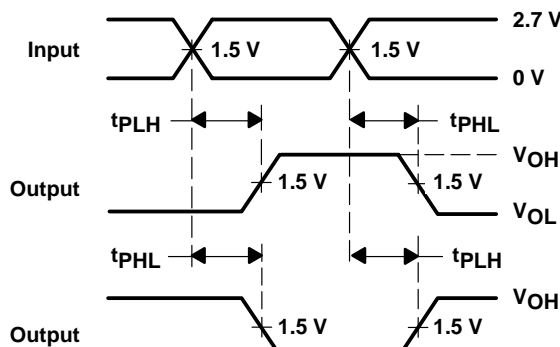
LOAD CIRCUIT



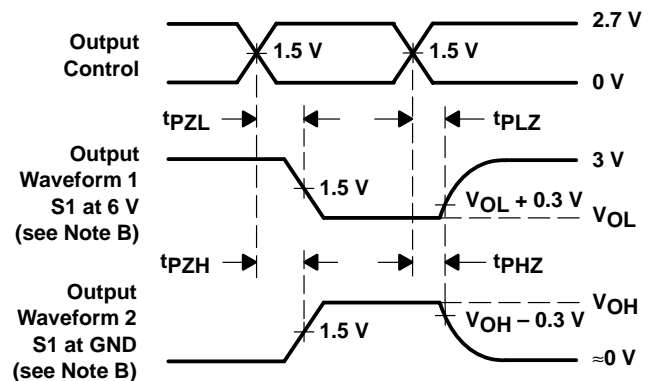
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

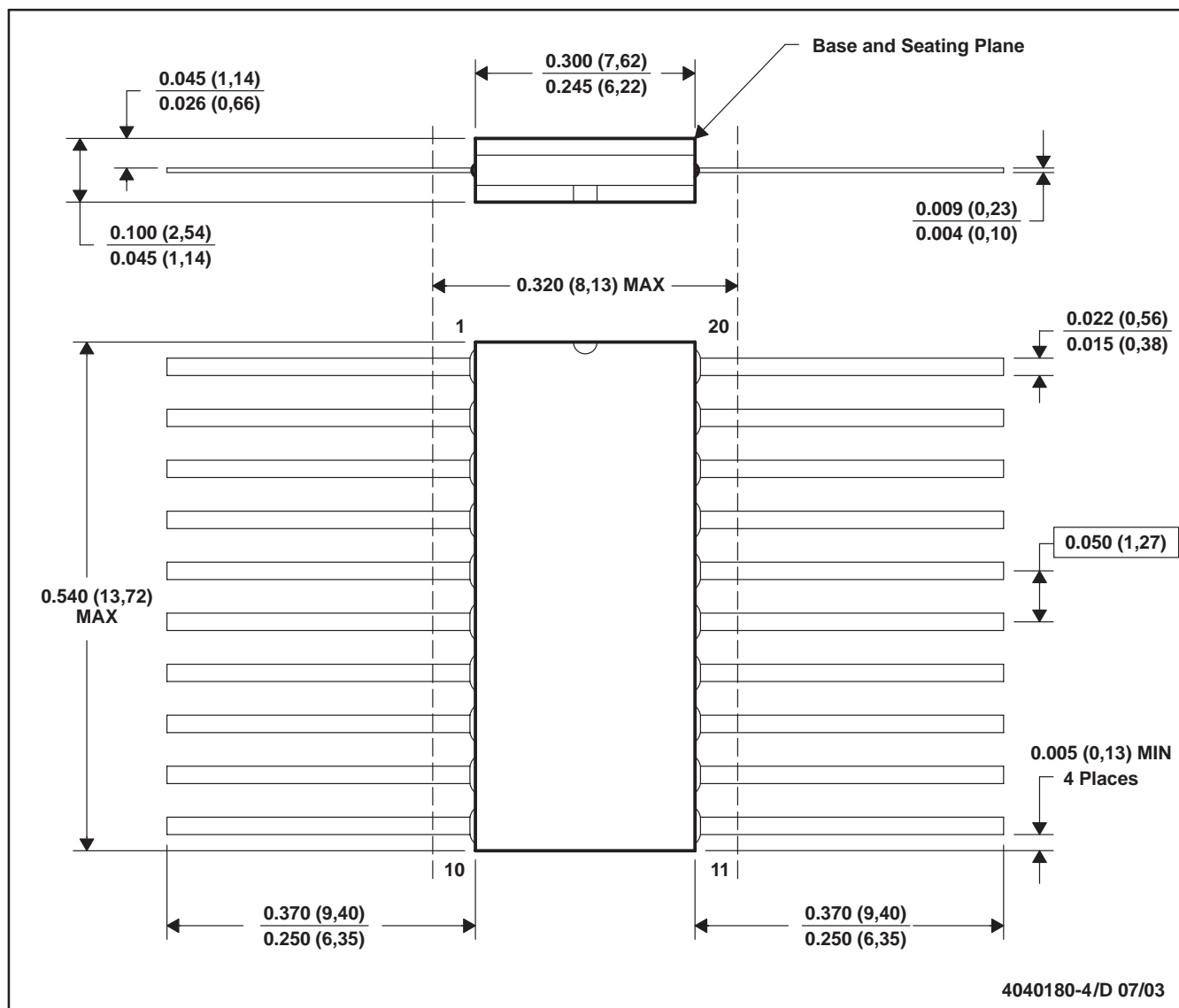


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

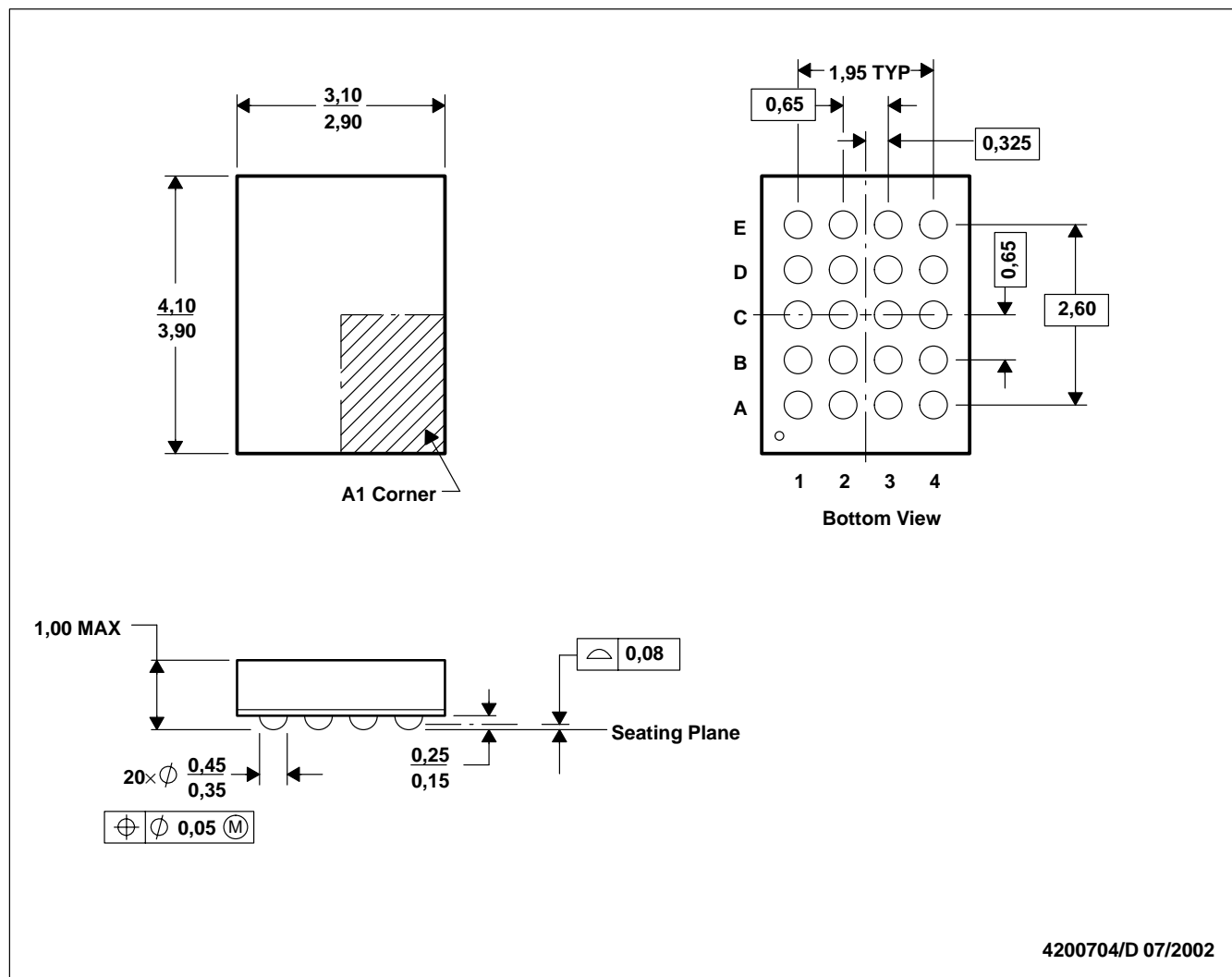
28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY

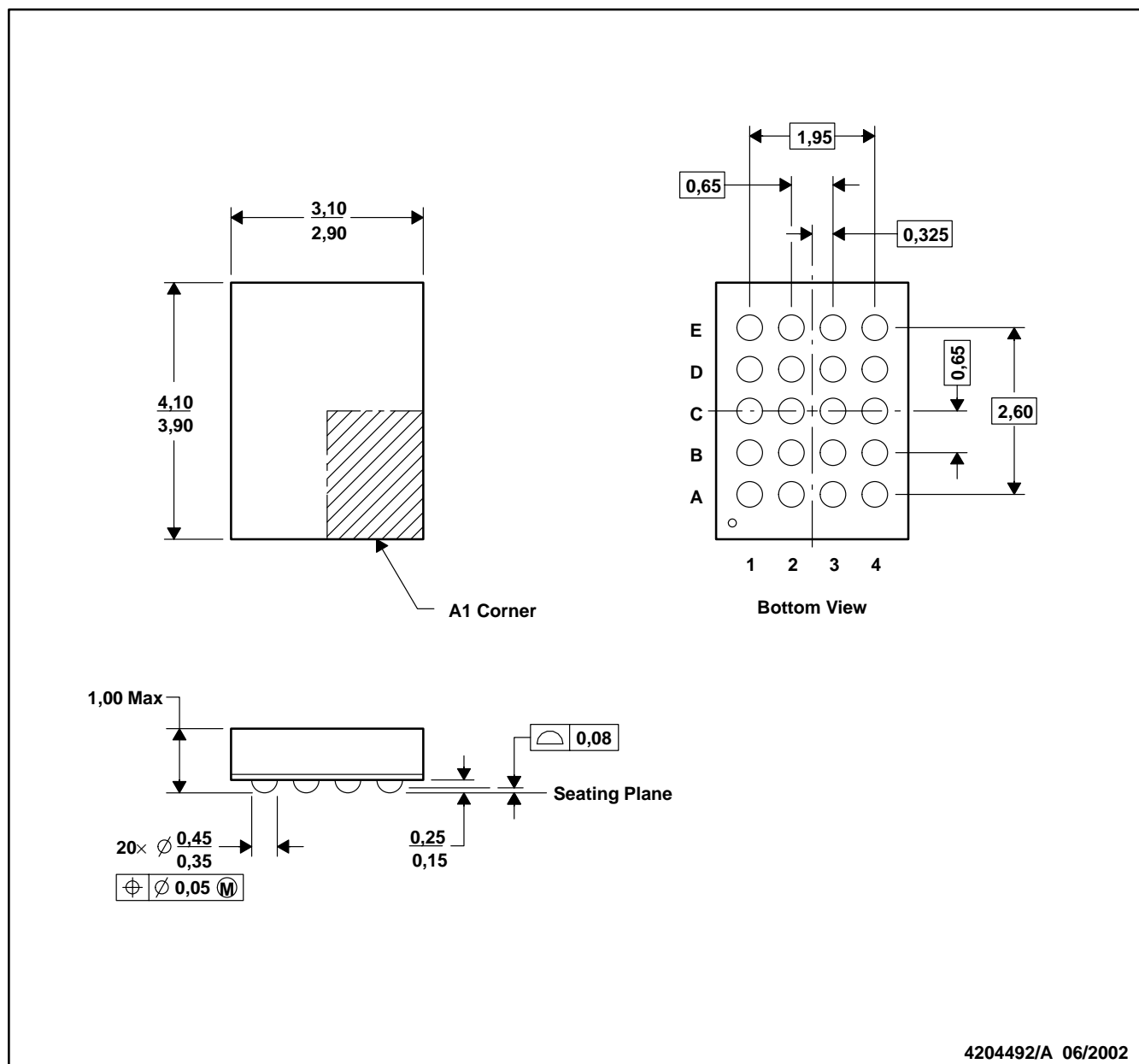


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ configuration
 - D. Falls within JEDEC MO-225 variation BC.
 - E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY

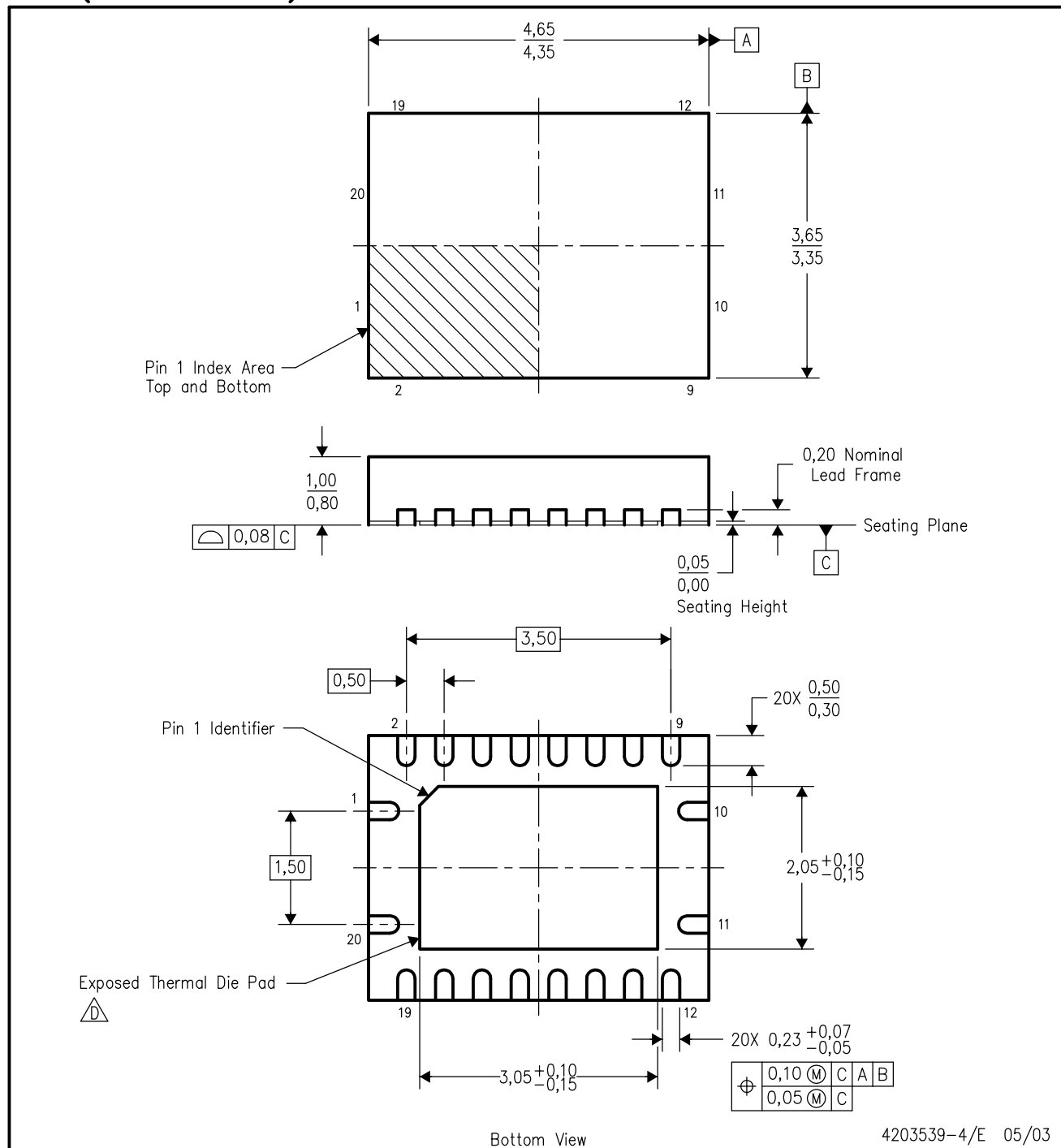


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ configuration.
 - D. Fall within JEDEC MO-225 variation BC.
 - E. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments.

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



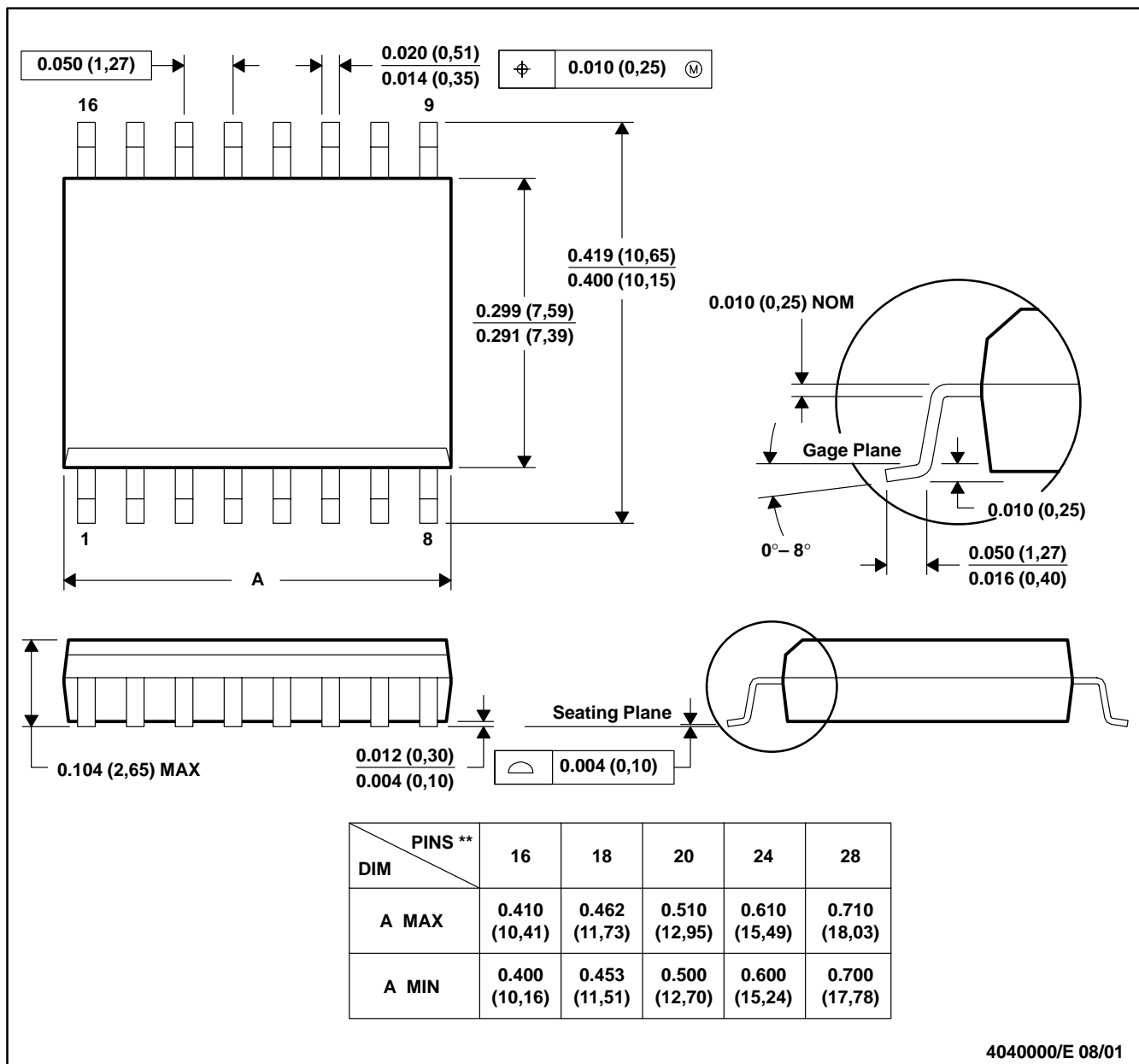
4203539-4/E 05/03

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - Package complies to JEDEC MO-241 variation BC.

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

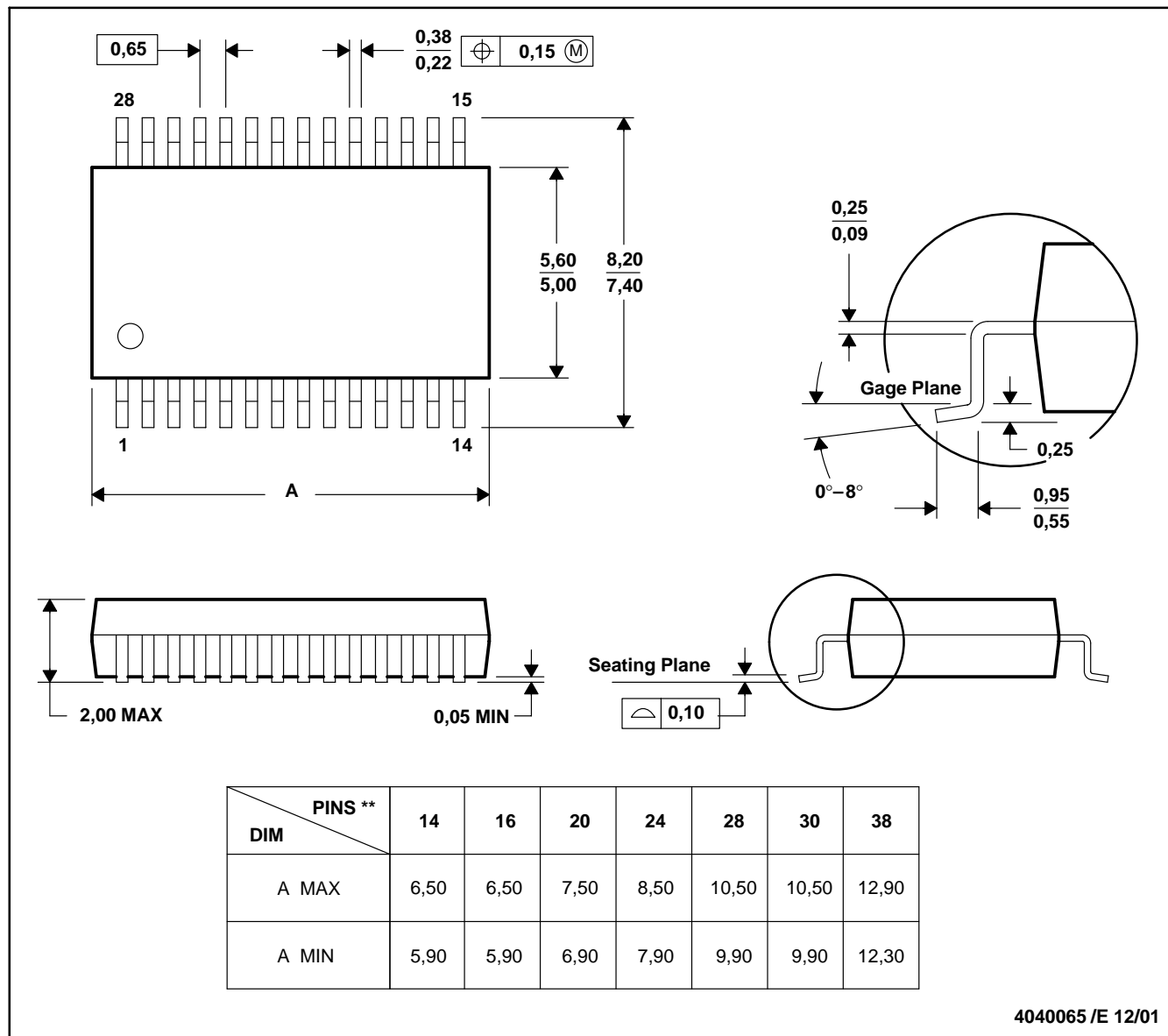


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

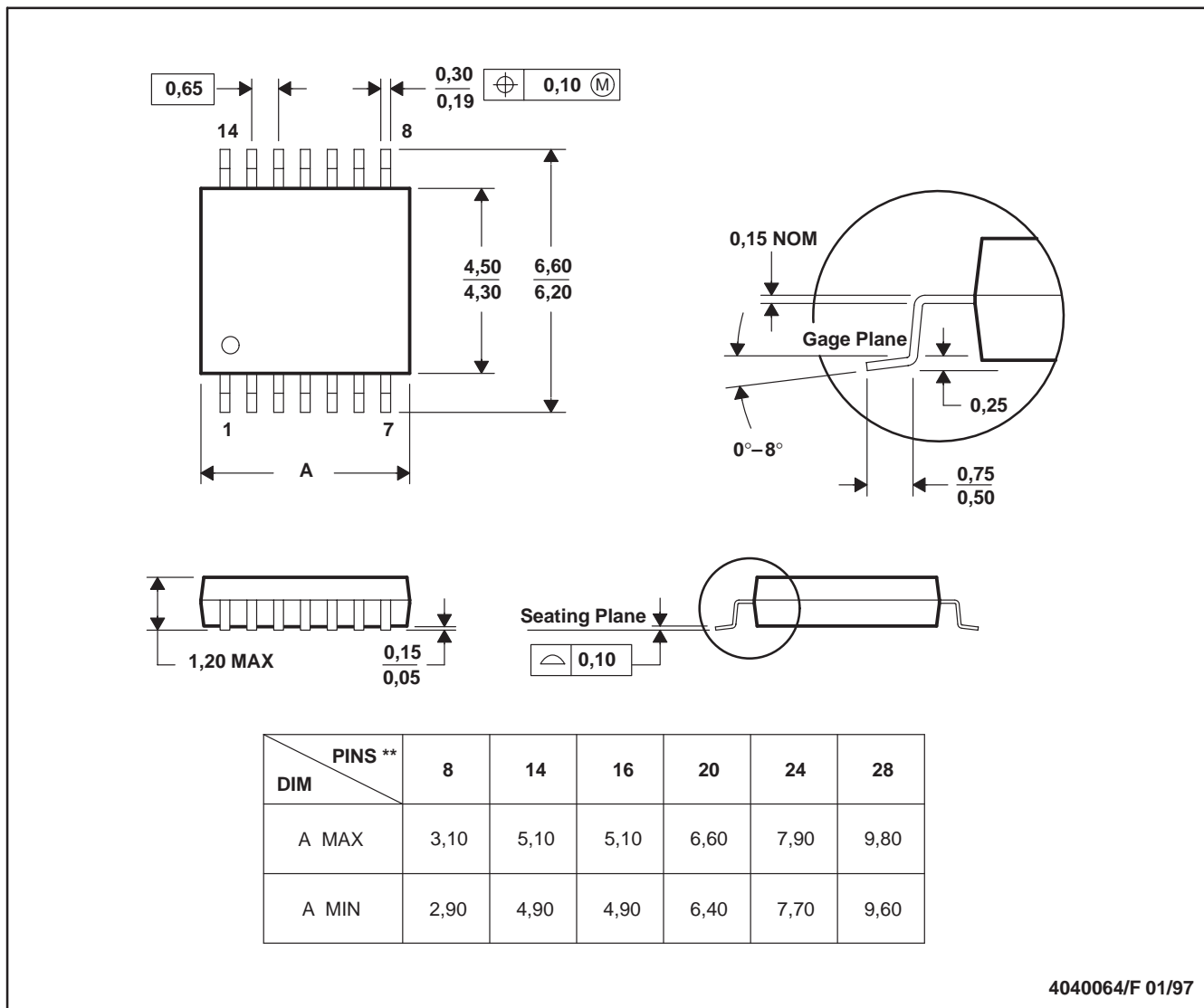


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated