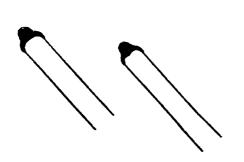
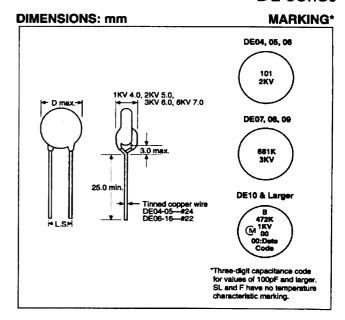
CERAMIC CAPACITORS MEDIUM VOLTAGE CAPACITORS 1KV to 6KVDC E.I.A. CLASS II & III



DE Series





PART NUMBERING SYSTEM

	TYPE DE04	LEADS 05	TEMP. CHAR. B	CAPACITA 101	ANCE TOL K T	. VOLTAGE	:
CAPACITOR TYPE AND SIZE	LEAD SPACING 05 = 5 07 = 7.5 10 = 10	Class I Class I TEMPE MAX. (B = ±10 E = +20	RATURE RANGE: -25°C CAP. CHANGE OVER TEM	ications. V to +85°C	ALUE	CAPACITANCE TOLERANCE J = ±5% K = ±10% Z = +80, -20%	VOLTAGE Identified by a one-digit numbe

*1KV - B

IVA - D	KV - B			
PART NUMBER	DIA (mm)	LS (mm)	CAP (pF)	
DE0405B101K1K	4.5	5	100	
DE0405B151K1K	4.5	5	150	
DE0405B221K1K	4.5	5	220	
DE0405B331K1K	4.5	5	330	
DE0505B471K1K	5	5	470	
DE0605B681K1K	6	5	680	
DE0605B102K1K	6	5	1000	
DE0805B152K1K	8	5	1500	
DE0905B222K1K	9	5	2200	
DE1005B332K1K	10	5	3300	
DE1205B472K1K	12	5	4700	
DE1510B682K1K	15	10	6800	

	_	-	•	•	v
	n	F	1	3	n

*3KV - B

DE 13 IUB 062K IK	10	1 10	6800
(V – B			
DE0405B101K2K	4.5	5	100
DE0405B151K2K	4.5	5	150
DE0405B221K2K	4.5	5	220
DE0505B331K2K	5	5	330
DE0605B471K2K	6	5	470
DE0705B681K2K	7	5	680
DE0805B102K2K	8	5	1000
DE0905B152K2K	9	5	1500
DE1005B222K2K	10	5	2200
DE1205B332K2K	12	5	3300
DE1510B472K2K	15	10	4700

PART NUMBER	DIA (mm)	LS (mm)	CAP (pF)
DE0507B101K3K	5	7.5	100
DE0507B151K3K	5	7.5	150
DE0507B221K3K	5	7.5	220
DE0607B331K3K	6	7.5	330
DE0707B471K3K	7	7.5	470
DE0807B681K3K	8	7.5	680
DE0907B102K3K	9	7.5	1000
DE1107B152K3K	11	7.5	1500
DE1307B222K3K	13	7.5	2200
DE1510B332K3K	15	10	3300

DKV - B			
DE0910B101K6K	9	10	100
DE0910B151K6K	9	10	150
DE0910B221K6K	9	10	220
DE0910B331K6K	9	10	330
DE1010B471K6K	10	10	470
DE1110B681K6K	11	10	680
DE1310B102K6K	13	10	1000

CERAMIC CAPACITORS MEDIUM VOLTAGE CAPACITORS 1KV to 6KVDC E.I.A. CLASS II & III

wuRata

DE Series

1KV – E			
DE0505E102Z1K	5	5	1000
DE0705E222Z1K	7	5 5	2200
DE0905E472Z1K	9	5	4700
DE1307E103Z1K	13	7.5	10000
2KV – E			
DE0605E102Z2K	6	5	1000
DE0805E222Z2K	8	5	2200
DE1105E472Z2K	11	5	4700
DE1610E103Z2K	16	10	10000
3KV – E			
DE0707E102Z3K	7	7.5	1000
DE1007E222Z3K	10	7.5	2200
DE1307E472Z3K	13	7.5	4700
6KV - E			
DE1110E102Z6K	11	10	1000
DE1510E222Z6K	15	10	2200
IKV – F			
DE0605F222Z1K	6	5	2200
DE0705F472Z1K	7	5	4700
DE1005F103Z1K	10	5	10000
2KV – F		- · · · · · · · · · · · · · · · · · · ·	
DE0505F102Z2K	5	5	1000
DE0705F222Z2K	7	5	2200
DE0905F472Z2K	9	5	4700
DE1205F103Z2K	12	5	10000

SPECIFICATIONS: CLASS II & III

Test Conditions: Unless otherwise specified, measurements shall be made at $\pm 25^{\circ}$ C, $\pm 10^{\circ}$ C, a relative humidity no greater than 75%, and normal atmospheric pressure.

Capacitance: Capacitance shall be within the specified limits when measured at, or corrected to, a temperature of +20°C, a RMS voltage between .05 and 5.0, and a frequency of 1KHz.

Dissipation Factor, or (Ratio of Equivalent Series Resistance to Reactance): Dissipation Factor shall not be greater than 2.5% for B and E characteristics, or greater than 5% for F.

Insulation Resistance: $10,000M\Omega$ minimum when measured between terminals of capacitor 1 minute after application of a DC test voltage of 500 applied through a protective resistance which will limit the charging current to 50mA.

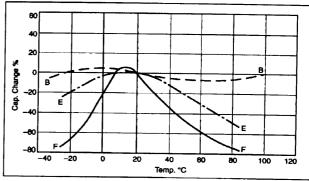
Dielectric Strength: Capacitors shall be subjected to a DC voltage equal to 200% of their rated working voltage. This voltage shall be applied for 5, ± 1 seconds through a protective resistance that will limit the charging current to 50mA.

Humidity Resistance: After exposure for a period of 500 hours to an atmosphere of 95% relative humidity at a temperature of 40°C, capacitor shall have a minimum insulation resistance of 1,000MΩ.

Life: Capacitors shall be subjected to a DC voltage equal to 150% of the rated working voltage for 1,000 hours at +85°C. After this test, dissipation factor shall not be more than twice the stated initial value, and insulation resistance shall not be less than 2,000MΩ.

Encapsulation: Ceramic disc is coated in an epoxy resin which conforms to UL94V-0.

TYPICAL TEMPERATURE CHARACTERISTICS



The structure of the "Global Part Numbers" that have been adopted since June 2001 and the meaning of each code are described herein. If you have any questions about details, inquire at your usual Murata sales office or distributor.

Part Numbering

High Voltage Ceramic Capacitors (250V-6.3kV)

(Global Part Number) DE B B3 3A 102 K N2 A

Product ID

Product ID	
DE	High-voltage (250V - 6.3kV) / Safety Standard Recognized Ceramic Capaictors

Series Category

Code	Outline	Contents
A		Class1 (char. SL) DC1-3.15kV Rated
В		Class2 DC1-3.15kV Rated
С	High-Voltage	Class 1,2 DC6.3kV Rated
н		High Temperature Guaranteed, Low-dissipation Factor (char. R, C)

First three digit (●Product ID and ●Series Category) express "Series Name".

Temperature Characteristics

	124 1 2 1 3		
Code	Temperature Characteristics	Cap.Change or Temp. Coeff.	Temperature Range
В3	В	±10%	
E3	E	+20%,-55%	–25 to +85℃
F3	F	+30%,-80%	
C3	С	±20%	–25 to +85℃
	C	+15%,-30%	+85 to +125℃
R3	J	±15%	–25 to +85℃
N3	R	+15%,-30%	+85 to +125℃
1X	SL	+350 to −1000ppm/℃	+20 to +85℃

• Rated Voltage

Code	Rated Voltage
2E	DC250V
2H	DC500V
3 A	DC1kV
3D	DC2kV
3F	DC3.15kV
3 J	DC6.3kV

Capacitance

Expressed by three figures. The unit is pico-farad(pF). The first and second figures are significant digits, and the third figure expresses the number of zeros which follow the two numbers. If there is a decimal point, it is expressed by the capital letter "R". In this case, all figures are significant digits.

6Capacitance Tolerance

Code	Capacitance Tolerance
J	±5%
K	±10%
Z	+80%, -20%

Lead Style

	Lead	Dimensions(mm)			
Code	Style	Lead Spacing	Lead Diameter	Pitch of Components	
A2	Vertical Crimp Long	5	ø0.6±0.05	_	
А3		7.5			
A4		10			
B2	Vertical Crimp	5	ø0.6±0.05	_	
В3		7.5			
B4	Short	10			
C1	Straight Long	5	ø0.5±0.05		
С3		7.5	ø0.6±0.05	_	
C4		10			
CD		7.5	ø0.5±0.05	1	
D1	Straight Short	5	ø0.5±0.05		
D3		7.5	ø0.6±0.05] –	
DD		7.5	ø0.5±0.05	1	
N2	Vertical Crimp Taping	5		12.7	
N3		7.5	ø0.6±0.05	15	
N7		7.5		30	
P2	Straight	5	-0.610.05	12.7	
Р3	Taping	7.5	ø0.6±0.05	15	

Packaging

Code	Packaging
Α	Ammo Pack
В	Bulk

■SPECIFICATION AND TEST METHOD

Item		m	Specification Temp. Compensating High Dielectric Constant		Testing Method	
				High Dielectric Constant		
1			_25 to +85℃	−25 to +85℃	The capacitance shall be measured at 20°C with 1±0.2kH	
2	2 Capacitance		Within the specified tolerance.	Within the specified tolerance.	(SL: 1±0.2MHz) and 5Vrms max.	
3	Dissipatio	Q on Factor (D. F.)	SL C≥30pF : Q≥1000 C<30pF : Q≥400+20C¹)	B, E D. F.≤2.5% F D. F.≤5.0%	Same condition as capacitance.	
4	Insulation Resistance (I. R.)	Between Lead wires	10000MΩ min.	10000MΩ min.	The insulation resistance shall be measured with 500±50VD within 60±5 sec. of charging.	
		Between Lead wires	No failure.	No failure.	The capacitors shall not be damage when DC voltage of 200% of the rated voltage are applied between the lead wires for 1 to 5 sec. (Charge/discharge current≤50mA)	
5	Dielectric Strength	Body Insulation	No failure.	No failure.	The capacitor is placed in the container with metal balls of diameter 1mm so that each lead wire, shortcircuited, is kept approximately 2mm off the balls as shown in the figure, and DC voltages of 1.3kV is applied for 1 to 5 sec. between capacitor lead wires and small metals. (Charge / discharge current≤50mA)	
				T.C. Cap. Change	The capacitance measurement shall be made at each ste specified in table. Capacitance change from the value of step 3 shall not exceed the limit specified.	
6	Temperature Ci	neracteristic	T. C. Temp. Coefficient	B within±10%	Step 1 2 3 4 5 20±2° -25±3° 20±2° 85±2° 20±2°	
-			SL +350 to -1000pm/°C	E within + 30%		
			(Temp. Range : +20 to +85℃)	F within=80%	Pre-treatment: Capacitor shall be stored at 85±2°c for 1 hour, then placed at ²⁾ room condition for 24±2 hours before initial measurements. (B,E,F)	
		Appearance	No marked defect.	No marked defect.	The capacitor shall firmly be soldered to the supporting le	
7	Vibration	Capacitance	Within the specified tolerance.	Within the specified tolerance.	wire and vibration which is 10 to 55Hz in the vibration frequency range, 1.5mm in total amplitude, and about 1	
1	Resistance	Q.	C≥30pF : Q≥1000	B, E D. F.≤2.5%	minute in the rate of vibration change from 10Hz to 55Hz	
		D. F.	SL C<30pF : Q≥400+20C¹)	F D. F.≤5.0%	and back to 10Hz is applied for a total of 6 hours; 2 hours each in 3 mutually perpendicular directions.	
		Appearance	No marked defect.	No marked defect.	The lead wire shall be immersed into the melted solder of	
				B within±5%	350±10℃ (Body of ¢5 and under : 270±5℃) up to about 1 to 2mm from the main body for 3.5±0.5 sec. (Body of ¢5	
		Capacitance	SL within±2.5%	E within±15%	and under: 5±0.5sec.).	
	1,37	Change		F within±20%	Pre-treatment : Capacitor shall be stored at 85±2°c for 1	
8	Soldering				hour, then placed at 2) room condition for	
	Effect	Dielectric			24±2 hours before initial measurements. (B,E,F)	
	100	Strength		S	Post-treatment : Capacitor shall be stored for 1 to 2 hours	
	1 3 to 1 150a	(Between lead	Pass the item No. 5.	Pass the item No. 5.	2) room condition. (SL)	
	Tenuni yan iyo	wires)			Post-treatment : Capacitor shall be stored for 24±2 hours at	
-		Appearance	No marked defect.	No marked defect.	2) room condition. (B,E,F) Set the capacitor for 500 ±24 hours at 40±2°C in 90 to 95%	
				B within±10%	humidity.	
		Capacitance	St. within±5%	E within±20%	Pre-treatment : Capacitor shall be stored at 85±2°C for 1	
9	Humidity (Under Steady	Change		F within±30%	hour, then placed at ²⁾ room condition for 24±2 hours before initial measurements.	
•	State)	Q.	C≥30pF : Q≥350	B, E D. F.≤5.0%	(B,E,F)	
	1976	D. F.	SL C<30pF : Q≥275+ ½ C¹)	F D. F.≤7.5%	Post-treatment : Capacitor shall be stored for 1 to 2 hours	
	la la tata .	I.R.	1000MΩ min.	1000MΩ min.	²⁾ room condition.	
		Appearance	No marked defect.	No marked defect.	Apply the rated voltage for 500 ⁺²⁴ hours at 40±2℃ in 90 t	
					95% humidity.	
	4.40	Capacitance		8 within±10%	(Charge / discharge current≤50mA)	
10	Humidity	Change	SL within±7.5%	F within±20% F within±30%	Pre-treatment: Capacitor shall be stored at 85±2℃ for 1 hour, then placed at ²⁾ room condition for 24±2 hours before initial measurements.	
	Loading		C>20-E . O>200	D.E. CEON	(B,E,F)	
		Q D.F.	C≥30pF : Q≥200 C<30pF : Q≥100+ ¹⁰ / ₃ C¹)	B, E D. F.≤5.0% F D. F.≤7.5%	Post-treatment: Capacitor shall be stored for 1 to 2 hours 2) room condition. (SL)	
		Tarit, tuparsiyes			Post-treatment : Capacitor shall be stored at 85±2°C for 1	
		I.R.	500MΩ min.	500MΩ min.	hour, then placed at 2) room condition for	
4.5		Appearance	No marked defect.	No marked defect.	24±2 hours. (B,E,F) Apply a DC voltage of 150% of the rated voltage for 1000 ⁺⁴	
					hours at 85±2°C.	
		Capacitance		B within±10%	(Charge/discharge current≤50mA)	
		Change	SL within±3%	E within±20%	Pre-treatment : Capacitor shall be stored at 85±2°c for 1 hour, then placed at ²⁾ room condition for	
	 I z z z z z z z z z z z z z z z z z z z			F within±30%	nour, then placed at 2 room condition for 24±2 hours before initial measurements.	
			0.00 = 0.00		(B,E,F)	
11	Life		C≥30pF : Q≥350 C<30pF : Q≥275+ ½C1)	B E D. F.≤4.0% F D. F.≤7.5%	Pos-treatment : Capacitor shall be stored for 1 to 2 hours a	
11	Life	Q		F D. F.≤7.5%	2) room condition. (SL) Pos-treatment: Capacitor shall be stored at 85±2°c for 1	
11	Life	Q D. F.	0 (00pr : Q=2701 20			
11	Life	D.F.	Violation, and the second seco		hour, then placed at 2) room condition for	
11	Life	Q D. F.	2000MΩ min.	2000MΩ min.		
11	Life	D.F.	Violation, and the second seco	2000MΩ min.	hour, then placed at ²⁾ room condition for 24±2 hours. (B,E,F) As a figure, fix the body of capacitor, apply a	
11	Life	D.F.	Violation, and the second seco	2000M Ω min.	hour, then placed at ²⁾ room condition for 24±2 hours. (B,E,F) As a figure, fix the body of capacitor apply a tensile weight gradually to each lead wire in	
11	Life	D.F.	Violation, and the second seco	2000M Ω min.	hour, then placed at ²⁾ room condition for 24±2 hours. (B.E.F) As a figure, fix the body of capacitor apply a tensile weight gradually to each lead wire in the radial direction of capacitor up to 10N	
	Life	D.F.	Violation, and the second seco		hour, then placed at ²⁾ room condition for 24±2 hours. (B,E,F) As a figure, fix the body of capacitor, apply a tensile weight gradually to each lead wire in the radial direction of capacitor up to 10N (1.0kgf) 5N (0.51kgf) for Lead diameter e	
11		D.F.	2000MΩ min.	ot cut off.	hour, then placed at ²⁾ room condition for 24±2 hours. (B,E,F) As a figure, fix the body of capacitor apply a tensile weight gradually to each lead wire in the radial direction of capacitor up to 10N (1.0kgf) 5N (0.51kgf) for Lead diameter e 0.5.), and keep it for 10±1 sec. Each lead wire shall be subjected to 5N (0.51kgf) 2.5N	
	Strength	D.F. I.R. Pull	2000MΩ min. Lead wire shall no	ot cut off.	hour, then placed at ²⁾ room condition for 24±2 hours. (B,E,F) As a figure, fix the body of capacitor apply a tensile weight gradually to each lead wire in the radial direction of capacitor up to 10N (1.0 kgh 5N (0.51 kgh for Lead diameter e 0.5), and keep it for 10±1 sec. Each lead wire shall be subjected to 5N (0.51 kgh) 2.5N (0.25 kgh for Lead diameter e 0.5) weight and then a 90°	
	Strength	D.F.	2000MΩ min. Lead wire shall no	ot cut off.	hour, then placed at ²⁾ room condition for 24±2 hours. (B,E,F) As a figure, fix the body of capacitor, apply a tensile weight gradually to each lead wire in the radial direction of capacitor up to 10N (1.0kgf) 5N (0.51kgf) for Lead diameter • 0.5), and keep it for 10±1 sec. Each lead wire shall be subjected to 5N (0.51kgf) 2.5N (0.25kgf) for Lead diameter • 0.5) weight and then a 90° bend, at the point of egress, in one direction, return to	
	Strength	D.F. I.R. Pull	2000MΩ min. Lead wire shall no	ot cut off.	hour, then placed at ²⁾ room condition for 24±2 hours. (B,E,F) As a figure, fix the body of capacitor,apply a tensile weight gradually to each lead wire in the radial direction of capacitor up to 10N (1.0kgf) 5N (0.51kgf) for Lead diameter e 0.5.), and keep it for 10±1 sec. Each lead wire shall be subjected to 5N (0.51kgf) 2.5N (0.25kgf) for Lead diameter e0.5) weight and then a 90° bend, at the point of egress, in one direction, return to original position, and then a 90° bend in the opposite	
	Strength	D.F. I.R. Pull	2000MΩ min. Lead wire shall no Capacitor shall no	ot cut off. It be broken.	hour, then placed at ²⁾ room condition for 24±2 hours. (B,E,F) As a figure, fix the body of capacitor apply a tensile weight gradually to each lead wire in the radial direction of capacitor up to 10N (1.0kgf) 5N (0.51kgf) for Lead diameter ø 0.5.) and keep it for 10±1 sec. Each lead wire shall be subjected to 5N (0.51kgf) 2.5N (0.25kgf) for Lead diameter ø 0.5) weight and then a 90° bend, at the point of egress, in one direction, return to original position, and then a 90° bend in the opposite direction at the rate of one bend in 2 to 3 seconds.	
	Strength	D. F. I. R. Pult Bending	2000MΩ min. Lead wire shall no	ot cut off. It be broken.	hour, then placed at ²⁾ room condition for 24±2 hours. (B,E,F) As a figure, fix the body of capacitor, apply a tensile weight gradually to each lead wire in the radial direction of capacitor up to 10N (1.0kgf) 5N (0.51kgf) for Lead diameter e 0.5), and keep it for 10±1 sec. Each lead wire shall be subjected to 5N (0.51kgf) 2.5N (0.25kgf) for Lead diameter é 0.5) weight and then a 90° bend, at the point of egress, in one direction, return to original position, and then a 90° bend in the opposite direction at the rate of one bend in 2 to 3 seconds.	

^{1) &}quot;C" expresses nominal capacitance value (pF) .
2) "room condition" temperature : 15 to 35°C, humidity : 45 to 75%, atmospheric pressure : 86 to 106kPa

1. Operating Voltage

When DC-rated capacitors are to be used in AC or ripple current circuits, be sure to maintain the Vp-p value of the applied voltage or the Vo-p which contains DC bias within the rated voltage range.

When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use a capacitor within rated voltage containing these irregular voltage.

When using the low-dissipation DEA/DEH series in a high-frequency and high-voltage circuit, be sure to read the instructions in item 4.

Voltage	DC Voltage	DC+AC Voltage	AC Voltage	Pulse Voltage (1)	Pulse Voltage (2)
Positional measurement	Vo-p	Vo-p	Vp-p	Vp-p	Vp-p

2. Operating Temperature and Self-generated Heat Keep the surface temperature of a capacitor below the upper limit of its rated operating temperature range. Be sure to take into account the heat generated by the capacitor itself. When the capacitor is used in a highfrequency current, pulse current or the like, it may have the self-generated heat due to dielectric-loss. The allowable frequency should be in less than 300kHz in sine wave. Applied voltage should be the load such as self-generated heat is within 5 °C in case of temperature characteristic SL and within 20°C for other temperature characteristic on the condition of atmosphere temperature 25 °C. When measuring, use a thermocouple of small thermal capacity-K of ø0.1mm and be in the condition where capacitor is not affected by radiant heat of other components and wind of surround-

(Never attempt to perform measurement with the cooling fan running. Otherwise, accurate measurement cannot be ensured.)

Before using the low-dissipation DEA/DEH series, be sure to read the instructions in item 4.

3. Fail-Safe

When capacitor would be broken, failure may result in a short circuit. Be sure to provide an appropriate fail-safe function like a fuse on your product if failure would follow an electric shock, fire or fume.

Continued on the following page.



4. Load Reduction and Self-generated Heat During Application of High-frequency and High-voltage Since the heat generated by the low-dissipation capacitor itself is low, its allowable power is much higher than the general B characteristic. However, in case such an applied load that the self-heating temperature is 20°C at the rated voltage, the allowable power may be exceeded. Therefore, when using the DEA/DEH series in a highfrequency and high-voltage circuit with a frequency of 1kHz or higher, make sure that the Vp-p values including the DC bias, do not exceed the applied voltage value specified in Table 1. Also make sure that the self-heating temperature (the difference

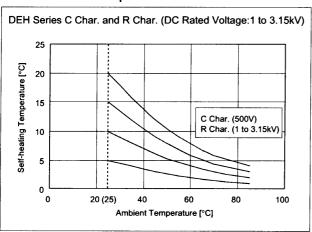
<Table 1> Allowable Conditions at High-frequency

between the capacitor's surface temperature and the

Series	Temp. Char.	DC Rated Voltage	Allowab at High	Operating		
			Applied Voltage (Max.)	Self-heating Temp. (25°C Ambient Temp.) *1	Environment Temp. *2	
DEH	R	250V	250Vp-p	10°C Max.		
	С	500V	500Vp-p	20°C Max.		
	R	1kV	800Vp-p	20°C Max.	-25 to +85°C	
			1000Vp-p	5°C Max.		
		2kV	1400Vp-p	20°C Max.		
			2000Vp-p	5°C Max.		
		3.15kV	1600Vp-p	20°C Max.		
			3150Vp-p	5°C Max.		
DEA	SL	1kV	1000Vp-p			
		SL 2kV	2000Vp-p	5°C Max.		
		3.15kV	3150Vp-p			

^{*1} Fig. 1 shows the relationship between the applied voltage and the allowable selfheating temperature regarding 1 to 3.15kV rated voltage of the DEH series R characteristic

<Fig. 2> Dependence of Self-heating Temperature on **Ambient Temperature**

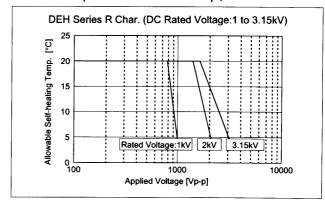


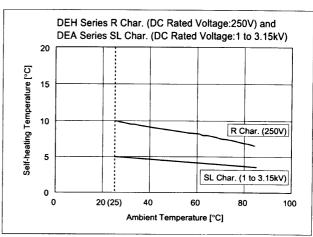
capacitor's ambient temperature) at an ambient temperature of 25°C does not exceed the value specified in Table 1.

As shown in Fig. 2, the self-heating temperature depends on the ambient temperature. Therefore, if you are not able to set the ambient temperature to approximately 25°C, please contact our sales representatives or product engineers.

Failure to follow the above cautions (item 1 to 4) may result, worst case, in a short circuit and cause fuming or partial dispersion when the product is used.

<Fig. 1> Relationship Between Applied Voltage and Self-heating Temperature (Allowable Self-heating Temp. at 25°C Ambient Temp.)





^{*2} When the ambient temperature is 85 to 125°C, the applied voltage needs to be further reduced. If the DEA/DEH series needs to be used at an ambient temperature of 85 to 125°C, please contact our sales representatives or product

^{*3} Fig. 3 shows reference data on the allowable voltage-frequency characteristic for a sine wave voltage.

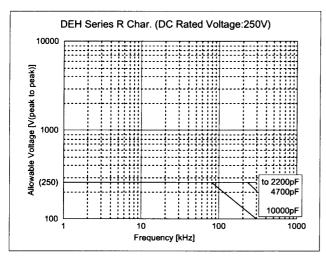
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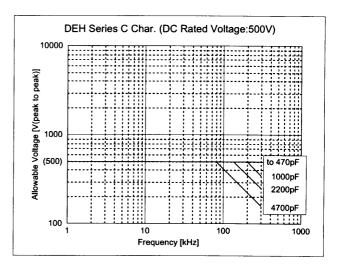
Because of the influence of harmonics, when the applied voltage is a rectangular wave or pulse wave voltage (instead of a sine wave voltage), the heat generated by the capacitor

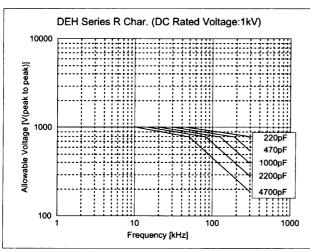
is higher than the value obtained by application of the sine wave with the same fundamental frequency.

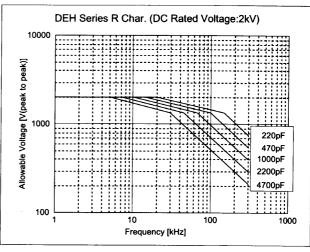
Roughly calculated for reference, the allowable voltage for a rectangular wave or pulse wave corresponds approximately

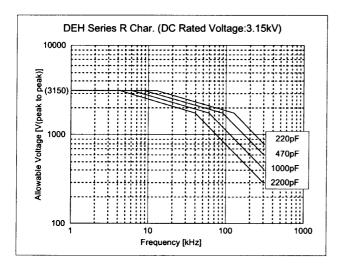
<Fig. 3> Allowable Voltage (Sine Wave Voltage) - Frequency Characteristic (At Ambient Temperature of 85°C or less) to the allowable voltage for a sine wave whose fundamental frequency is twice as large as that of the rectangular wave or pulse wave. This allowable voltage, however, varies depending on the voltage and current waveforms. Therefore, you are requested to make sure that the selfheating temperature is not higher than the value specified in Table 1.









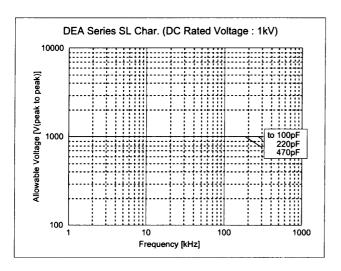


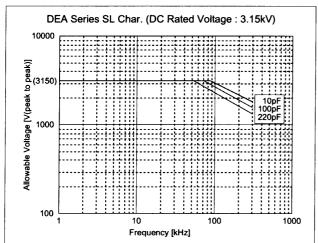
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<Fig. 3 (continue)> Allowable Voltage (Sine Wave Voltage) -Frequency Characteristic (At Ambient Temperature of 85°C or less)

Because of the influence of harmonics, when the applied voltage is a rectangular wave or pulse wave voltage (instead of a sine wave voltage), the heat generated by the capacitor is higher than the value obtained by application of the sine wave with the same fundamental frequency.

Roughly calculated for reference, the allowable voltage for a rectangular wave or pulse wave corresponds





approximately to the allowable voltage for a sine wave whose fundamental frequency is twice as large as that of the rectangular wave or pulse wave.

This allowable voltage, however, varies depending on the voltage and current waveforms.

Therefore, you are requested to make sure that the self-heating temperature is not higher than the value specified in Table 1.

