mDOC G4 1Gb/2Gb to mDOC H3 1Gb/2Gb

Migration Guide, Rev. 0.7

July 2006
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REVISION HISTORY

Doc. No	Revision	Date	Description	Reference
92-UM-0905-00	0.1	October 2005	Initial version	
	0.2	November 2005	mDOC H3 power management parameters updated	Section 4.2
	0.3	November 2005	Electrical configuration schematics modified	Section 4.2
	0.4	December 2005	Mechanical package information added	Section 6
	0.5	December 2005	Core 3.3V and I/O 1.8V Electrical Configuration	Section 4.2, Figure 3
			Changed location of GPIO_TIMER and JTAG RSRVD signals	Section 4.3
	0.6	January 2006	Changed mechanical specification	Section 6
			RSRVD ball assignment changes	Sections 4.3, 4.4
	0.7	July 2006	Ordering information modified	Sections 1 and 3
			mDOC H3 performance updated	Section 3
			A note regarding top boot in mDOC H3 added	Section 3
			Added migration path of mDOC G4 2Gb to mDOC H3 2Gb	Entire document
			DPD signal removed from mDOC H3 (replaced with A0/VSS, which should be connected to CPU A0 or to VSS)	Sections 4.3 and 4.4
			RSRVD balls left floating changed from a recommendation to a requirement	Sections 4.3 and 4.4
			Standard I/F Ball H9 changed from RSRVD to VSS	Section 4.3
			Ball G4 changed from RSRVD to VCCQ	Sections 4.3 and 4.4

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1. SCOPE

mDOC H3 is the next generation of the mDOC family of products, consisting of a new controller and advanced NAND technology flash. mDOC H3 products are packaged in a FBGA package that is ball to ball compatible with the mDOC G4 product lines. mDOC H3 introduces easier storage integration and boot implementation, multiple sources and a wide range of densities from 1Gb to 16Gb in 2006.

This guide describes the hardware-related guidelines for migrating from mDOC G4 1Gb and 2Gb 9x12mm devices to mDOC H3 1Gb and 2Gb 9x12 devices.

mDOC G4 1Gb, mDOC G4 2Gb, mDOC H3 1Gb and mDOC H3 2Gb ordering information is provided in Table 1.

Table 1: mDOC G4 and mDOC H3– Ordering information

Product	Capacity	Ordering Information
mDOC G4	128MByte (1Gbit) 1.8V core	MD8832-d1G-V18-X-P
	128MByte (1Gbit) 3.3V core	MD8832-d1G-V3-X-P
	256MByte (2Gbit) 1.8V core	MD8331-d2G-V18-X-P
	256MByte (2Gbit) 3.3V core	MD8331-d2G-V3-X-P
mDOC H3	128MByte (1Gbit) 3.3V/1.8V core and I/O	MD2534-d1G-X-P
	256MByte (2Gbit) 3.3V/1.8V core and I/O	MD2534-d2G-X-P

Note: Throughout this guide, product capacities will be referred to in Mbit (Mb), Gbit (Gb) MByte (MB), and GByte (GB).

2. MIGRATION REQUIREMENTS

It is possible to migrate from the mDOC G4 1Gb and 2Gb devices to mDOC H3 1Gb and 2Gb devices. All mDOC products are ball-to-ball compatible.

Designers should focus on the following issues when migrating between mDOC products:

- Revising the PCB layout (Section 4.1): mDOC H3 introduces some additional signals which are not available in mDOC G4. It is possible to design the PCB to accommodate a dual footprint for both mDOC H3 and G4 due to the ball to ball compatibility.
- Timing verification (Section 5): mDOC H3 product line has new timing specifications.
- Software changes (Section 7): mDOC H3 requires an updated version of TrueFFS.

Please note that mDOC G4 1Gb and 2Gb have 69 balls while the mDOC H3 1Gb and 2Gb devices have 115 balls. The migration path described in this document defines a combined, 115 ball foot print that accommodates both devices.

3. FEATURE COMPARISON

Table 2 compares the features offered by mDOC G4 1Gb to those offered by mDOC H3 1Gb.

Table 2: Feature List for mDOC G4 1Gb vs. H3 1Gb Product

Features	mDOC G4		mDOC H3	
	mDOC G4 1Gb	**mDOC G4 2Gb**	**mDOC H3 1Gb**	**mDOC H3 2Gb**
Ordering Information	MD8832-d1G-V18-X-P, MD8832-d1G-V3-X-P	MD8331-d2G-V18-X-P MD8331-d2G-V3-X-P	MD2534-d1G-X-P	MD2534-d2G-X-P
NAND Process (nm)	90	90	70	70
Form Factor (mm) Total Number of Balls	9x12x1.2 FBGA 69 balls	9x12x1.2 FBGA 69 balls	9x12 x1.2 FBGA 115 balls	9x12 x1.2 FBGA 115 balls
Asynchronous Boot Mode	√	√	√	√
Interface: NOR-like/Multiplexed	√/√	√/√	√/√	√/√
Interface: Serial SPI	-	-	√	√
Boot Block (KB)	2	2	32²	32²
Security and Protection Features (OTP, unique ID, protected partition)	√	√	√	√
Cascading (Maximum Number of Devices)	4	2	2	2
EDC/ECC	BCH & Hamming 4-bit	BCH & Hamming 4-bit	BCH 6-bit	BCH 6-bit
8 bit Bus Width	√	√	-	-
16 bit Bus Width	√	√	√	√
Power Requirements (Typical Parameters)				
Core / I/O Operation Voltage (VCC/VCCQ) (V)	3.3/3.3; 3.3/1.8 1.8/1.8	3.3/3.3; 3.3/1.8 1.8/1.8	3.3/3.3; 3.3/1.8 1.8/1.8	3.3/3.3; 3.3/1.8 1.8/1.8
Typical Current Requirement per Operation (Icc) (mA)	Read 4.2 Program 7.4 Erase 7.4	Read 4.2 Program 7.4 Erase 7.4	Turbo Mode – 30 PowerSave Mode - 20	Turbo Mode – 30 PowerSave Mode - 20
Typical Deep Power Down Current (Iccs) (µA)	10	20	45	45

Features	mDOC G4		mDOC H3	
	mDOC G4 1Gb	mDOC G4 2Gb	mDOC H3 1Gb	mDOC H3 2Gb
Performance				
Sustained Write (MB/sec)	2.4	2.4	5-7	5-7
Sustained Read (MB/sec)	10	10	15-25	15-25

1. Note: the "√" symbol indicates that a feature is implemented.
2. Up to 32KB may be used when using 128KB memory window (connecting A13-A16). Up to 2KB may be used when using 8KB memory window (connecting A13-A16 not required). When using 8KB memory window, only boot from lowest mDOC address (mDOC base address, typically address zero) is supported. Boot from top address (mDOC base address + 0x1ffe) is not supported, as mDOC top address range (0x1800-0x1ffe) does not alias IPL in this mode.

4. MDOC G4 1GB/2GB TO MDOC H3 1GB/2GB MIGRATION

4.1. Revising the PCB Layout

mDOC H3 is ball to ball compatible with mDOC G4.

However when migrating from mDOC G4 1Gb or 2Gb 9x12mm to mDOC H3 1Gb or 2Gb 9x12mm products:

- Changes must be made to account for the increase in the number of balls (from 69 in G4 to 115 in H3).
- New signal routing is required for the PCB, to support the additional signals of mDOC H3.

The following sections describe the ballout and signal descriptions of the standard and multiplexed interfaces (of both mDOC G4 and mDOC H3 devices). DPD Signal in mDOC G4 and mDOC H3

DPD Signal is relevant for the mDOC G4 product line only. When enabled, the DPD input is used to enter/exit Deep Power-Down mode. Depending on the settings in the DPD register, it can be used to enter or exit upon either assertion or negation.
For mDOC H3 devices this signal is not used. The DPD functionality is activated via SW, and no HW support is required. In case this signal is pulled high during mDOC H3 normal work, some functionality is disabled. Please refer to *Errata for mDOC H3 and mDOC H3-Based MCPs* for further information.

Figure 1 below describes a possible single PCB design to support both mDOC G4 and mDOC H3.

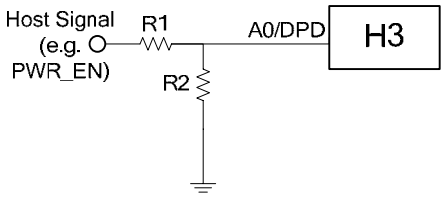

Figure 1: Single PCB Design for mDOC G4 and mDOC H3

- When mDOC H3 is used, the R2 ball should be connected (zero value resistor) and the R1 ball should be disconnected. This way A0/DPD signal is always low for mDOC H3 and mDOC H3-based MCPs.
- When mDOC G4 is used, the R1 ball should be connected (zero value resistor) and the R2 ball should be disconnected. This way A0/DPD signal can still be pulled low when taking mDOC out of DPD.

4.2. mDOC G4 and H3 Power Management

mDOC G4 and H3 share the same Device IO power supply (VCCQ) signals. mDOC H3 requires additional device controller supply connectivity as shown below:

Table 3: mDOC H3 Added Device Controller Supply

Signal	Ball No.	Description
VCCQ	K6 , G4	I/O power supply. Ball K6 requires a 10 nF and 0.1 µF capacitor.
VCC	K5	mDOC Device supply. Requires a 10 nF and 0.1 µF capacitor.
VCC1	E7	mDOC H3 internal supply. Requires a 1µF capacitor. Note: If 1.8V VCC supply is not available this ball should be connected to a 1uF capacitor only.
VCC2	D5	mDOC H3 internal supply. Requires a 1µF and 0.1 µF capacitor. Note: If 3.3V supply is not available this ball should be connected to 1µF and 0.1 µF capacitors only.
C+, C-	E6, F6	mDOC H3 requires a 33nF capacitor connected between the C+ and C- signals.

mDOC devices can be configured to support different combinations of Core and IO host supply. When migrating from mDOC G4 to H3, additional power supply connectivity of mDOC H3 should be added.

Table 4 lists the connectivity required for the support of the different available combinations.

Table 4: mDOC Core and IO Power Supply Connectivity

mDOC power Supply	VCC (Ball K5)	VCCQ (Ball K6 , G4)	VCC1 (Ball E7)	VCC2 (Ball D5)	C+, C- (Balls E6, F6)
Core: 3.3V [2.7V-3.6V] IO: 3.3V [2.5V-3.6V]	3.3V [2.7V-3.6V]	3.3V [2.5V-3.6V]	Requires a 1uF capacitor only	3.3V [2.7V-3.6V]	No Connection
Core: 3.3V [2.7V-3.6V] IO: 1.8V [1.65V-1.95V]	3.3V [2.7V-3.6V]	1.8V [1.65V-1.95V]	Requires a 1uF capacitor only]	3.3V [2.7V-3.6V]	No Connection
Core: 1.8V [1.65V-1.95V] IO: 1.8V [1.65V-1.95V]	1.8V [1.65V-1.95V]	1.8V [1.65V-1.95V]	1.8V [1.65V-1.95V]	Requires a 1uF and 0.1 µF capacitor only	requires a 33nF capacitor

Figure 2, Figure 3 and Figure 4 provide a schematic view of the connectivity required for the different core and IO voltages.

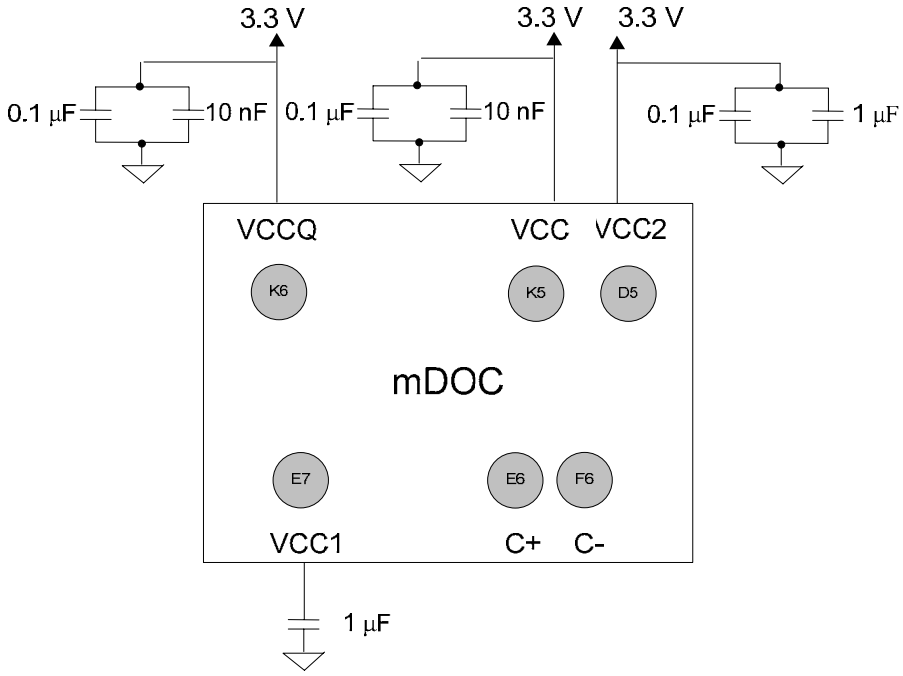

Figure 2: Core 3.3V and IO 3.3V Electrical Configuration

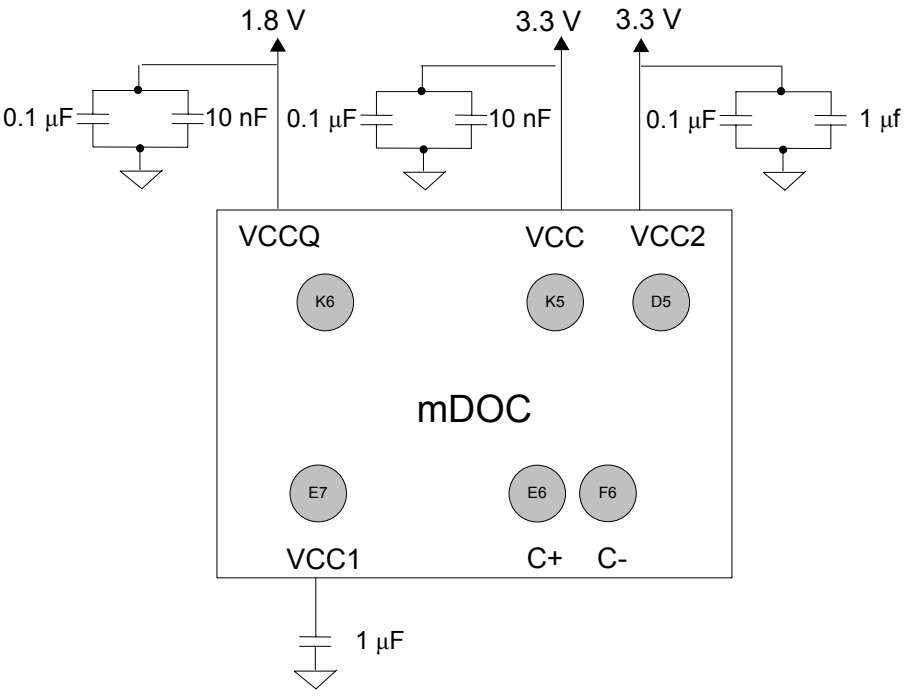

Figure 3: Core 3.3V and IO 1.8V Electrical Configuration

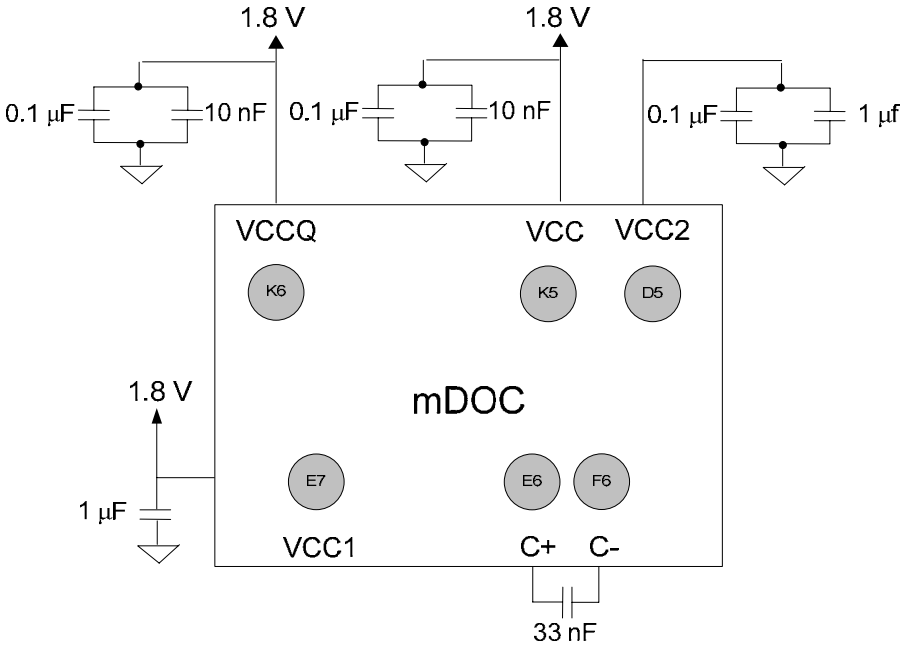

Figure 4: Core 1.8V and IO 1.8V Electrical Configuration

4.3. Standard Interface

4.3.1. Ballout

Figure 5 shows a top view of the ballout for the standard interface upgrade path from mDOC G4 1Gb/2Gb 9x12mm 69 ball to mDOC H3 1Gb/2Gb 9x12mm 115 ball.

Note: The balls highlighted in grey represent the balls of the mDOC G4 1Gb/2Gb device (69 balls). The white balls represent the balls added in mDOC H3 1Gb/2Gb (115 balls). The black ball represents an alignment identifier in the 69 ball layout that is a reserved ball in the 115 ball layout.

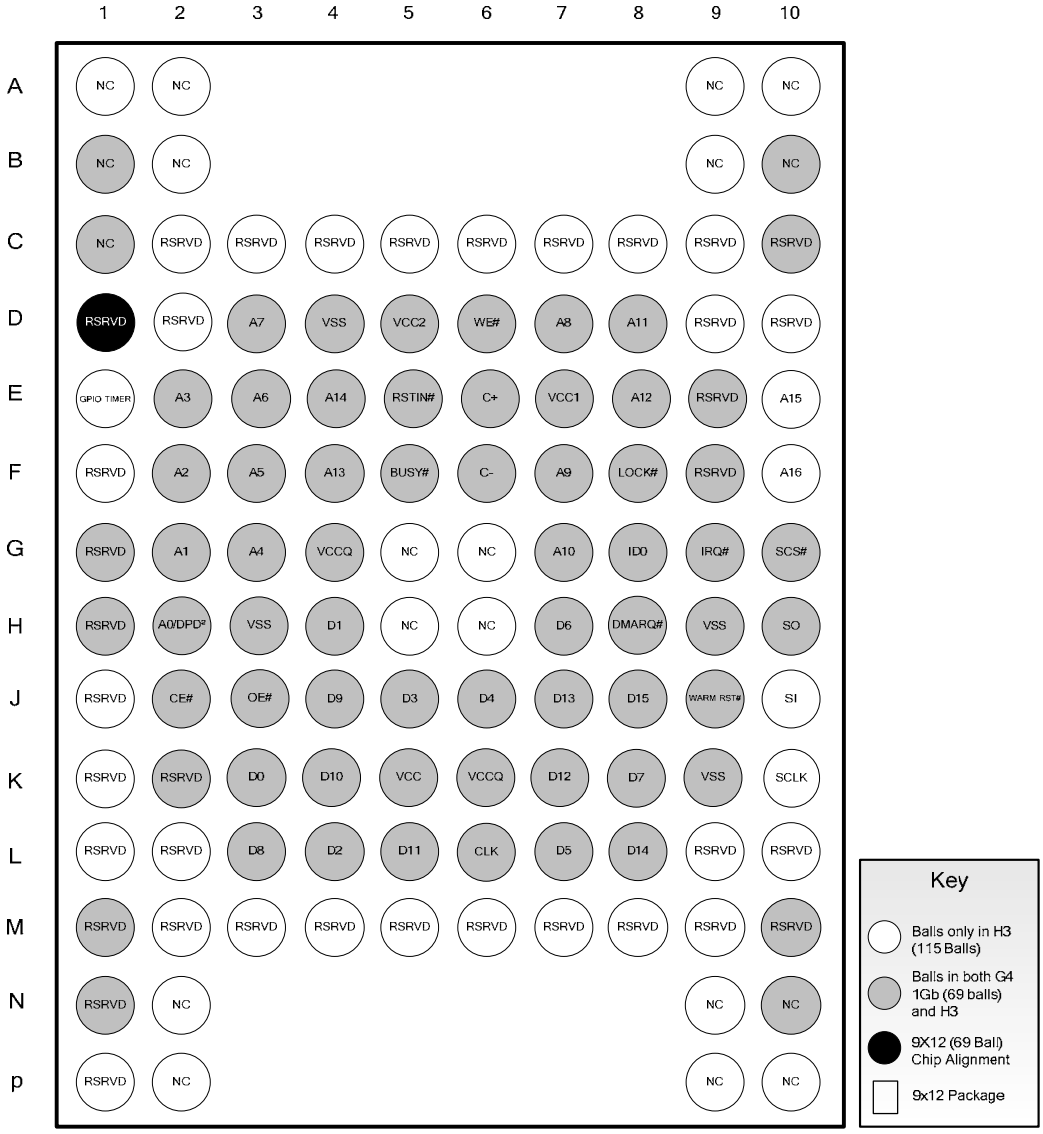

Figure 5: Standard Interface Ball Diagram – Top View

Notes: 1. Ball D1 is the 9x12 package (69 ball) chip alignment ball.
C1 is the 9x12 and 12x18 package (115 ball) chip alignment ball (no ball).

2. Please refer to section 4.1 for further details regarding how to connect ball H2.

3. Ball G4 must be connected to VCCQ. Connecting this ball to capacitors is not mandatory (can be connected same as IF_CFG signal on mDOC G3/P3, mDOC G3/P3 LP, mDOC G4 and mDOC H1).

4.3.2. Signal Description

All mDOC products specified in this document are ball to ball compatible.

The ball designations are listed in the signal descriptions, presented in logic groups, in Table 5.

Table 5: Standard Interface Signal Description

Signal	Ball No.	Description	G4 69 Balls	H3 115 Balls
System Interface				
A[16:15] A[14:13]	F10, E10 E4, F4	Address bus. If not used may be left floating.	-	√
A[12:11] A[10:8] A[7:4] A[3:0]	E8, D8 G7, F7, D7 D3, E3, F3, G3 E2, F2, G2, H2	Address bus.	√	√
D[7:6] D[5:3] D[2:0]	K8, H7 L7, J6, J5 L4, H4, K3	Data bus, low byte.	√	√
D[15:14] D[13:12] D[11:8]	J8, L8 J7, K7 L5, K4, J4, L3	Data bus, high byte.	√	√.
CE#	J2	Chip Enable, active low.	√	√
OE#	J3	Output Enable, active low.	√	√
WE#	D6	Write Enable, active low.	√	√
Configuration				
GPIO_TIMER	E1	mDOC H3 GPIO or configurable timer. If not used may be left floating.	-	√
ID[1:0]	H9, G8	Identification. Configuration control to support up to four chips cascaded in the same memory window. Chip 1: ID1, ID0 = VSS, VSS (0,0); required for single chip as well. Chip 2: ID1, ID0 = VSS, VCC (0,1) Chip 3: ID1, ID0 = VCC, VSS (1,0) Chip 4: ID1, ID0 = VCC, VCC (1,1)	√	-/√ mDOC H3 support cascading of up to 2 devices only. In this case ID1 is not used, and must be connected to VSS.
IF_CFG	G4	Interface Configuration. Set to 1 (VCCQ) for 16-bit interface mode. Clear to 0 (VSS) for 8-bit interface mode.	√	-/√ mDOC H3 support only 16 bit interface. This signal must be connected

Signal	Ball No.	Description	G4 69 Balls	H3 115 Balls
				to VCCQ
LOCK#	F8	Lock, active low. When active, provides full hardware data protection of selected partitions.	√	√
Control				
WARM_RST#	J9	mDOC H3 Warm reset input, used for triggering device warm-reset. Active low. If not used may be left floating.	-	√
BUSY#	F5	Busy. Active low, open drain. Indicates that mDOC is initializing and should not be accessed. A pull-up resistor to VCCQ is required if this ball drives an input. A pull-up resistor is recommended even if this ball is not used (resistor value depends on the system).	√	√
RSTIN#	E5	Reset, active low.	√	√
CLK	L6	External clock input used for burst mode data transfers. If not used may be left floating.	√	√
DMARQ#	H8	DMA request. Active low. A pull-up resistor to VCCQ is required if this ball drives an input. A pull-up resistor is recommended even if this ball is not used (resistor value depends on the system).	√	√
IRQ#	G9	Interrupt Request. Active low. A pull-up resistor to VCCQ is required if this ball drives an input. A pull-up resistor is recommended even if this ball is not used (resistor value depends on the system).	√	√
DPD	H2	When IF_CFG=1(16bit), the device can be programmed to use this input to enter or exit DPD mode.	√	Not used on mDOC H3 (see section 4.1)
Serial Interface				
SCS#	G10	Serial Interface chip select. Active low. If not used may be left floating.	-	√
SO	H10	Serial Interface data out (In Serial slave mode) [1]. If not used may be left floating.	-	√
SI	J10	Serial Interface data in (In serial slave mode) [1]. If not used may be left floating.	-	√
SCLK	K10	Serial Interface clock. If not used may be left floating.	-	√
Power				
VCC2	D5	mDOC H3 internal supply. Requires a 1µF and 0.1 µF capacitor.	-	√
VCC1	E7	mDOC H3 internal supply. Requires a 1µF capacitor.	-	√
VCCQ	K6, G4	I/O power supply. Ball K6 requires a 10 nF and 0.1 µF capacitor.	√/-	√/√
VCC	K5	Device supply. Requires a 10 nF and 0.1 µF	√	√

Signal	Ball No.	Description	G4 69 Balls	H3 115 Balls
		capacitor.		
VSS	D4, H3, H9, K9	Ground. All VSS balls must be connected.	√	√
C+	E6	C1 - 33nF capacitor positive terminal[2].	-	√
C-	F6	C1 - 33nF capacitor negative terminal[2].	-	√
Reserved				
RSRVD	C2, C3, C4, C5, C6, C7, C8, C9, C10, D1, D2, D9, D10, E9, F1, F9, G1, H1, J1, K1, K2, L2, L9, L10, M2, M3, M4, M5, M6,M7, M8, M9, M10	Reserved signal that is not connected internally. All reserved signals are not connected internally, and if not identified in this document then it is recommended to leave them floating to guarantee forward compatibility with future products. They should not be connected to arbitrary signals and must not be left floating.	√	√
	P1	Test Data In (JTAG). Used for dedicated developer product only[3].	-	√
	M1	Test Data Out (JTAG). Used for dedicated developer product only[3].	-	√
	L1	Test Mode Select (JTAG). Used for dedicated developer product only[3].	-	√
	N1	Test Clock (JTAG). Used for dedicated developer product only[3].	-	√
Mechanical				
NC	A1, A2, A9, A10, B1, B2, B9, C1, B10, G5, G6, H5, H6, N2, N9, N10, P2, P9, P10	Not Connected.		

1. When mDOC H3 is used as a Master device, SO is used for Serial Interface Data In, and SI is used for Serial Interface Data Out.
2. The 33 nF capacitor is required only for 1.8V Core and 1.8V I/O configuration. Please see section 4.2 for further details.
3. The RSRVD JTAG balls will only be enabled on special versions of the mDOC H3 devices that will be used for debugging severe system problems. In order to support this feature, the JTAG balls should be brought out to a separate header or test points. The JTAG RSRVD balls must not be connected to the JTAG scan chain that is used for the rest of the PCB. If not used they should be left floating.

4.4. Multiplexed Interface

4.4.1. Ballout

Figure 6 shows a top view of the ballout for the multiplexed interface upgrade path from mDOC G4 1Gb/2Gb 9x12 mm 69 ball to mDOC H3 1Gb/2Gb 9x12 115 ball.

Note: The balls highlighted in grey represent the balls of the mDOC G4 device (69 balls). The white balls represent the balls added in mDOC H3 (115 balls). The added balls are all dummy balls. The black ball represents an alignment identifier in the 69 ball layout that is a reserved ball in the 115 ball layout.

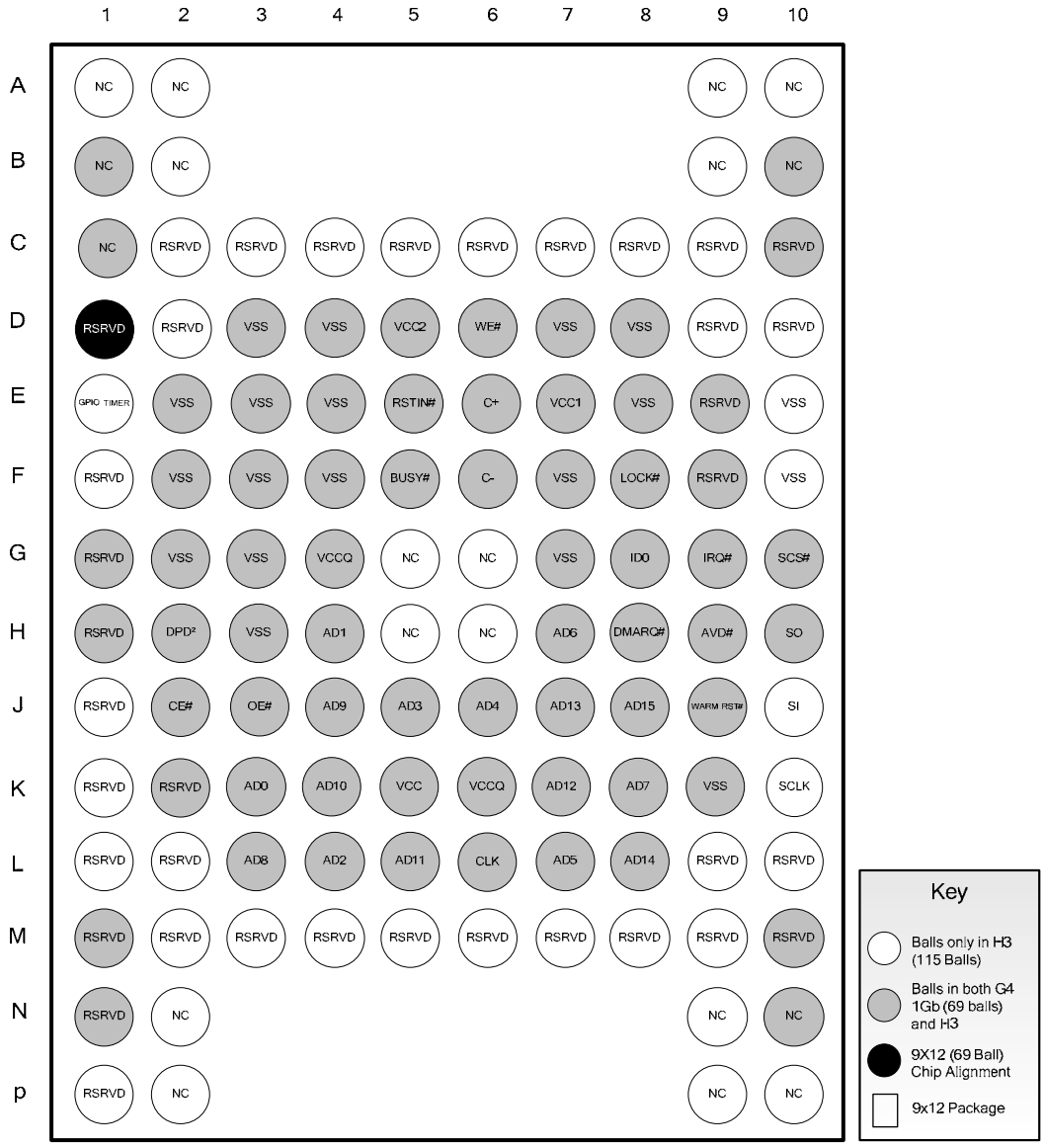

Figure 6: Multiplexed Interface Ball Diagram for FBGA – Top View

Notes: 1. Ball D1 is the 9x12 package (69 ball) chip alignment ball. C1 is the 9x12 and 12x18 package (115 ball) chip alignment ball (no ball).

2. Please refer to section 4.1 for further details regarding how to connect this ball.

3. Ball G4 must be connected to VCCQ. Connecting this ball to capacitors is not mandatory (can be connected same as IF_CFG signal on mDOC G3/P3, mDOC G3/P3 LP, mDOC G4 and mDOC H1).

4.4.2. Signal Description

All mDOC products specified in this document support common interface signals.

The ball designations are listed in the signal descriptions, presented in logic groups, in Table 6.

Table 6: Multiplexed Interface Signal Description

Signal	Ball No.	Description	G4 69 Balls	H3 115 Balls
System Interface				
AD[15:12] AD[11:8] AD[7:4] AD[3:0]	J8, L8, J7, K7 L5, K4, J4, L3 K8, H7, L7,J6 J5, L4, H4, K3	Multiplexed bus. Address and data signals.	√	√
CE#	J2	Chip Enable, active low.	√	√
OE#	J3	Output Enable, active low.	√	√
WE#	D6	Write Enable, active low.	√	√
Configuration				
GPIO_TIMER	E1	mDOC H3 GPIO or a configurable timer. If not used may be left floating.	-	√
AVD#	H9	Address Valid strobe. Set multiplexed interface.	√	√
ID0	G8	Identification. Configuration control to support up to two chips cascaded in the same memory window. Chip 1: ID0 = VSS, must be used for single-chip configuration. Chip 2: ID0 = VCCQ.	√	√
LOCK#	F8	Lock. Active low. When active, provides full hardware data protection of selected partitions.	√	√
Control				
WARM_RST#	J9	Active low. Warm reset input, used for triggering device warm-reset. If not used may be left floating.	-	√
BUSY#	F5	Busy. Active low, open drain. Indicates that mDOC is initializing and should not be accessed. A pull-up resistor to VCCQ is required if this ball drives an input. A pull-up resistor is recommended even if this ball is not used (resistor value depends on the system).	√	√
RSTIN#	E5	Reset, active low.	√	√

Signal	Ball No.	Description	G4 69 Balls	H3 115 Balls
CLK	L6	External clock input used for burst mode data transfers. If not used may be left floating.	√	√
DMARQ#	H8	DMA request. Open drain. A pull-up resistor to VCCQ is required if this ball drives an input. A pull-up resistor is recommended even if this ball is not used (resistor value depends on the system).	√	√
IRQ#	G9	Interrupt Request. Active low. A pull-up resistor to VCCQ is required if this ball drives an input. A pull-up resistor is recommended even if this ball is not used (resistor value depends on the system).	√	√
DPD	H2	Device can be programmed to use this input to enter or exit DPD mode.	√	Not used on mDOC H3 (see section 4.2)
Serial Interface				
SCS#	G10	Serial Interface chip select. Active Low. If not used may be left floating.	-	√
SO	H10	Serial Interface data out (In Serial slave mode) [1]. If not used may be left floating.	-	√
SI	J10	Serial Interface data in (In serial slave mode) [1]. If not used may be left floating.	-	√
SCLK	K10	Serial Interface clock. If not used may be left floating.	-	√
Power				
VCC2	D5	mDOC H3 internal supply. Requires a 1µF and 0.1 µF capacitor.	-	√
VCC1	E7	mDOC H3 internal supply. Requires a 1µF capacitor.	-	√
VCCQ	K6, G4	I/O power supply. Ball K6 requires a 10 nF and 0.1 µF capacitor.	√/√	√/√
VCC	K5	Device supply. Requires a 10 nF and 0.1 µF capacitor.	√	√
VSS	D3, D4, D7, D8, E2, E3, E4 E8, E10, F2, F3, F4, F7, F10, G2, G3, G7, H3, K9,	Ground. All VSS balls must be connected.	√	√
C+	E6	C1 - 33nF capacitor positive terminal[2].	-	√

Signal	Ball No.	Description	G4 69 Balls	H3 115 Balls
C-	F6	C1 - 33nF capacitor negative terminal[2].	-	√

Signal	Ball No.	Description	G4 69 Balls	H3 115 Balls
Reserved				
RSRVD	C2, C3, C4, C5, C6, C7, C8, C9, C10, D1, D2, D9, D10, E9, F1, F9, G1, H1, J1, K1, K2, L2, L9, L10, M2, M3, M4, M5, M6,M7, M8, M9, M10	Reserved signal that is not connected internally. All reserved signals are not connected internally and if not identified in this document then it is recommended to leave them floating to guarantee forward compatibility with future products. They should not be connected to arbitrary signals and must not be left floating.	RSRVD √	RSRVD √
	P1	Test Data In (JTAG). Used for dedicated developer product only[3].	-	√
	M1	Test Data Out (JTAG). Used for dedicated developer product only[3].	-	√
	L1	Test Mode Select (JTAG). Used for dedicated developer product only[3].	-	√
	N1	Test Clock (JTAG) Used for dedicated developer product only[3].	-	√
Mechanical				
NC	A1, A2, A9, A10, B1, B2, B9, B10, C1, G5, G6, H5, H6, N2, N9, N10, P2, P9, P10	Not Connected.		

1. When mDOC H3 is used as a Master device, SO is used for Serial Interface Data In, and SI is used for Serial Interface Data Out.
2. The 33 nF capacitor is required only for 1.8V Core and 1.8V I/O configuration. Please see section 4.2 for further details.
3. The RSRVD JTAG balls will only be enabled on special versions of the mDOC H3 devices that will be used for debugging severe system problems. In order to support this feature, the JTAG balls should be brought out to a separate header or test points. The JTAG RSRVD balls must not be connected to the JTAG scan chain that is used for the rest of the PCB.

5. TIMING SPECIFICATIONS

When reviewing the timing specifications during the migration design, the following should be taken into account:

- Timing specifications for mDOC G4 standard and multiplexed interface read/write cycles are not identical to the timing specifications for mDOC H3 devices.
- When designing for compatibility between several mDOC devices, the worst-case timing should be used.
- For further information, see the product data sheets for mDOC G4 and mDOC H3.

6. MECHANICAL DIMENSIONS

mDOC H3 1Gb (128MB) / 2Gb (256MB)

FBGA 128MB (1Gb) dimensions: 9.0 ±0.20 mm x 12.0 ±0.20 mm x 1.1 ±0.1 mm

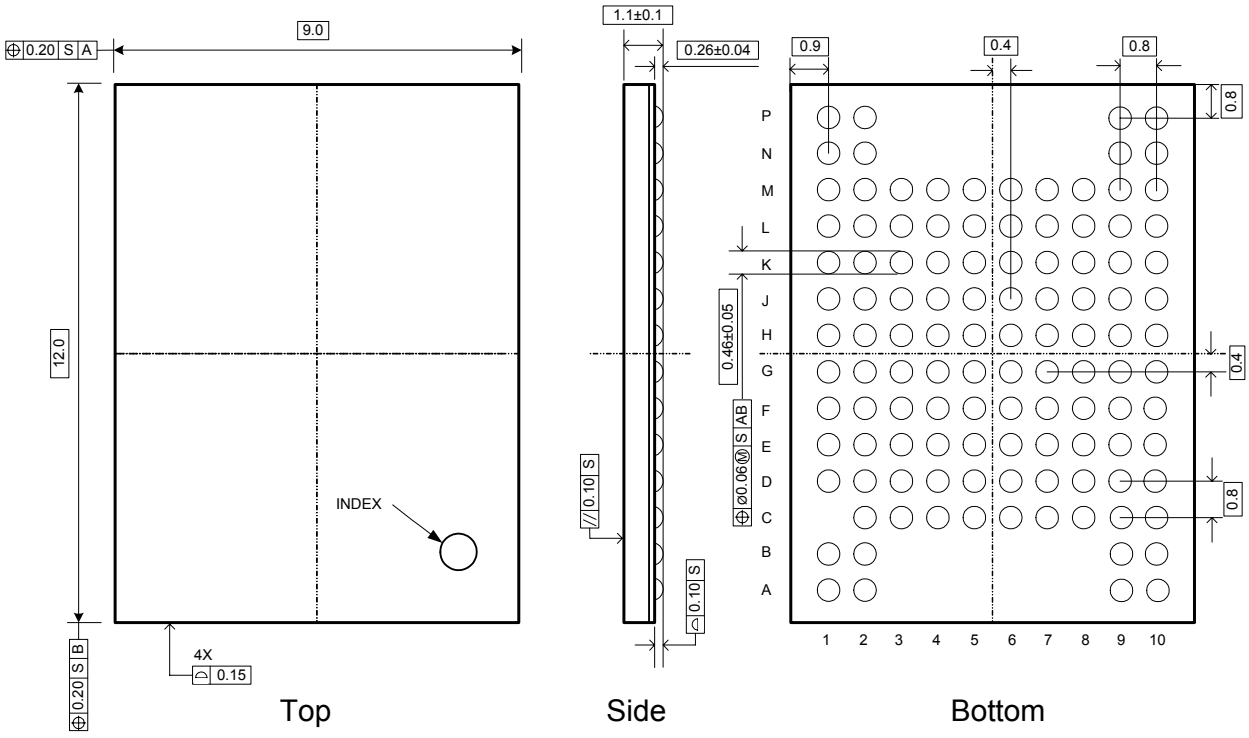

Figure 7: Mechanical Dimensions 9x12 FBGA Package

7. SOFTWARE CHANGES

- The software version must be upgraded to TrueFFS 7.1 for mDOC H3 devices. TrueFFS 7.1 supports both mDOC G3/P3, G3/P3 LP, G4, H1 and H3 families
- Boot code must be changed to support the new product line of mDOC H3. This includes:
  - Initiation Program Loader (IPL)
  - Secondary Program Loader (SPL) – not needed in mDOC H3
  - Rebuild of O/S Boot loader.
- More information regarding TrueFFS 7.x can be found in:
  - *mDOC TrueFFS 7.1 Software Development Kit (SDK) developer guide*.
  - *mDOC Software Utilities for TrueFFS 7.1 user manual.*

8. ADDITIONAL INFORMATION

Additional information about mDOC product families, including data sheets, developer guide and application notes, can be found at www.m-systems.com.

Document	Description
Data Sheet	mDOC G4 128MB/1Gb, 256MB/2Gb
Data Sheet	mDOC H1 512MB/4Gb, 1GB/8Gb
Data Sheet	mDOC H1 256MB/2Gb
Data Sheet	mDOC H3
Developer Guide	mDOC TrueFFS 7.1 Software Developer Kit (SDK)
Developer Guide	mDOC TrueFFS 7.1 Boot Software Development Kit (BDK)
Developer Guide	mDOC TrueFFS 7.1 Software Utilities
Developer Guide	mDOC Driver Extended Functions Based on TrueFFS 7.1

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