

MPC555

Product Brief **MPC555 Microcontroller**

Features

- MPC555 core with floating-point unit
- 26 Kbytes fast RAM and 6 Kbytes TPU microcode RAM
- 448 Kbytes flash EEPROM with 5-V programming
- 5-V I/O system
- Serial system: queued serial multi-channel module (QSMCM), dual CAN 2.0B controller modules (TouCAN™)
- 50-channel timer system: dual time processor units (TPU3), modular I/O system (MIOS1)
- 32 analog inputs: dual queued analog-to-digital converters (QADC64)
- Submicron HCMOS (CDR1) technology
- 272-pin plastic ball grid array (PBGA) packaging
- 40-MHz operation, -40 °C to 125 °C with dual supply (3.3 V, 5 V)
- 32-bit architecture (compliant with the PowerPC architecture, Book 1)
- Core performance measured at 52.7-Kbyte Dhrystones (v2.1) @ 40 MHz
- Fully static, low power operation
- Integrated double-precision floating-point unit
- Precise exception model
- Extensive system development support
 - On-chip watchpoints and breakpoints
 - Program flow tracking
 - BDM on-chip emulation development interface

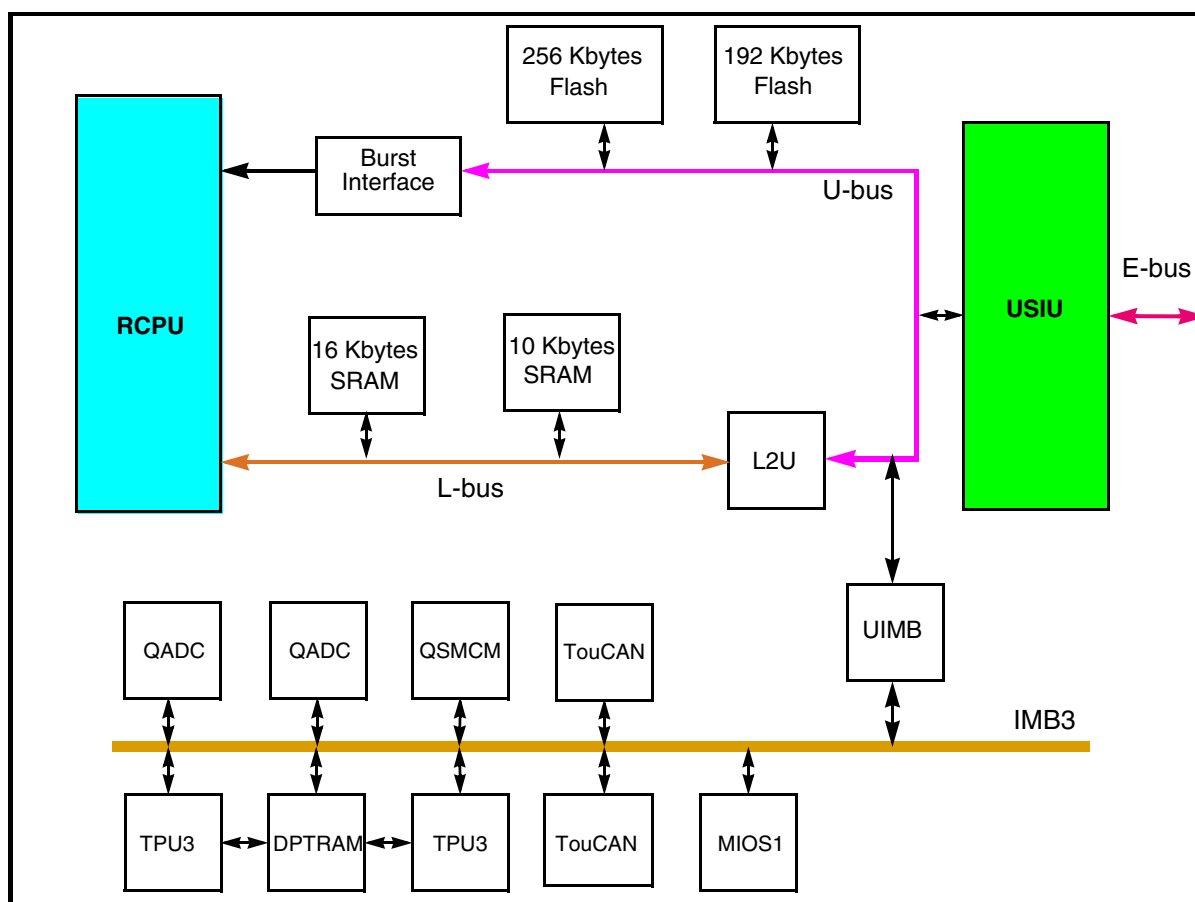


Figure 1 RISC MCU Central Processing Unit (RCPU)

Four-Bank Memory Controller

- Works with SRAM, EPROM, flash EEPROM, and other peripherals
- Byte write enables
- 32-bit address decodes with bit masks

U-Bus System Interface Unit (USIU)

- Clock synthesizer
- Power management
- Reset controller
- MPC555 decremter and time base
- Real-time clock register
- Periodic interrupt timer
- Hardware bus monitor and software watchdog timer
- Interrupt controller that supports up to eight external and eight internal interrupts
- IEEE 1149.1 JTAG test access port
- External bus interface
 - 24 address pins, 32 data pins
 - Supports multiple master designs
 - Four-beat transfer bursts, two-clock minimum bus transactions
 - Supports 5V inputs, provides 3.3-V outputs

Flexible Memory Protection Unit

- Four instruction regions and four data regions
- 4-Kbyte to 16-Mbyte region size support
- Default attributes available in one global entry
- Attribute support for speculative accesses

448-Kbyte Flash EEPROM Memory

- One 256-Kbyte and one 192-Kbyte module
- Page read mode
- Block (32-Kbyte) erasable
- External 4.75-V to 5.25-V program and erase power supply

26-Kbytes of Static RAM

- One 16-Kbyte and one 10-Kbyte module
- Fast (one-clock) access
- Keep-alive power
- Soft defect detection (SDD)

General-Purpose I/O Support

- Address (24) and data (32) pins can be used for general-purpose I/O in single-chip mode
- Nine general-purpose I/O pins in MIOS1 unit
- Many peripheral pins can be used for general-purpose I/O when not used for primary function
- 5-V tolerant inputs/outputs

Two Time Processor Units (TPU3)

- Each TPU3 module provides these features:
 - A dedicated micro-engine operates independently of the RCP
 - 16 independent programmable channels and pins
 - Each channel has an event register consisting of a 16-bit capture register, a 16-bit compare register and a 16-bit comparator
 - Nine pre-programmed timer functions are available
 - Any channel can perform any time function
 - Each timer function can be assigned to more than one channel
 - Two timer count registers with programmable prescalers
 - Each channel can be synchronized to one or both counters
 - Selectable channel priority levels
 - 5-V tolerant inputs/outputs
- 6-Kbyte dual port TPU RAM (DPTRAM) is shared by the two TPU3 modules for TPU microcode

18-Channel Modular I/O System (MIOS1)

- Ten double action submodules (DASM)
- Eight dedicated PWM sub-modules (PWMSM)
- Two 16-bit modulus counter submodules (MCSM)
- Two parallel port I/O submodules (PIOSM)
- 5-V tolerant inputs/outputs

Two Queued Analog-to-Digital Converter 2 Modules (QADC64)

Each QADC provides:

- Up to 16 analog input channels, using internal multiplexing
- Up to 41 total input channels, using internal and external multiplexing
- 10-bit A/D converter with internal sample/hold
- Typical conversion time of 10 μ s (100,000 samples per second)
- Two conversion command queues of variable length
- Automated queue modes initiated by:

- External edge trigger/level gate
- Software command
- 64 result registers
- Output data that is right- or left-justified, signed or unsigned
- 5-V reference and range

Two CAN 2.0B Controller Modules (TouCAN™)

Each TouCAN™ provides these features:

- Full implementation of CAN protocol specification, version 2.0A and 2.0B
- Each module has 16 receive/transmit message buffers of 0 to 8 bytes data length
- Global mask register for message buffers 0 to 13
- Independent mask registers for message buffers 14 and 15
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- 16-bit free-running timer for message time-stamping
- Low power sleep mode with programmable wake-up on bus activity
- Programmable I/O modes
- Maskable interrupts
- Independent of the transmission medium (external transceiver is assumed)
- Open network architecture
- Multimaster concept
- High immunity to EMI
- Short latency time for high-priority messages
- Low power sleep mode with programmable wakeup on bus activity

Queued Serial Multi-Channel Module (QSMCM)

- Queued serial peripheral interface (QSPI)
 - Provides full-duplex communication port for peripheral expansion or interprocessor communication
 - Up to 32 preprogrammed transfers, reducing overhead
 - 160-byte queue buffer
 - Programmable transfer length: from 8 to 16 bits, inclusive
 - Synchronous interface with baud rate of up to system clock divided by 4
 - Four programmable peripheral-select pins support up to 16 devices
 - Wrap-around mode allows continuous sampling for efficient interfacing to serial peripherals (e.g., – serial A/D converters, I/O latches, etc.)
- Two serial communications interfaces (SCI). Each SCI offers these features:
 - UART mode provides NRZ format and half-or full-duplex interface
 - 16 register receive buffer and 16 register transmit buffer (SCI1 only)
 - Advanced error detection and optional parity generation and detection
 - Word length programmable as 8 or 9 bits
 - Separate transmitter and receiver enable bits and double buffering of data
 - Wakeup functions allow the CPU to run uninterrupted until either a true idle line is detected or a new address byte is received
 - External source clock for baud generation
 - Multiplexing of transmit data pins with discrete outputs and receive data pins with discrete inputs, allowing realization of a low-speed serial protocol

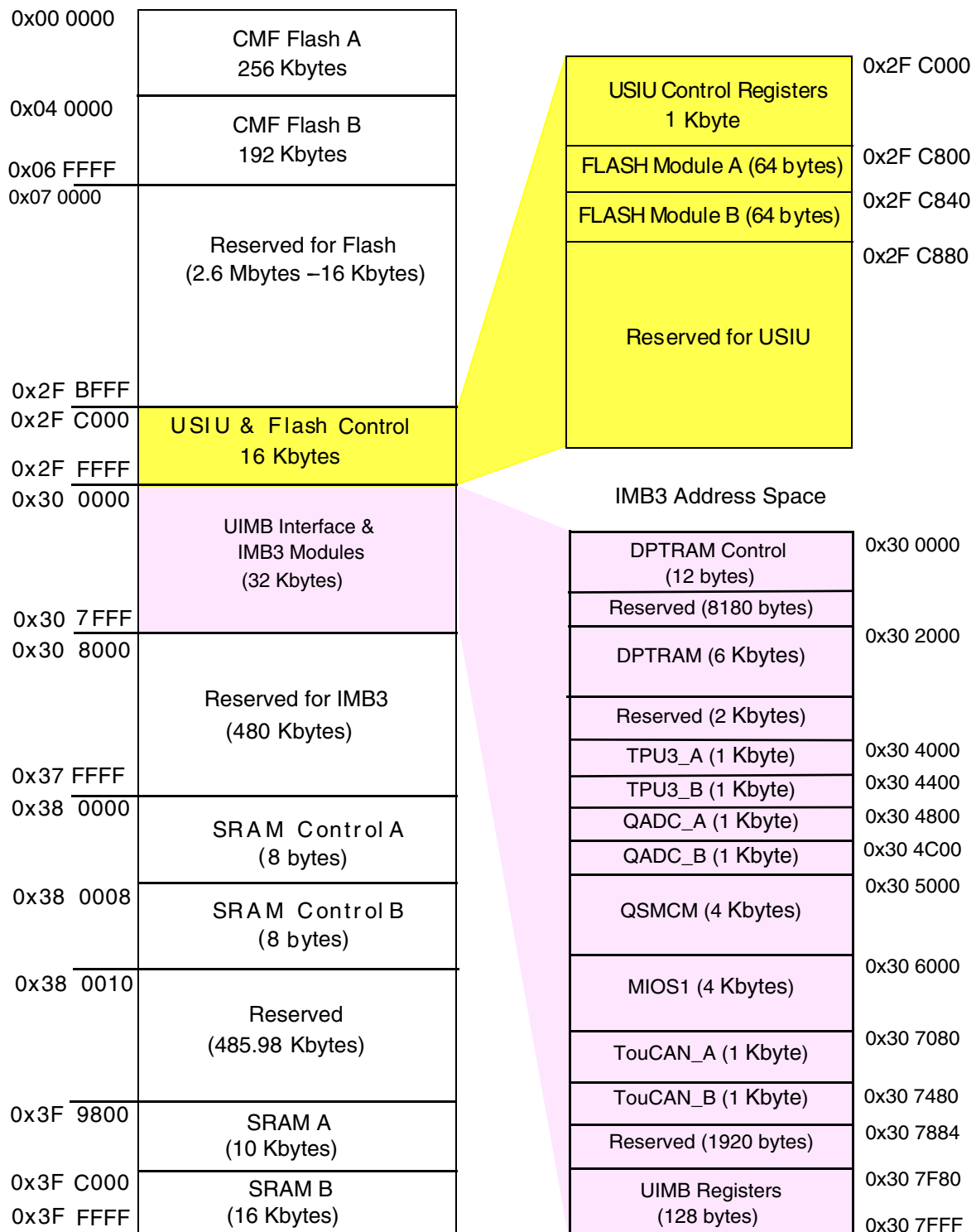


Figure 2 MPC555 Internal Memory Map

MPC555 Ball Map

A	VDDH	A_TPUCH1	A_TPUCH4	A_TPUCH8	A_TPUCH12	A_TPUCH16	VRL	AA0_PCB1	AA0_PCB2	AA0_PCB3	AA0_PCB4	AA0_PCB5	AA0_PCB6	AA0_PCB7	AA0_PCB8	AA0_PCB9	AA0_PCB10	AA0_PCB11	AA0_PCB12	AA0_PCB13	AA0_PCB14	AA0_PCB15	AA0_PCB16	AA0_PCB17	AA0_PCB18	AA0_PCB19	AA0_PCB20
B	B_TZLK	VDDH	A_TPUCH5	A_TPUCH9	A_TPUCH13	A_TPUCH17	VRH	AA1_PCB1	AA1_PCB2	AA1_PCB3	AA1_PCB4	AA1_PCB5	AA1_PCB6	AA1_PCB7	AA1_PCB8	AA1_PCB9	AA1_PCB10	AA1_PCB11	AA1_PCB12	AA1_PCB13	AA1_PCB14	AA1_PCB15	AA1_PCB16	AA1_PCB17	AA1_PCB18	AA1_PCB19	AA1_PCB20
C	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA2_PCB1	AA2_PCB2	AA2_PCB3	AA2_PCB4	AA2_PCB5	AA2_PCB6	AA2_PCB7	AA2_PCB8	AA2_PCB9	AA2_PCB10	AA2_PCB11	AA2_PCB12	AA2_PCB13	AA2_PCB14	AA2_PCB15	AA2_PCB16	AA2_PCB17	AA2_PCB18	AA2_PCB19	AA2_PCB20
D	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA3_PCB1	AA3_PCB2	AA3_PCB3	AA3_PCB4	AA3_PCB5	AA3_PCB6	AA3_PCB7	AA3_PCB8	AA3_PCB9	AA3_PCB10	AA3_PCB11	AA3_PCB12	AA3_PCB13	AA3_PCB14	AA3_PCB15	AA3_PCB16	AA3_PCB17	AA3_PCB18	AA3_PCB19	AA3_PCB20
E	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA4_PCB1	AA4_PCB2	AA4_PCB3	AA4_PCB4	AA4_PCB5	AA4_PCB6	AA4_PCB7	AA4_PCB8	AA4_PCB9	AA4_PCB10	AA4_PCB11	AA4_PCB12	AA4_PCB13	AA4_PCB14	AA4_PCB15	AA4_PCB16	AA4_PCB17	AA4_PCB18	AA4_PCB19	AA4_PCB20
F	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA5_PCB1	AA5_PCB2	AA5_PCB3	AA5_PCB4	AA5_PCB5	AA5_PCB6	AA5_PCB7	AA5_PCB8	AA5_PCB9	AA5_PCB10	AA5_PCB11	AA5_PCB12	AA5_PCB13	AA5_PCB14	AA5_PCB15	AA5_PCB16	AA5_PCB17	AA5_PCB18	AA5_PCB19	AA5_PCB20
G	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA6_PCB1	AA6_PCB2	AA6_PCB3	AA6_PCB4	AA6_PCB5	AA6_PCB6	AA6_PCB7	AA6_PCB8	AA6_PCB9	AA6_PCB10	AA6_PCB11	AA6_PCB12	AA6_PCB13	AA6_PCB14	AA6_PCB15	AA6_PCB16	AA6_PCB17	AA6_PCB18	AA6_PCB19	AA6_PCB20
H	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA7_PCB1	AA7_PCB2	AA7_PCB3	AA7_PCB4	AA7_PCB5	AA7_PCB6	AA7_PCB7	AA7_PCB8	AA7_PCB9	AA7_PCB10	AA7_PCB11	AA7_PCB12	AA7_PCB13	AA7_PCB14	AA7_PCB15	AA7_PCB16	AA7_PCB17	AA7_PCB18	AA7_PCB19	AA7_PCB20
I	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA8_PCB1	AA8_PCB2	AA8_PCB3	AA8_PCB4	AA8_PCB5	AA8_PCB6	AA8_PCB7	AA8_PCB8	AA8_PCB9	AA8_PCB10	AA8_PCB11	AA8_PCB12	AA8_PCB13	AA8_PCB14	AA8_PCB15	AA8_PCB16	AA8_PCB17	AA8_PCB18	AA8_PCB19	AA8_PCB20
J	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA9_PCB1	AA9_PCB2	AA9_PCB3	AA9_PCB4	AA9_PCB5	AA9_PCB6	AA9_PCB7	AA9_PCB8	AA9_PCB9	AA9_PCB10	AA9_PCB11	AA9_PCB12	AA9_PCB13	AA9_PCB14	AA9_PCB15	AA9_PCB16	AA9_PCB17	AA9_PCB18	AA9_PCB19	AA9_PCB20
K	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA10_PCB1	AA10_PCB2	AA10_PCB3	AA10_PCB4	AA10_PCB5	AA10_PCB6	AA10_PCB7	AA10_PCB8	AA10_PCB9	AA10_PCB10	AA10_PCB11	AA10_PCB12	AA10_PCB13	AA10_PCB14	AA10_PCB15	AA10_PCB16	AA10_PCB17	AA10_PCB18	AA10_PCB19	AA10_PCB20
L	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA11_PCB1	AA11_PCB2	AA11_PCB3	AA11_PCB4	AA11_PCB5	AA11_PCB6	AA11_PCB7	AA11_PCB8	AA11_PCB9	AA11_PCB10	AA11_PCB11	AA11_PCB12	AA11_PCB13	AA11_PCB14	AA11_PCB15	AA11_PCB16	AA11_PCB17	AA11_PCB18	AA11_PCB19	AA11_PCB20
M	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA12_PCB1	AA12_PCB2	AA12_PCB3	AA12_PCB4	AA12_PCB5	AA12_PCB6	AA12_PCB7	AA12_PCB8	AA12_PCB9	AA12_PCB10	AA12_PCB11	AA12_PCB12	AA12_PCB13	AA12_PCB14	AA12_PCB15	AA12_PCB16	AA12_PCB17	AA12_PCB18	AA12_PCB19	AA12_PCB20
N	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA13_PCB1	AA13_PCB2	AA13_PCB3	AA13_PCB4	AA13_PCB5	AA13_PCB6	AA13_PCB7	AA13_PCB8	AA13_PCB9	AA13_PCB10	AA13_PCB11	AA13_PCB12	AA13_PCB13	AA13_PCB14	AA13_PCB15	AA13_PCB16	AA13_PCB17	AA13_PCB18	AA13_PCB19	AA13_PCB20
O	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA14_PCB1	AA14_PCB2	AA14_PCB3	AA14_PCB4	AA14_PCB5	AA14_PCB6	AA14_PCB7	AA14_PCB8	AA14_PCB9	AA14_PCB10	AA14_PCB11	AA14_PCB12	AA14_PCB13	AA14_PCB14	AA14_PCB15	AA14_PCB16	AA14_PCB17	AA14_PCB18	AA14_PCB19	AA14_PCB20
P	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA15_PCB1	AA15_PCB2	AA15_PCB3	AA15_PCB4	AA15_PCB5	AA15_PCB6	AA15_PCB7	AA15_PCB8	AA15_PCB9	AA15_PCB10	AA15_PCB11	AA15_PCB12	AA15_PCB13	AA15_PCB14	AA15_PCB15	AA15_PCB16	AA15_PCB17	AA15_PCB18	AA15_PCB19	AA15_PCB20
Q	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA16_PCB1	AA16_PCB2	AA16_PCB3	AA16_PCB4	AA16_PCB5	AA16_PCB6	AA16_PCB7	AA16_PCB8	AA16_PCB9	AA16_PCB10	AA16_PCB11	AA16_PCB12	AA16_PCB13	AA16_PCB14	AA16_PCB15	AA16_PCB16	AA16_PCB17	AA16_PCB18	AA16_PCB19	AA16_PCB20
R	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA17_PCB1	AA17_PCB2	AA17_PCB3	AA17_PCB4	AA17_PCB5	AA17_PCB6	AA17_PCB7	AA17_PCB8	AA17_PCB9	AA17_PCB10	AA17_PCB11	AA17_PCB12	AA17_PCB13	AA17_PCB14	AA17_PCB15	AA17_PCB16	AA17_PCB17	AA17_PCB18	AA17_PCB19	AA17_PCB20
S	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA18_PCB1	AA18_PCB2	AA18_PCB3	AA18_PCB4	AA18_PCB5	AA18_PCB6	AA18_PCB7	AA18_PCB8	AA18_PCB9	AA18_PCB10	AA18_PCB11	AA18_PCB12	AA18_PCB13	AA18_PCB14	AA18_PCB15	AA18_PCB16	AA18_PCB17	AA18_PCB18	AA18_PCB19	AA18_PCB20
T	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA19_PCB1	AA19_PCB2	AA19_PCB3	AA19_PCB4	AA19_PCB5	AA19_PCB6	AA19_PCB7	AA19_PCB8	AA19_PCB9	AA19_PCB10	AA19_PCB11	AA19_PCB12	AA19_PCB13	AA19_PCB14	AA19_PCB15	AA19_PCB16	AA19_PCB17	AA19_PCB18	AA19_PCB19	AA19_PCB20
U	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA20_PCB1	AA20_PCB2	AA20_PCB3	AA20_PCB4	AA20_PCB5	AA20_PCB6	AA20_PCB7	AA20_PCB8	AA20_PCB9	AA20_PCB10	AA20_PCB11	AA20_PCB12	AA20_PCB13	AA20_PCB14	AA20_PCB15	AA20_PCB16	AA20_PCB17	AA20_PCB18	AA20_PCB19	AA20_PCB20
V	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA21_PCB1	AA21_PCB2	AA21_PCB3	AA21_PCB4	AA21_PCB5	AA21_PCB6	AA21_PCB7	AA21_PCB8	AA21_PCB9	AA21_PCB10	AA21_PCB11	AA21_PCB12	AA21_PCB13	AA21_PCB14	AA21_PCB15	AA21_PCB16	AA21_PCB17	AA21_PCB18	AA21_PCB19	AA21_PCB20
W	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA22_PCB1	AA22_PCB2	AA22_PCB3	AA22_PCB4	AA22_PCB5	AA22_PCB6	AA22_PCB7	AA22_PCB8	AA22_PCB9	AA22_PCB10	AA22_PCB11	AA22_PCB12	AA22_PCB13	AA22_PCB14	AA22_PCB15	AA22_PCB16	AA22_PCB17	AA22_PCB18	AA22_PCB19	AA22_PCB20
X	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA23_PCB1	AA23_PCB2	AA23_PCB3	AA23_PCB4	AA23_PCB5	AA23_PCB6	AA23_PCB7	AA23_PCB8	AA23_PCB9	AA23_PCB10	AA23_PCB11	AA23_PCB12	AA23_PCB13	AA23_PCB14	AA23_PCB15	AA23_PCB16	AA23_PCB17	AA23_PCB18	AA23_PCB19	AA23_PCB20
Y	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA24_PCB1	AA24_PCB2	AA24_PCB3	AA24_PCB4	AA24_PCB5	AA24_PCB6	AA24_PCB7	AA24_PCB8	AA24_PCB9	AA24_PCB10	AA24_PCB11	AA24_PCB12	AA24_PCB13	AA24_PCB14	AA24_PCB15	AA24_PCB16	AA24_PCB17	AA24_PCB18	AA24_PCB19	AA24_PCB20
Z	B_TZLK	VDDH	A_TPUCH1	A_TPUCH5	A_TPUCH9	A_TPUCH13	VDDA	AA25_PCB1	AA25_PCB2	AA25_PCB3	AA25_PCB4	AA25_PCB5	AA25_PCB6	AA25_PCB7	AA25_PCB8	AA25_PCB9	AA25_PCB10	AA25_PCB11	AA25_PCB12	AA25_PCB13	AA25_PCB14	AA25_PCB15	AA25_PCB16	AA25_PCB17	AA25_PCB18	AA25_PCB19	AA25_PCB20

Note: The pinout is a top down view of the package.

Figure 3 MPC555 Pinout Data

Version 10.2

21 November 1997

Substrate 9/30/97a

Y Dees

Ordering Information

Table 1 MPC555 Package Information

Device Name	Order Part Number	Package Info	Temp. Range
MPC555	MPC555LFMZP40	272 PBGA	-40 to +125 °C
MPC555	MPC555LFCZP40	272 PBGA	-40 to +85 °C
MPC555	MPC555LFMZP40R2	272 PBGA Shipped in tape and reel media	-40 to +125 °C
MPC555	MPC555LFCZP40R2	272 PBGA Shipped in tape and reel media	-40 to +85 °C

Table 2 lists the documents that provide a complete description of the MPC555 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola Semiconductor documentation page on the Internet (the source for the latest information).

Table 2 Available Documentation

Document Number	Title
MPC555UM/AD	<i>MPC555/556 User's Manual</i>
AN1282/D	<i>Board Strategies for Ensuring Optimum Frequency Synthesizer Performance.</i>
AN1778/D	<i>Using the MIOS on the MPC555 Evaluation Board</i>
AN1821/D	<i>Exception Table Relocation and Multi-Processor Address Mapping in the Embedded MPC5XX Family</i>
AN1837/D	<i>Non-Volatile Memory Technology Overview</i>
AN2001/D	<i>Designing Expansion Boards for the Motorola EVB555/ETAS ES200.</i>
AN2109/D	<i>MPC555 Interrupts.</i>
AN2127/D	<i>EMC Guidelines for MPC500-Based Automotive Powertrain Systems</i>

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How to reach us:

USA/EUROPE

Motorola Literature Distribution

P.O. Box 5405
Denver, Colorado 80217
1-303-675-2140
1-800-441-2447

Technical Information Center

1-800-521-6274

JAPAN

Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu, Minato-ku
Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC

Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
852-26668334

Home Page

<http://www.motorola.com/semiconductors>



MOTOROLA

Order Number MPC555PB/D