Double Data Rate (DDR) SDRAM

MT46V64M4 – 16 Meg x 4 x 4 banks
MT46V32M8 – 8 Meg x 8 x 4 banks
MT46V16M16 – 4 Meg x 16 x 4 banks

Features

- V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V
- V_{DD} = +2.6V ±0.1V, V_{DDQ} = +2.6V ±0.1V (DDR400)
- Bidirectional data strobe (DQS) transmitted/ received with data, i.e., source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two – one per byte)
- Programmable burst lengths: 2, 4, or 8
- Auto Refresh and Self Refresh Modes
- Longer-lead TSOP for improved reliability (OCPL)
- 2.5V I/O (SSTL_2 compatible)
- Concurrent auto precharge option supported
- ^{t}RAS lockout supported (^{t}RAP = ^{t}RCD)

Options — Marking

- Configuration
  - 64 Meg x 4 (16 Meg x 4 x 4 banks) — 64M4
  - 32 Meg x 8 (8 Meg x 8 x 4 banks) — 32M8
  - 16 Meg x 16 (4 Meg x 16 x 4 banks) — 16M16
- Plastic Package – OCPL
  - 66-pin TSOP — TG
  - 66-pin TSOP (lead-free) — P
- Plastic Package
  - 60-Ball FBGA (8mm x 14mm) — FG
  - 60-Ball FBGA (8mm x 14mm) lead-free — BG
- Timing – Cycle Time
  - 5ns @ CL = 3 (DDR400B) — -5B
  - 6ns @ CL = 2.5 (DDR333) FBGA only — -6
  - 6ns @ CL = 2.5 (DDR333) TSOP only — -6T
  - 7.5ns @ CL = 2 (DDR266) — -75E
  - 7.5ns @ CL = 2 (DDR266A) — -75Z
  - 7.5ns @ CL = 2.5 (DDR266B) — -75
- Self Refresh
  - Standard — None
  - Low-Power Self Refresh — L
- Temperature Rating
  - Commercial (0°C to +70°C) — None
  - Industrial (–40°C to +85°C) — IT
- Revision
  - x4, x8 — :G
  - x16 — :F

Table 1: Configuration Addressing

	64 Meg x 4	32 Meg x 8	16 Meg x 16
Configuration	16 Meg x 4 x 4 banks	8 Meg x 8 x 4 banks	4 Meg x 16 x 4 banks
Refresh Count	8K	8K	8K
Row Addressing	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	2K (A0–A9, A11)	1K (A0–A9)	512 (A0–A8)

Table 2: Key Timing Parameters

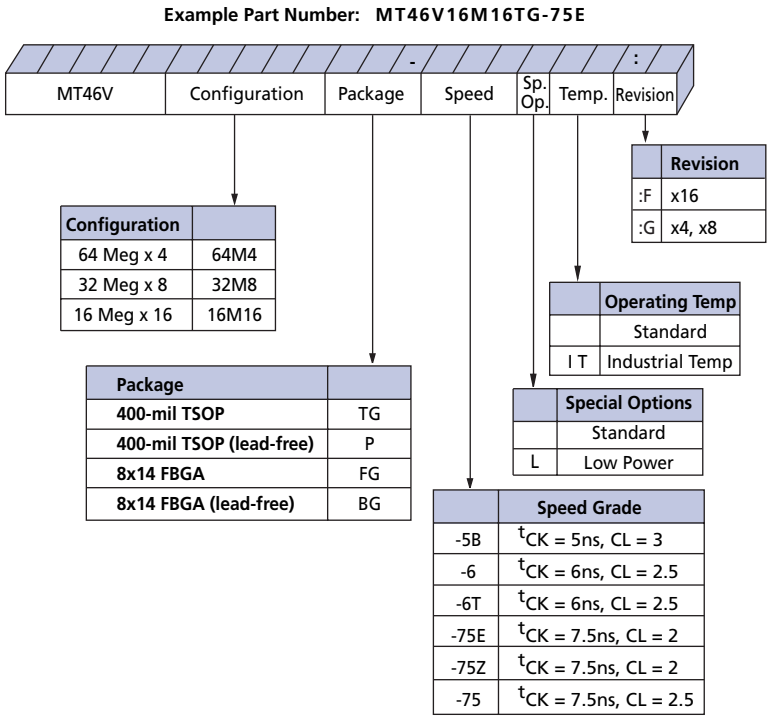
CL = CAS (READ) Latency; minimum clock rate @ CL = 2 (-75E, -75Z), CL = 2.5 (-6, -6T, -75), and CL = 3 (-5B)

Speed Grade	Clock Rate			Data-Out Window	Access Window	DQS–DQ Skew
	CL = 2	CL = 2.5	CL = 3			
-5B	133 MHz	167 MHz	200 MHz	1.6ns	±0.70ns	+0.40ns
-6	133 MHz	167 MHz	n/a	2.1ns	±0.70ns	+0.40ns
6T	133 MHz	167 MHz	n/a	2.0ns	±0.70ns	+0.45ns
-75E/-75Z	133 MHz	133 MHz	n/a	2.5ns	±0.75ns	+0.50ns
-75	100 MHz	133 MHz	n/a	2.5ns	±0.75ns	+0.50ns

Table 3: Speed Grade Compatibility

Marking	PC3200 (3-3-3)	PC2700 (2.5-3-3)	PC2100 (2-2-2)	PC2100 (2-3-3)	PC2100 (2.5-3-3)	PC1600 (2-2-2)
-5B	Yes	Yes	Yes	Yes	Yes	Yes
-6	–	Yes	Yes	Yes	Yes	Yes
-6T	–	Yes	Yes	Yes	Yes	Yes
-75E	–	–	Yes	Yes	Yes	Yes
-75Z	–	–	–	Yes	Yes	Yes
-75	–	–	–	–	Yes	Yes
	-5B	**-6/-6T**	**-75E**	**-75Z**	**-75**	**-75**

Figure 1: 256Mb DDR SDRAM Part Numbers



FBGA Part Marking System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on the Micron Web site: www.micron.com/decoder.

General Description

The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM.

The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte.

The 256Mb DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby effectively providing high bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC standard for SSTL_2. All full drive option outputs are SSTL_2, Class II compatible.

Notes:
1. The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
2. Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes, the lower byte and upper byte. For the lower byte (DQ0 through DQ7) DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8 through DQ15) DM refers to UDM and DQS refers to UDQS.
3. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
4. Any specific requirement takes precedence over a general statement.

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Figure 2: Functional Block Diagram: 64 Meg x 4

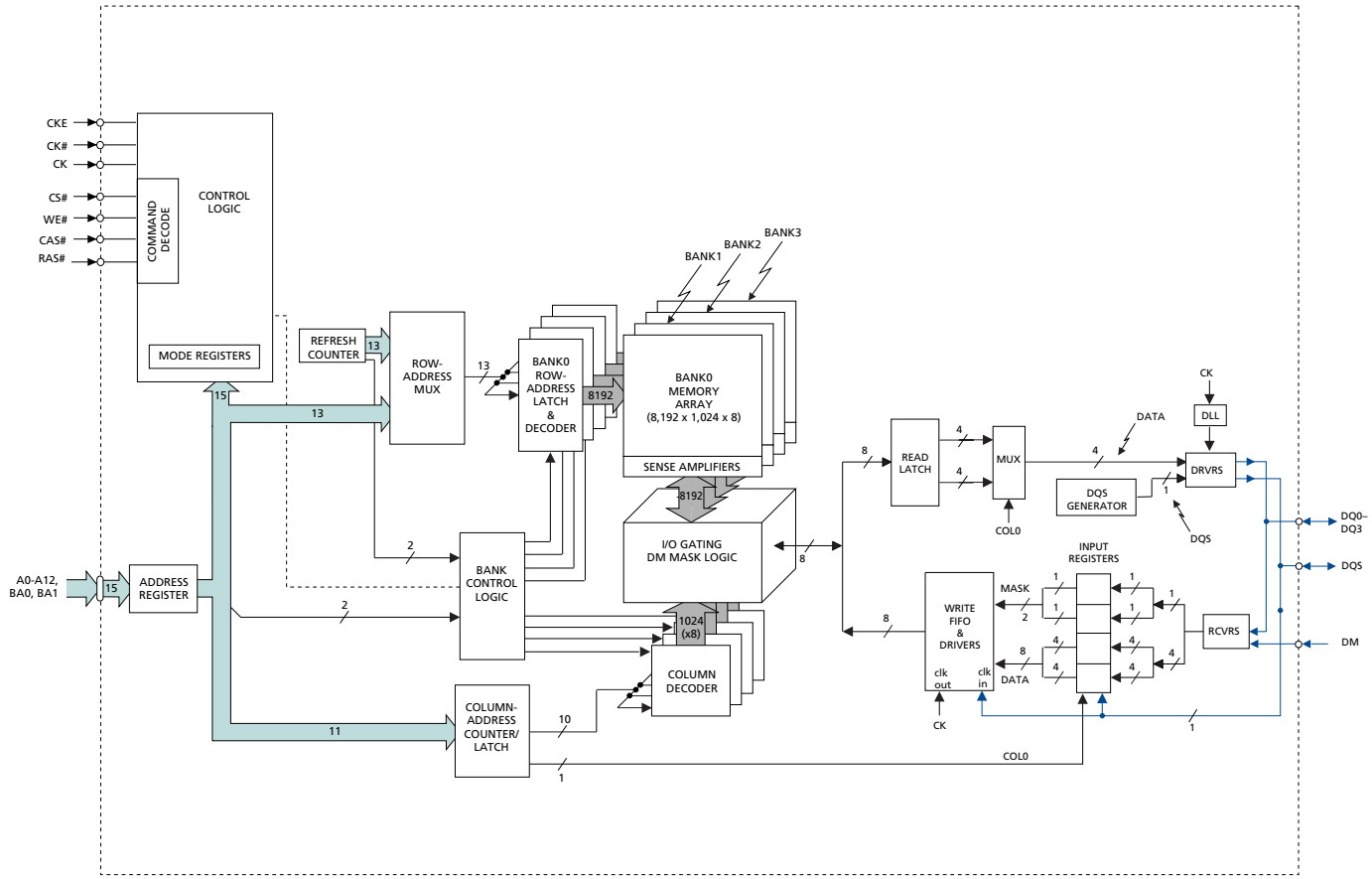


Figure 3: Functional Block Diagram: 32 Meg x 8

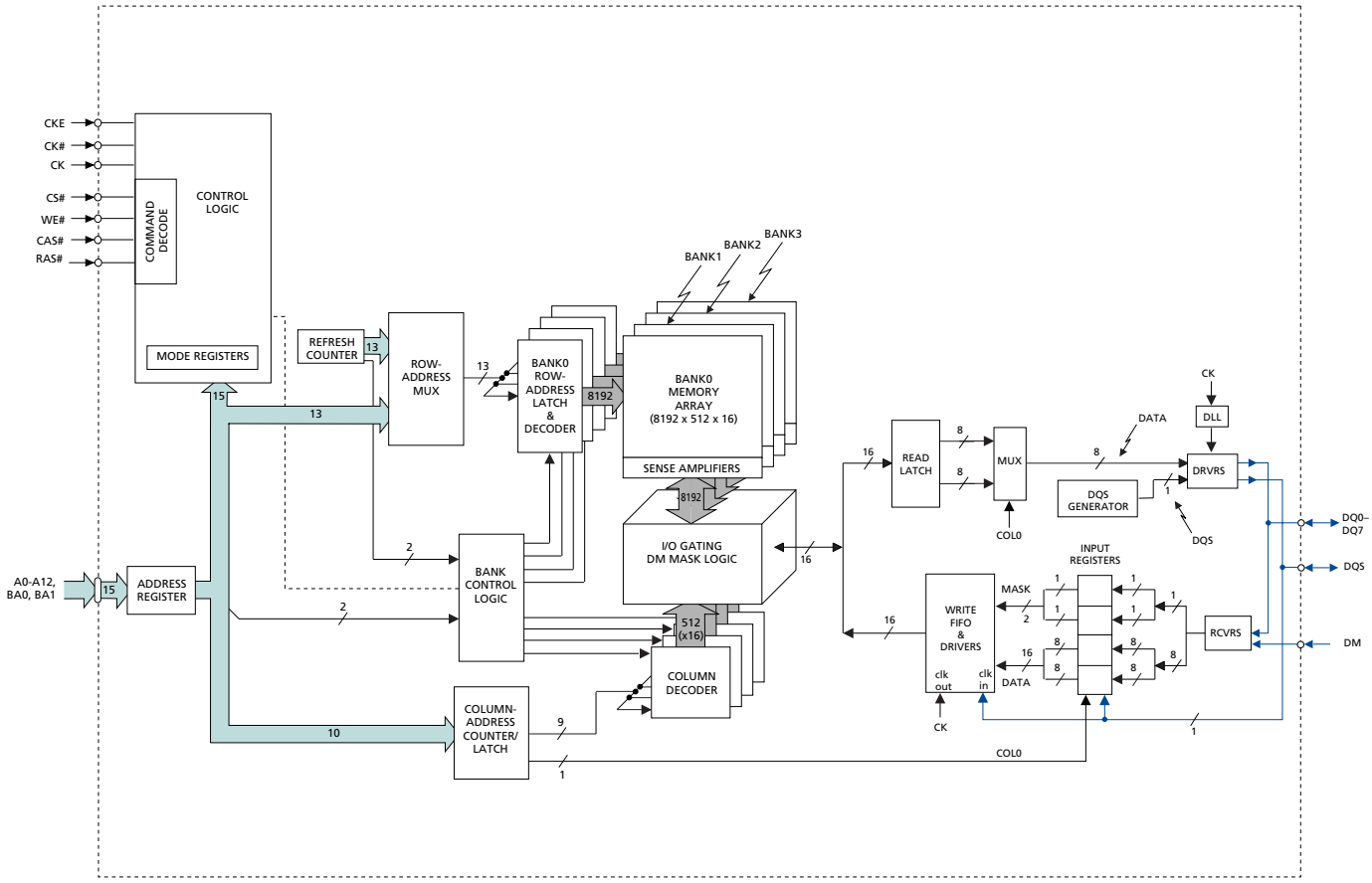
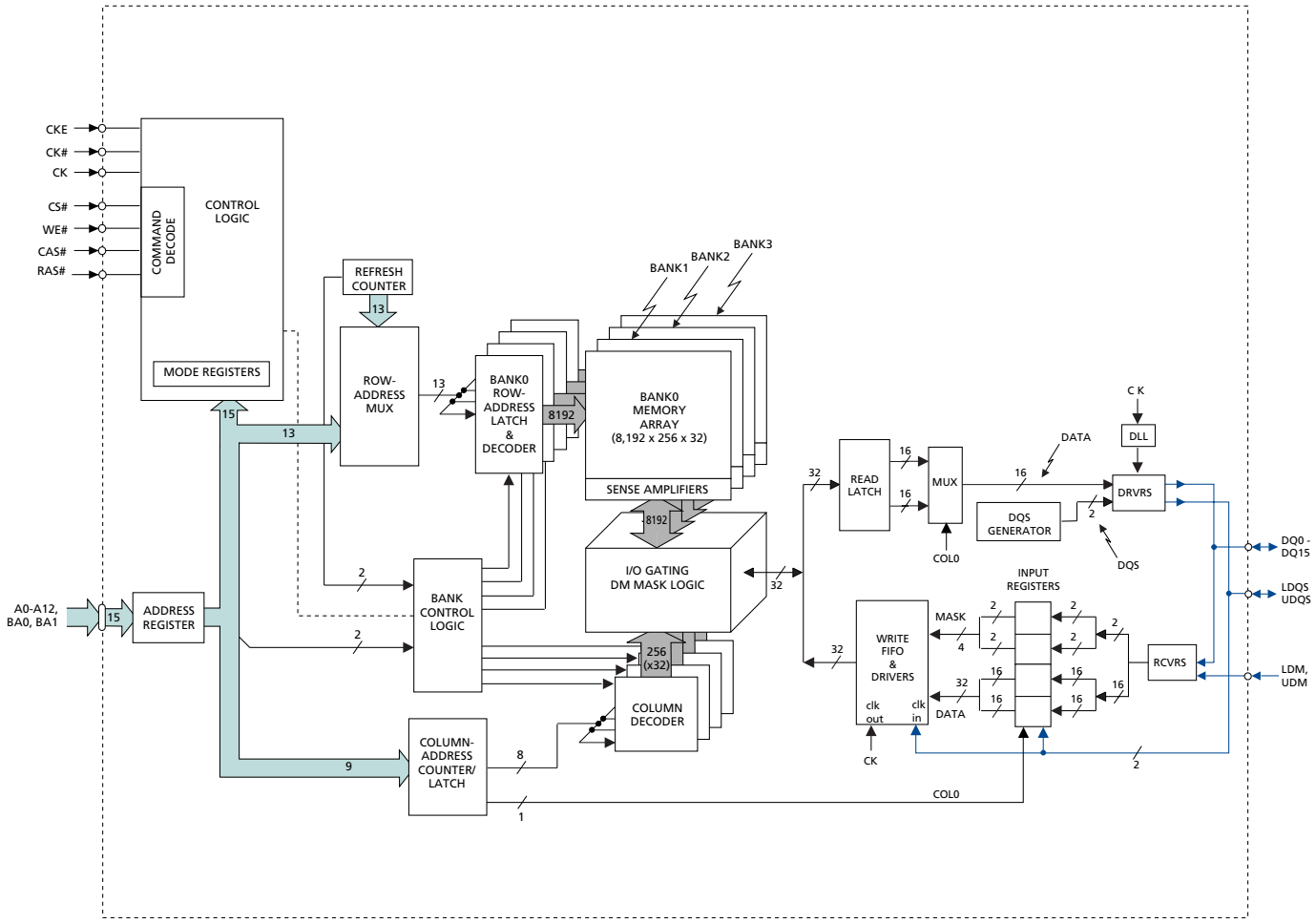


Figure 4: Functional Block Diagram: 16 Meg x 16



Pin/Ball Assignments and Descriptions

Table 4: Ball/Pin Descriptions

FBGA Numbers	TSOP Numbers	Symbol	Type	Description
G2, G3	45, 46	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
H3	44	CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle) or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER- DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought HIGH, after which it becomes a SSTL_2 input only.
H8	24	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
H7, G8, G7	23, 22, 21	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
3F F7, 3F	47 20, 47	DM LDM, UDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. For the x16, LDM is DM for DQ0–DQ7 and UDM is DM for DQ8–DQ15. Pin 20 is a NC on x4 and x8.
J8, J7	26, 27	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
K7, L8, L7, M8, M2, L3, L2, K3, K2, J3, K8, J2, H2	29, 30, 31, 32, 35, 36, 37, 38, 39, 40, 28 41, 42	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
A8, B9, B7, C9, C7, D9, D7, E9, E1, D3, D1, C3, C1, B3, B1, A2	2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ0–DQ2 DQ3–DQ5 DQ6–DQ8 DQ9–DQ11 DQ12–DQ14 DQ15	I/O	Data Input/Output: Data bus for **x16**.
	14, 17, 25, 43, 53	NC	–	No Connect for **x16** These pins should be left unconnected.

Table 4: Ball/Pin Descriptions (Continued)

FBGA Numbers	TSOP Numbers	Symbol	Type	Description
A8, B7, C7, D7, D3, C3, B3, A2	2, 5, 8, 11, 56, 59, 62, 65	DQ0–DQ2 DQ3–DQ5 DQ6, DQ7	I/O	Data Input/Output: Data bus for **x8**.
B1, B9, C1, C9, D1, D9, E1, E7, E9, F7	4, 7, 10, 13, 14, 16, 17, 20, 25, 43, 53, 54, 57, 60, 63,	NC	–	No Connect for **x8** These pins should be left unconnected.
B7, D7, D3, B3	5, 11, 56, 62	DQ0–DQ2 DQ3	I/O	Data Input/Output: Data bus for **x4**.
B1, B9, C1, C9, D1, D9, E1, E7, E9, F7,	4, 7, 10, 13, 14, 16, 17, 20, 25, 43, 53, 54, 57, 60, 63,	NC	–	No Connect for **x4** These pins should be left unconnected.
A2, A8, C3, C7	2, 8, 59, 65	NF	–	No Function for **x4** These pins should be left unconnected.
E3 E7 E3	51 16 51	DQS LDQS UDQS	I/O	Data Strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data. For the x16, LDQS is DQS for DQ0–DQ7 and UDQS is DQS for DQ8–DQ15. Pin 16 (E7) is NC on x4 and x8.
F9	17, 19, 50	DNU	–	Do Not Use: Must float to minimize noise on V_{REF}.
B2, D2, C8, E8, A9	3, 9, 15, 55, 61	$V_{DD}Q$	Supply	DQ Power Supply: +2.5V ±0.2V (+2.6V ±0.1V for DDR400). Isolated on the die for improved noise immunity.
A1, C2, E2, B8, D8	6, 12, 52, 58, 64	$V_{SS}Q$	Supply	DQ Ground: Isolated on the die for improved noise immunity.
F8, M7, A7	1, 18, 33	V_{DD}	Supply	Power Supply: +2.5V ±0.2V (+2.6V ±0.1V for DDR400).
A3, F2, M3	34, 48, 66	V_{SS}	Supply	Ground.
F1	49	V_{REF}	Supply	SSTL_2 reference voltage.

Table 5: Reserved NC Balls and Pins

NC pins not listed may also be reserved for other uses; this table defines NC pins of importance.

FBGA Numbers	TSOP Numbers	Symbol	Type	Description
F9	17	A13	I	Address input A13 for 1Gb devices. DNU for FBGA.

Figure 5: Pin Assignment (Top View) 66-Pin TSOP

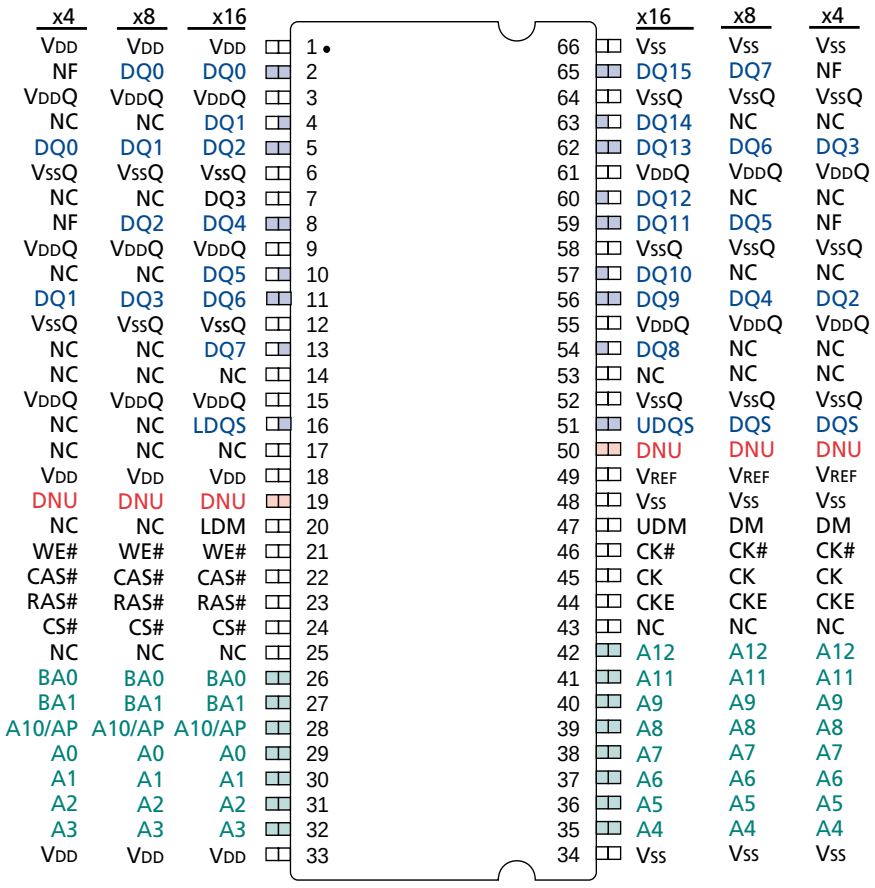


Figure 6: 60-Ball FBGA Ball Assignment (Top View)

x4 (Top View)

1	2	3	4	5	6	7	8	9
VSSQ	NF	VSS		A		VDD	NF	VDDQ
NC	VDDQ	DQ3		B		DQ0	VSSQ	NC
NC	VSSQ	NF		C		NF	VDDQ	NC
NC	VDDQ	DQ2		D		DQ1	VSSQ	NC
NC	VSSQ	DQS		E		NC	VDDQ	NC
VREF	VSS	DM		F		NC	VDD	DNU
	CK	CK#		G		WE#	CAS#	
	A12	CKE		H		RAS#	CS#	
	A11	A9		J		BA1	BA0	
	A8	A7		K		A0	A10	
	A6	A5		L		A2	A1	
	A4	VSS		M		VDD	A3	

x8 (Top View)

1	2	3	4	5	6	7	8	9
VSSQ	DQ7	VSS		A		VDD	DQ0	VDDQ
NC	VDDQ	DQ6		B		DQ1	VSSQ	NC
NC	VSSQ	DQ5		C		DQ2	VDDQ	NC
NC	VDDQ	DQ4		D		DQ3	VSSQ	NC
NC	VSSQ	DQS		E		NC	VDDQ	NC
VREF	VSS	DM		F		NC	VDD	DNU
	CK	CK#		G		WE#	CAS#	
	A12	CKE		H		RAS#	CS#	
	A11	A9		J		BA1	BA0	
	A8	A7		K		A0	A10	
	A6	A5		L		A2	A1	
	A4	VSS		M		VDD	A3	

x16 (Top View)

1	2	3	4	5	6	7	8	9
VSSQ	DQ15	VSS		A		VDD	DQ0	VDDQ
DQ14	VDDQ	DQ13		B		DQ2	VSSQ	DQ1
DQ12	VSSQ	DQ11		C		DQ4	VDDQ	DQ3
DQ10	VDDQ	DQ9		D		DQ6	VSSQ	DQ5
DQ8	VSSQ	UDQS		E		LDQS	VDDQ	DQ7
VREF	VSS	UDM		F		LDM	VDD	DNU
	CK	CK#		G		WE#	CAS#	
	A12	CKE		H		RAS#	CS#	
	A11	A9		J		BA1	BA0	
	A8	A7		K		A0	A10	
	A6	A5		L		A2	A1	
	A4	VSS		M		VDD	A3	

Functional Description

The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. The 256Mb DDR SDRAM is internally configured as a quad-bank DRAM.

The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a 2*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Initialization

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to V_{DD} and $V_{DD}Q$ simultaneously, and then to V_{REF} (and to the system V_{TT}). V_{TT} must be applied after $V_{DD}Q$ to avoid device latch-up, which may cause permanent damage to the device. V_{REF} can be applied any time after $V_{DD}Q$ but is expected to be nominally coincident with V_{TT}. Except for CKE, inputs are not recognized as valid until after V_{REF} is applied. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied. After CKE passes through V_{IH}, it will transition to a SSTL_2 signal and remain as such until power is cycled. Maintaining an LVCMOS LOW level on CKE during power-up is required to ensure that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200µs delay prior to applying an executable command.

Once the 200µs delay has been satisfied, a DESELECT or NOP command should be applied and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a LOAD MODE REGISTER command should be issued for the extended mode register (BA1 LOW and BA0 HIGH) to enable the DLL, followed by another LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL and to program the operating parameters. Two hundred clock cycles are required between the DLL reset and any READ command. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed (^{t}RFC must be satisfied). Additionally, a LOAD MODE REGISTER command for the mode register with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) is required. Following these requirements, the DDR SDRAM is ready for normal operation.

Register Definition

Mode Register

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 7 on page 16. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length; A3 specifies the type of burst (sequential or interleaved); A4–A6 specify the CAS latency; and A7–A12 specify the operating mode.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 7. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

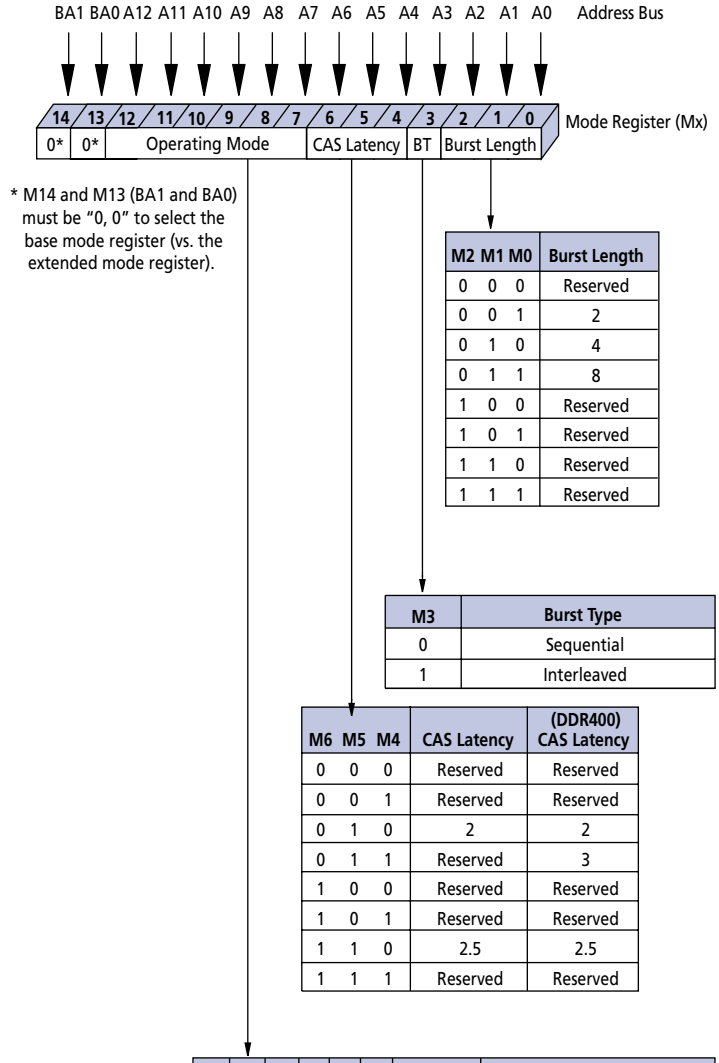
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A*i* when the burst length is set to two, by A2–A*i* when the burst length is set to four, and by A3-A*i* when the burst length is set to eight (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 6, “Burst Definition,” on page 17.

Figure 7: Mode Register Definition



M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	CAS Latency	(DDR400) CAS Latency
0	0	0	Reserved	Reserved
0	0	1	Reserved	Reserved
0	1	0	2	2
0	1	1	Reserved	3
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	2.5	2.5
1	1	1	Reserved	Reserved

M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	All other states reserved

Table 6: Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2	–	–	A0	–	–
	–	–	0	0-1	0-1
	–	–	1	1-0	1-0
4	–	A1	A0	–	–
	–	0	0	0-1-2-3	0-1-2-3
	–	0	1	1-2-3-0	1-0-3-2
	–	1	0	2-3-0-1	2-3-0-1
	–	1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0	–	–
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes: 1. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
2. For a burst length of two, A1–A*i* select the two-data-element block; A0 selects the first access within the block.
3. For a burst length of four, A2–A*i* select the four-data-element block; A0–A1 select the first access within the block.
4. For a burst length of eight, A3–A*i* select the eight-data-element block; A0–A2 select the first access within the block.

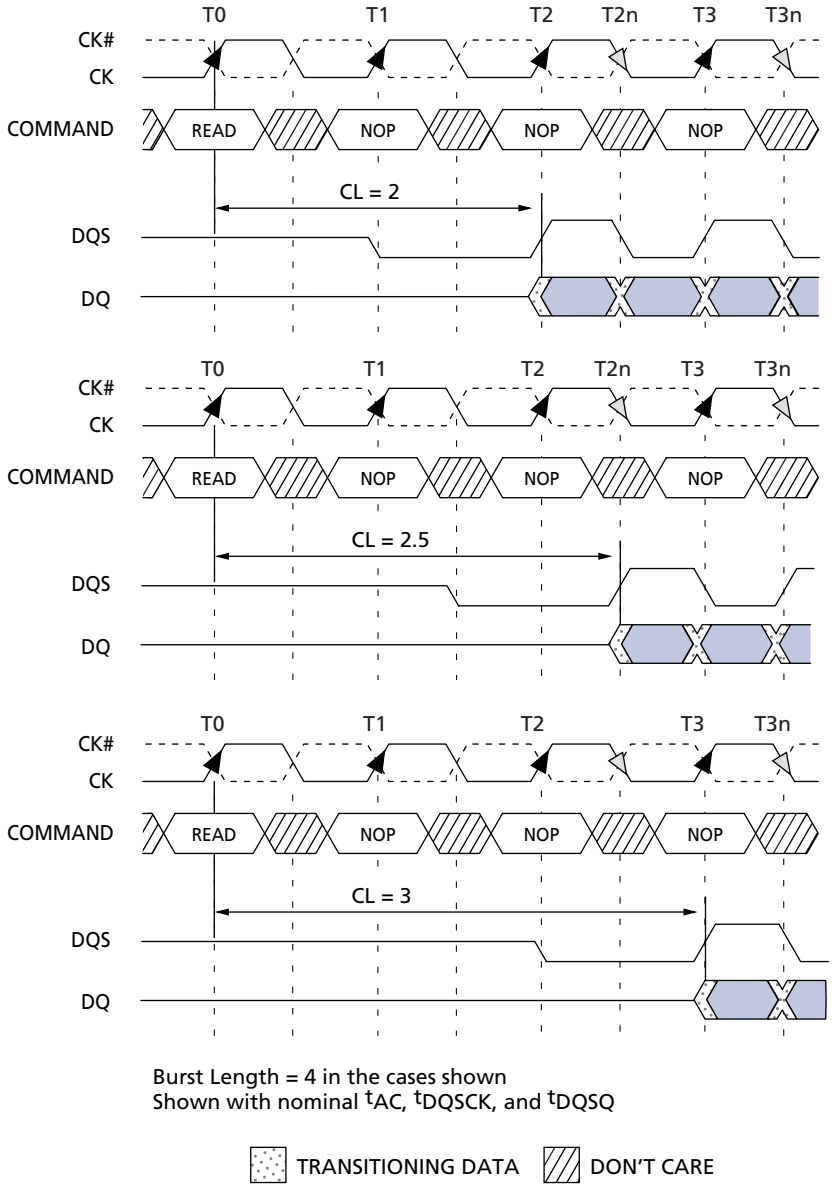
Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2, 2.5, or 3 (DDR400 only) clocks, as shown in Figure 8 on page 18.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. Table 7, "CAS Latency (CL)," on page 18 indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Figure 8: CAS Latency



Burst Length = 4 in the cases shown
Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ

Table 7: CAS Latency (CL)

Speed	Allowable Operating Clock Frequency (MHz)		
	CL = 2	CL = 2.5	CL = 3
-5B	75 ≤ f ≤ 133	75 ≤ f ≤ 167	133 ≤ f ≤ 200
-6/-6T	75 ≤ f ≤ 133	75 ≤ f ≤ 167	–
-75E	75 ≤ f ≤ 133	75 ≤ f ≤ 133	–
-75Z	75 ≤ f ≤ 133	75 ≤ f ≤ 133	–
-75	75 ≤ f ≤ 100	75 ≤ f ≤ 133	–

Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7–A12 each set to zero and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9–A12 each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7–A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable and output drive strength. These functions are controlled via the bits shown in Figure 9 on page 20. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL. Anytime a DLL reset occurs, 200 clock cycles with CKE high is required before a READ command can be issued.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

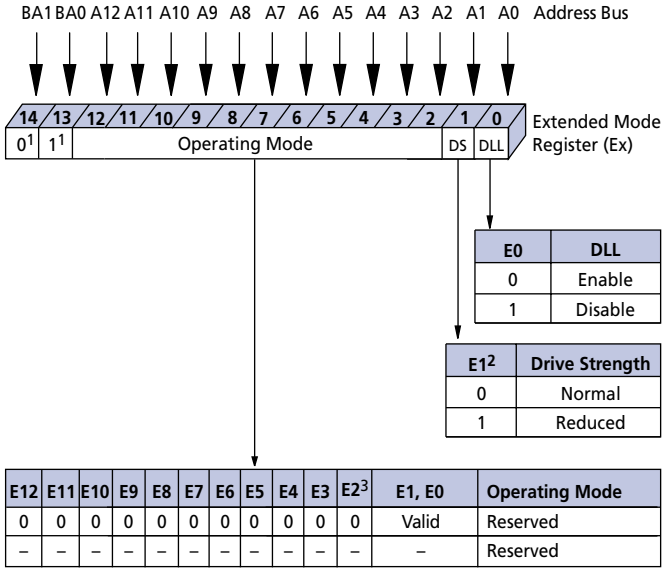
Output Drive Strength

The normal drive strength for all outputs are specified to be SSTL_2, Class II. The x16 supports a programmable option for reduced drive. This option is intended for the support of the lighter load and/or point-to-point environments. The selection of the reduced drive strength will alter the DQ pins and DQS pins from SSTL_2, Class II drive strength to a reduced drive strength, which is approximately 54 percent of the SSTL_2, Class II drive strength.

DLL Enable/Disable

When the part is running without the DLL enabled, device functionality may be altered. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, a DLL Reset and 200 clock cycles with CKE high must occur before a READ command can be issued.

Figure 9: Extended Mode Register Definition



E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2[3]	E1, E0	Operating Mode
0	0	0	0	0	0	0	0	0	0	0	Valid	Reserved
–	–	–	–	–	–	–	–	–	–	–	–	Reserved

Notes: 1. E14 and E13 (BA1 and BA0) must be “0, 1” to select the extended mode register vs. the base mode register.
2. The reduced drive strength option is not supported on the x4 and x8 versions; it is only available on the x16 version.
3. The QFC# option is not supported.

Commands

Table 8 and Table 9 provide a quick reference of available commands, followed by a description of each command. Two additional truth tables, Table 11 on page 49, and Table 12 on page 51, appear following the Operation section, provide current state/next state information.

Table 8: Truth Table – Commands

Note 1 applies to all commands.

Name (Function)	CS#	RAS#	CAS#	WE#	Addr	Notes
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0–BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register;
   BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A12 provide the op-code to be written to the selected mode register.
3. BA0–BA1 provide bank address and A0–A12 provide row address.
4. BA0–BA1 provide bank address; A0–A*i* provide column address, (where *i* = 8 for x16, *i* = 9 for x8, and *i* = 9,11 for x4) A10 HIGH enables the auto precharge feature (non persistent); and A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0–BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0–BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; within the self refresh mode, all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to READ bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
9. DESELECT and NOP are functionally interchangeable.

Table 9: Truth Table – DM Operation

Note 1 applies to all commands.

Name (Function)	DM	DQ
Write Enable	L	Valid
Write Inhibit	H	X

Notes:
1. Used to mask write data; provided coincident with the corresponding data.

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CS# is LOW with RAS#, CAS#, and WE# are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0–A12. See mode register descriptions in the Register Definition section on page 15. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where *i* = 8 for x16, 9 for x8, or 9, 11 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where *i* = 8 for x16, 9 for x8, or 9, 11 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate

any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise, BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging.

Auto Precharge

Auto precharge is a feature that performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This earliest valid stage is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating ^{t}RAS (MIN), as described for each burst type in the Operation section of this data sheet. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed.

BURST TERMINATE

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet. The open page, which the READ burst was terminated from, remains open.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All banks must be idle before an AUTO REFRESH command is issued.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 256Mb DDR SDRAM requires AUTO REFRESH cycles at an average interval of 7.8125µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 x 7.8125µs (70.3µs). Note that the JEDEC specification only allows 8 x 7.8125µs; thus, the Micron specification exceeds the JEDEC requirement by one clock. This maximum absolute interval is to allow future support for DLL updates internal to the DDR SDRAM to be restricted to AUTO REFRESH cycles, without allowing excessive drift in ^{t}AC between updates.

Although not a JEDEC requirement, to provide for future functionality, CKE must be active (HIGH) during the auto refresh period. The auto refresh period begins when the AUTO REFRESH command is registered and ends ^{t}RFC later.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled upon exiting SELF REFRESH. (A DLL reset and 200 clock cycles must then occur before a READ command can be issued.) Input signals except CKE are "Don't Care" during SELF REFRESH. VREF voltage is also required for the full duration of the SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK and CK# must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for ^{t}XSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for ^{t}XSRD time, then a DLL reset and NOPs for 200 additional clock cycles before applying a READ. Any command besides a READ can be performed ^{t}XSNR MIN after the DLL reset. NOP or DESELECT commands must be issued during the ^{t}XSNR MIN time.

Operations

Bank/Row Activation

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 10.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 133 MHz clock (7.5ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 11, which covers any case where $2 < {}^{t}\text{RCD (MIN)} / {}^{t}\text{CK} \leq 3$. (Figure 11 also shows the same case for ^{t}RRD; the same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 10: Activating a Specific Row in a Specific Bank

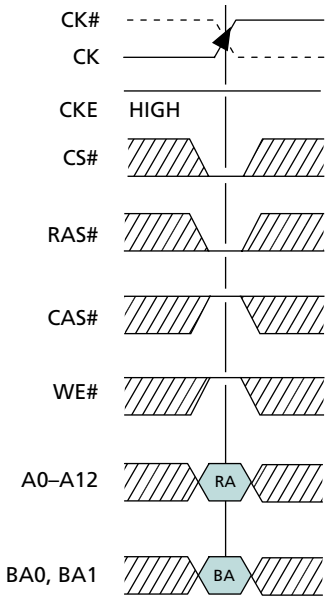
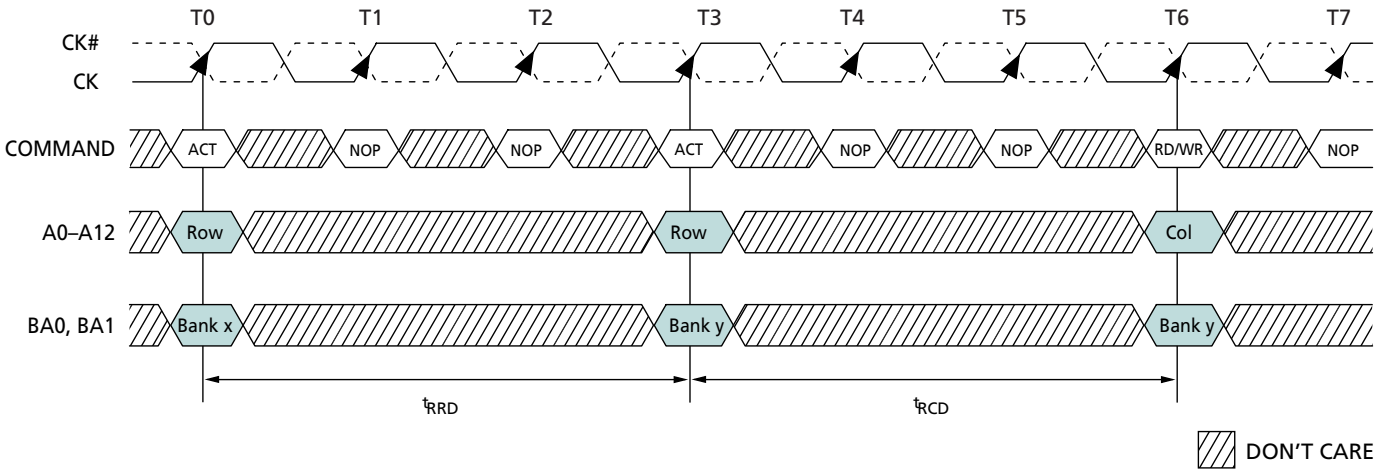


Figure 11: Example: Meeting ^{t}RCD (^{t}RRD) MIN When 2 < ^{t}RCD (^{t}RRD) MIN/^{t}CK ≤ 3



READs

READ bursts are initiated with a READ command, as shown in Figure 12 on page 28.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst.

Note: For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CK#). Figure 13 on page 29 shows general timing for each possible CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), and the valid data window are depicted in Figure 40 on page 77 and Figure 41 on page 78. A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) and ^{t}AC (data-out transition skew to CK) is depicted in Figure 42 on page 79.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued *x* cycles after the first READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture). This is shown in Figure 14 on page 30. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is illustrated in Figure 15, “Nonconsecutive READ Bursts,” on page 31. Full-speed random read accesses within a page (or pages) can be performed as shown in Figure 16, “Random READ Accesses,” on page 32.

Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 17 on page 33. The BURST TERMINATE latency is equal to the read (CAS) latency; i.e., the BURST TERMINATE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 18 on page 34. The ^{t}DQSS (NOM) case is shown; the ^{t}DQSS (MAX) case has a longer bus idle time. (^{t}DQSS [MIN] and ^{t}DQSS [MAX] are defined in the section on WRITEs.)

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated.

The PRECHARGE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture). This is shown in Figure 19 on page 35. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until both ^{t}RAS and ^{t}RP have been met. Note that part of the row precharge time is hidden during the access of the last data elements.

Figure 12: READ Command

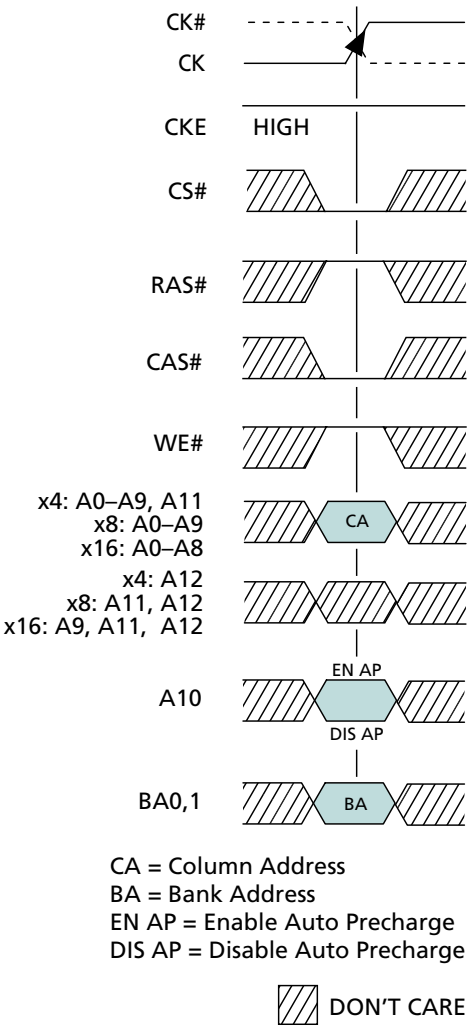
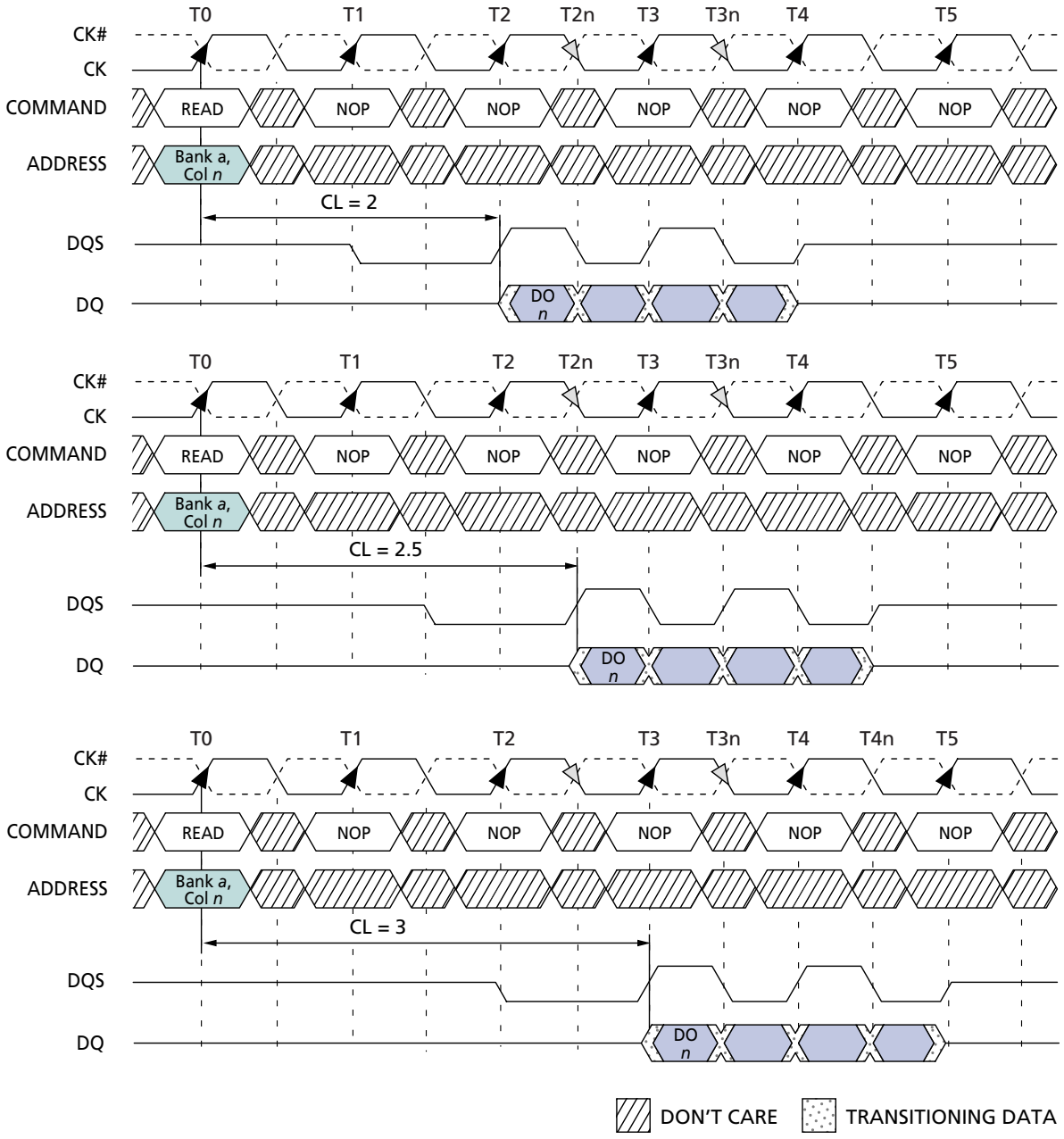
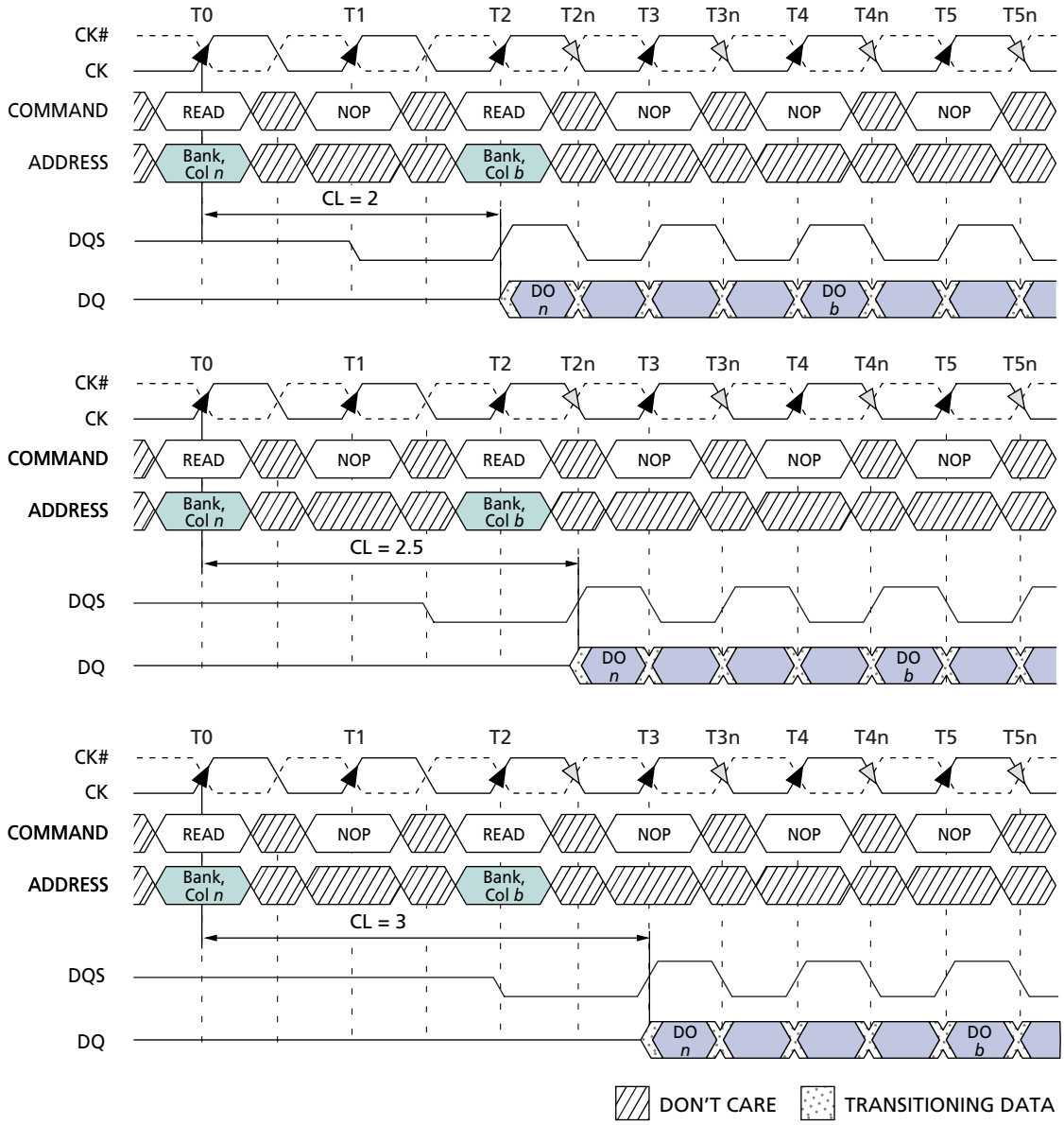


Figure 13: READ Burst



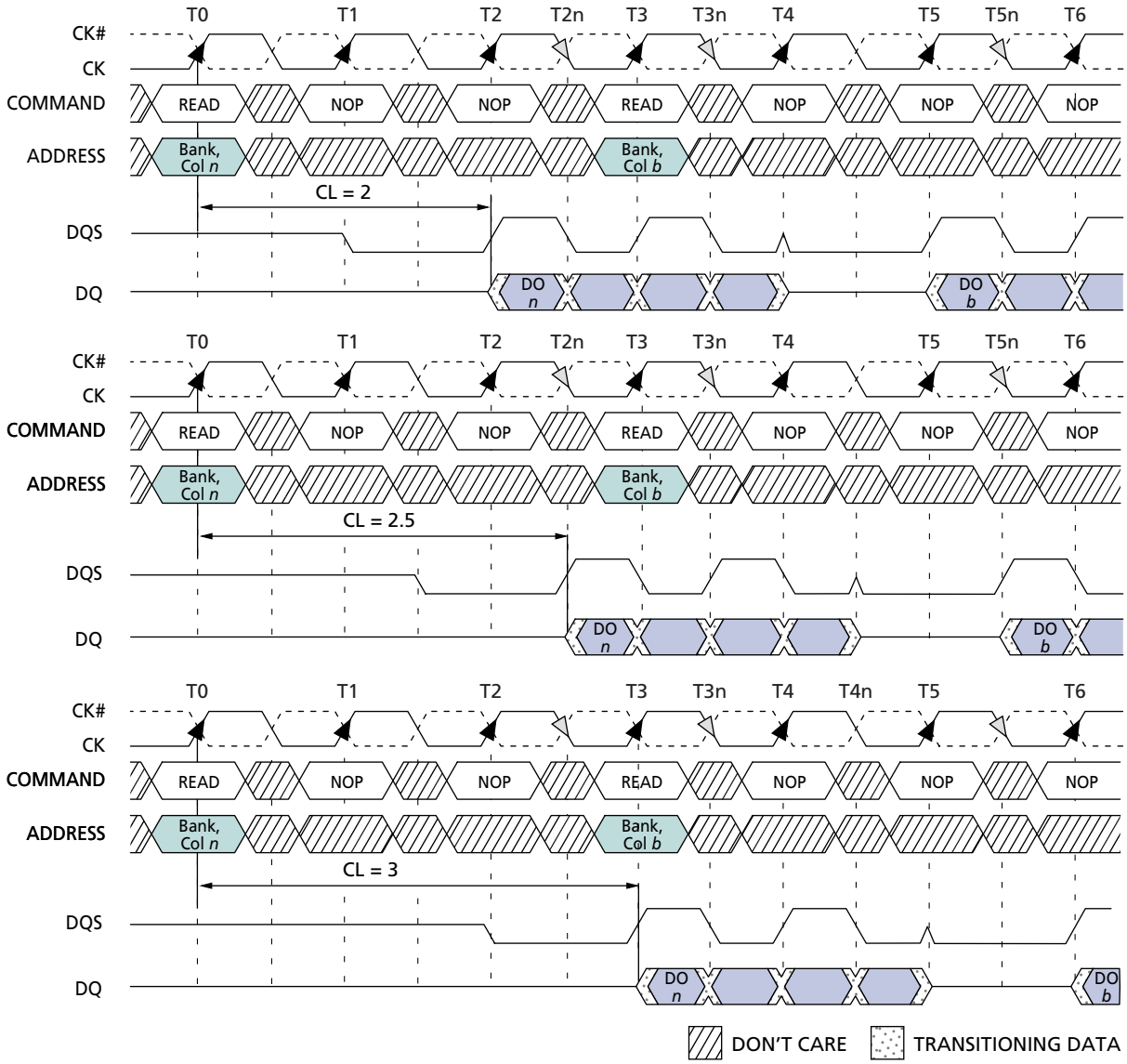
Notes: 1. DO *n* = data-out from column *n*.
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 14: Consecutive READ Bursts



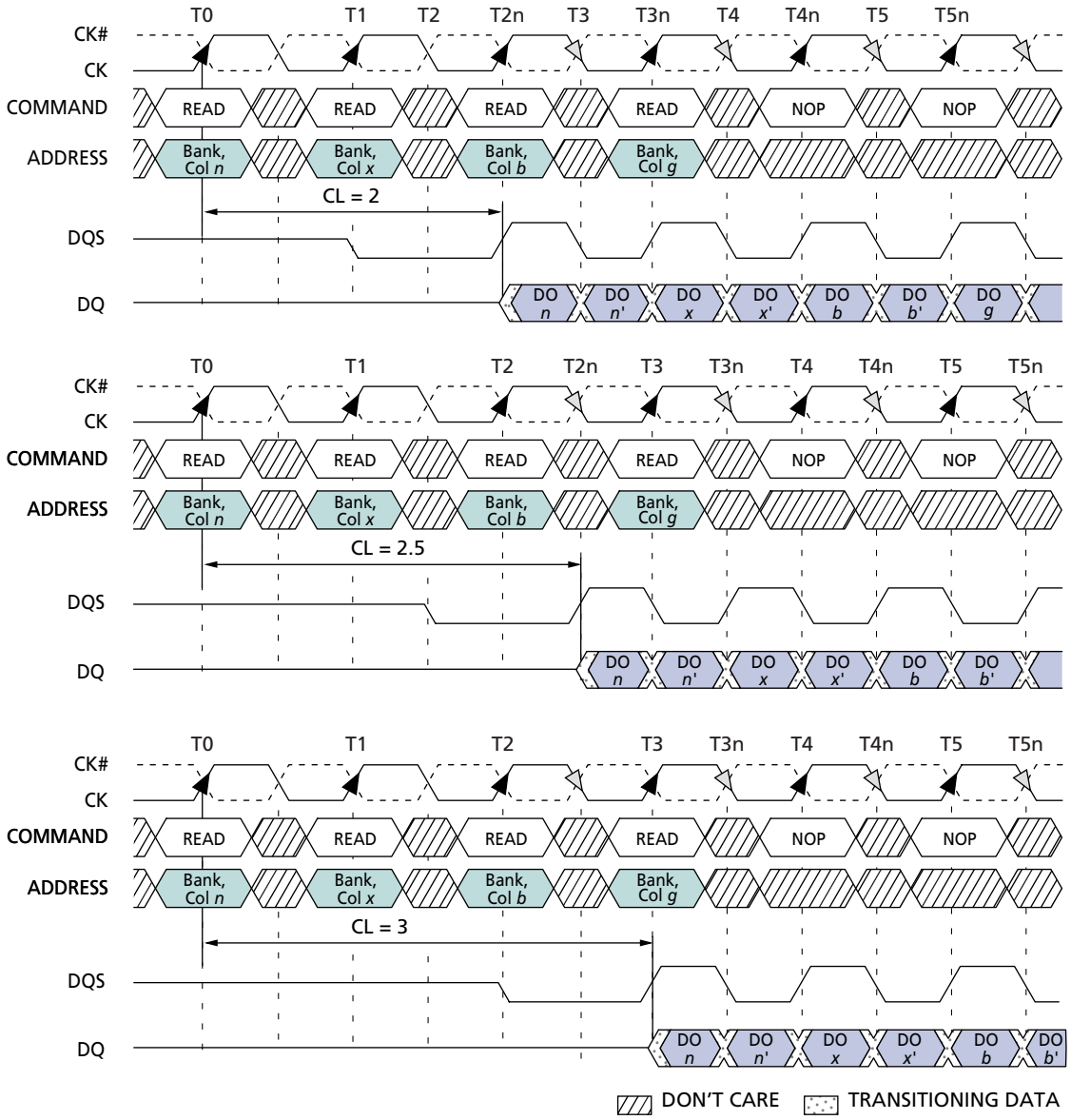
Notes:
1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first).
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three (or seven) subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies only when READ commands are issued to the same device.

Figure 15: Nonconsecutive READ Bursts



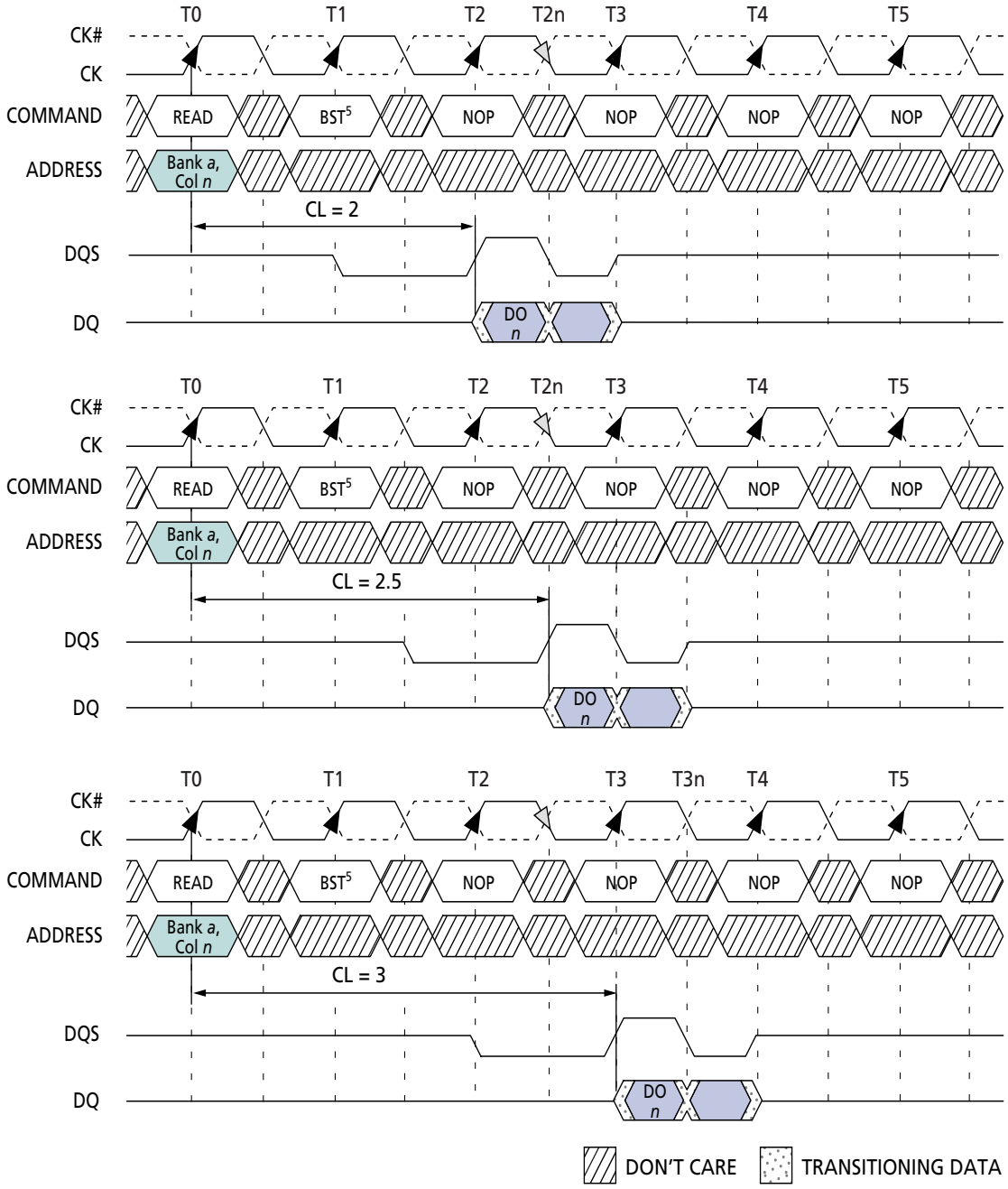
Notes: 1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first).
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three (or seven) subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 16: Random READ Accesses



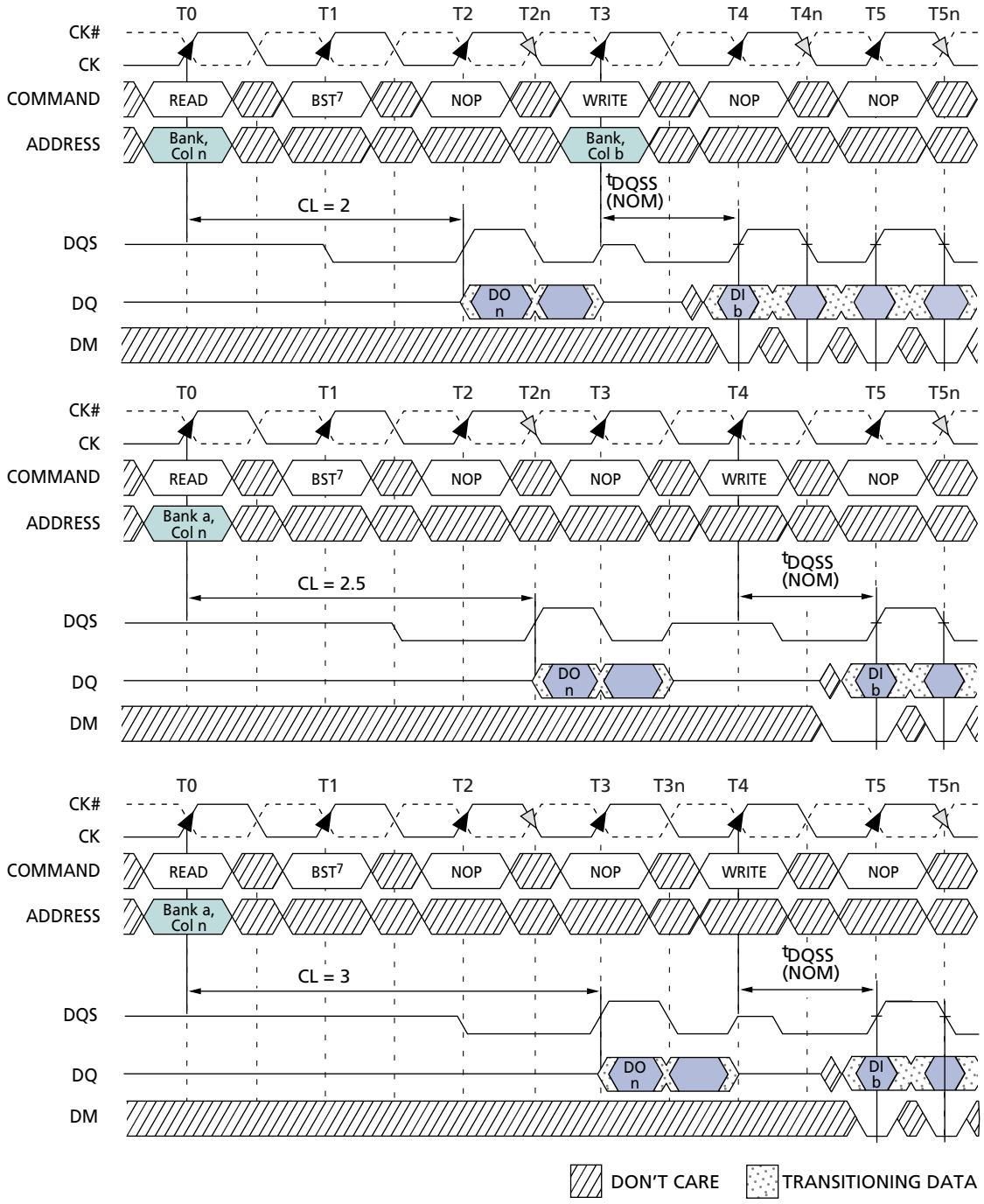
Notes:
1. DO *n* (or *x* or *b* or *g*) = data-out from column *n* (or column *x* or column *b* or column *g*).
2. BL = 2, 4, or 8 (if 4 or 8, the following burst interrupts the previous).
3. *n*' or *x*' or *b*' or *g*' indicates the next data-out following DO *n* or DO *x* or DO *b* or DO *g*, respectively.
4. READs are to an active row in any bank.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 17: Terminating a READ Burst



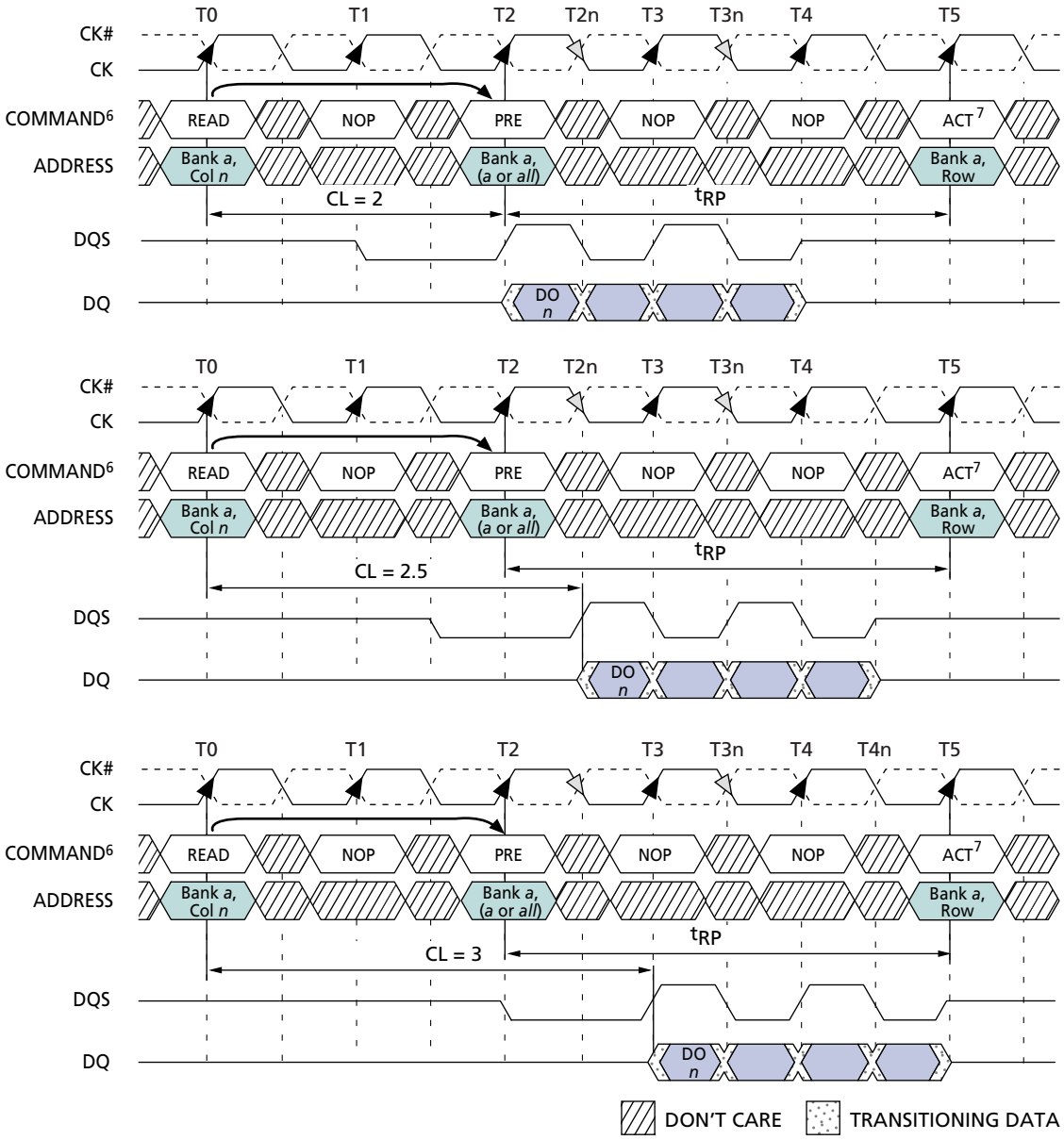
Notes:
1. DO *n* = data-out from column *n*.
2. BL = 4 or 8.
3. Subsequent element of data-out appears in the programmed order following DO *n*.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
5. BST = BURST TERMINATE command; page remains open.

Figure 18: READ-to-WRITE



Notes:
1. DO *n* = data-out from column *n*.
2. DI *b* = data-in from column *b*.
3. BL = 4 in the cases shown (applies for bursts of 8 as well; if the burst length is 2, the BST command shown can be NOP).
4. One subsequent element of data-out appears in the programmed order following DO *n*.
5. Data-in elements are applied following DI *b* in the programmed order.
6. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
7. BST = BURST TERMINATE command; page remains open.

Figure 19: READ-to-PRECHARGE



Notes:
1. DO *n* = data-out from column *n*.
2. BL = 4, or an interrupted burst of 8.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
5. READ to PRECHARGE equals two clocks, which allows two data pairs of data-out.
6. A READ command with AUTO-PRECHARGE enabled, provided ^{t}RAS (MIN) is met, would cause a precharge to be performed at *x* number of clock cycles after the READ command, where *x* = BL/2.
7. An active command to the same bank is only allowed if ^{t}RC (MIN) has been satisfied.
8. PRE = PRECHARGE command; ACT = ACTIVE command.

WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 20.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst and after the ^{t}WR time.

Note: For the WRITE commands used in the following illustrations, auto precharge is disabled.

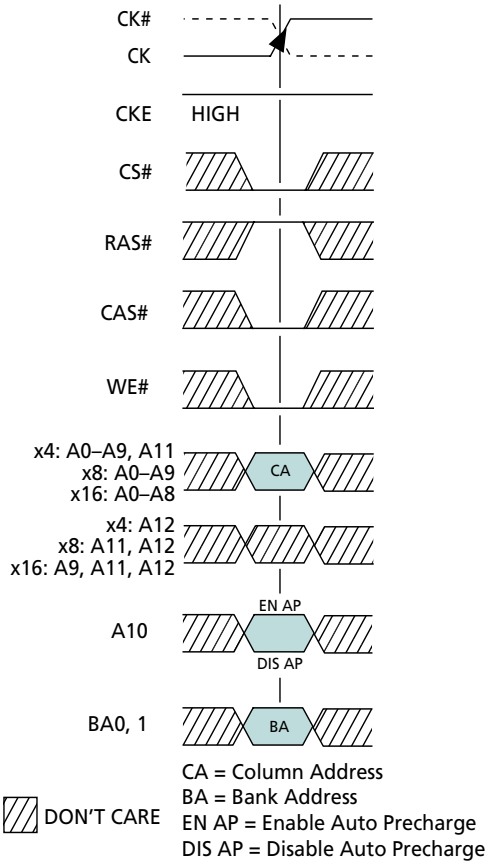
During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS (^{t}DQSS) is specified with a relatively wide range (from 75 percent to 125 percent of one clock cycle and 72 percent to 128 percent for DDR400). All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., ^{t}DQSS [MIN] and ^{t}DQSS [MAX]) might not be intuitive, they have also been included. Figure 21 on page 38 shows the nominal case and the extremes of ^{t}DQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

Figure 22 on page 39 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 23 on page 40. Full-speed random write accesses within a page or pages can be performed as shown in Figure 24 on page 40.

Figure 20: WRITE Command



Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst, ^{t}WTR should be met as shown in Figure 25 on page 41.

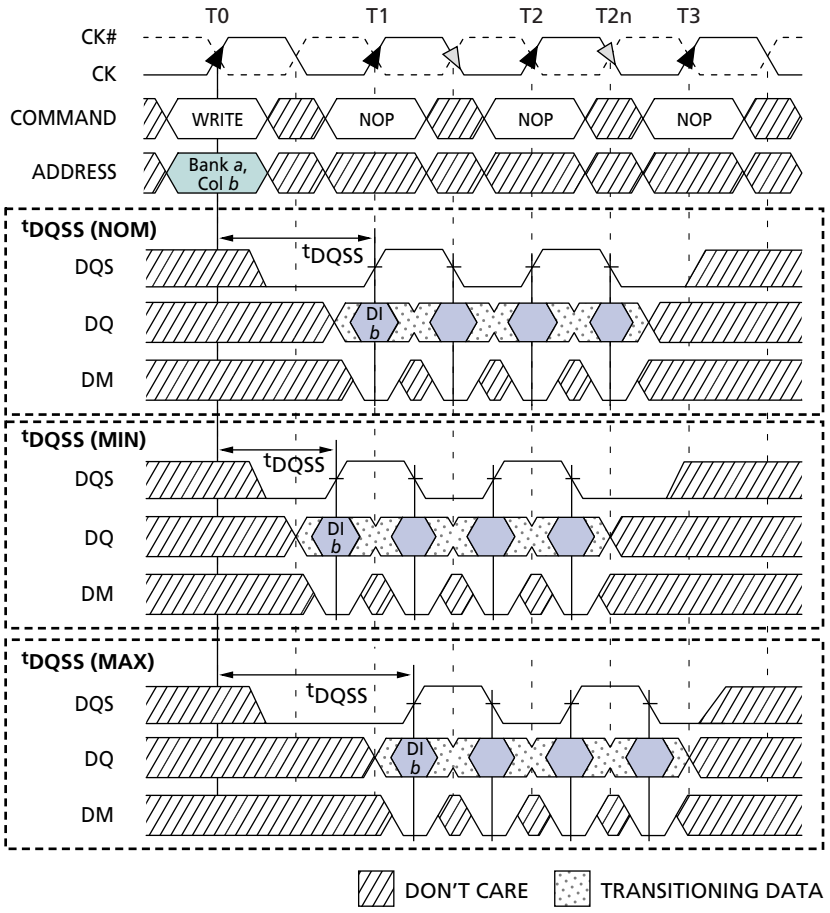
Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figure 26 on page 42.

Note that only the data-in pairs that are registered prior to the ^{t}WTR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 27 on page 43.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, ^{t}WR should be met as shown in Figure 28 on page 44.

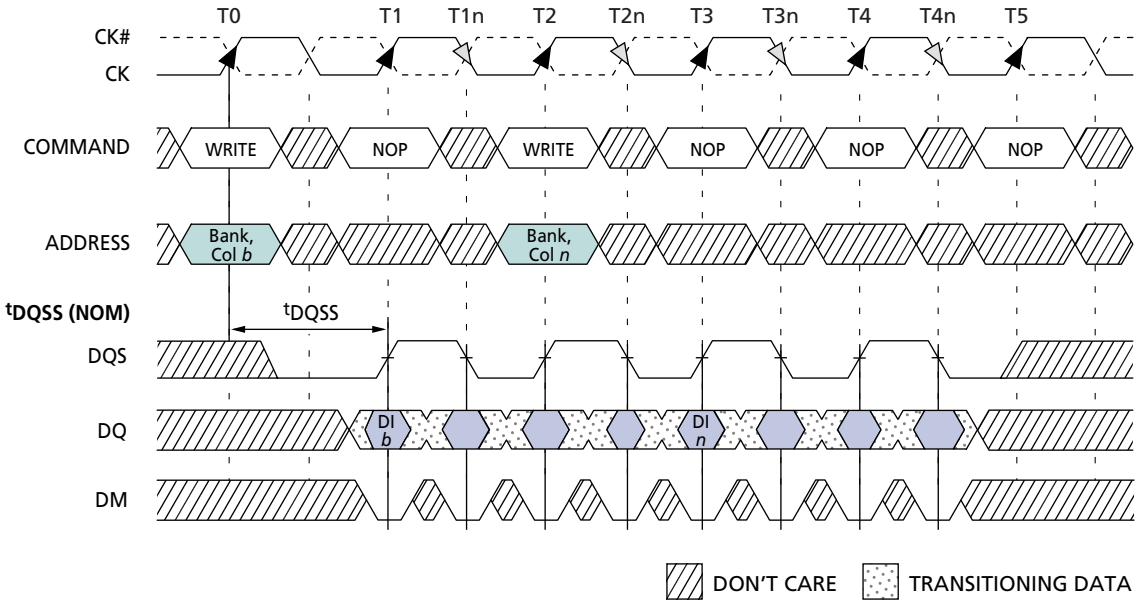
Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure 29 on page 45 and Figure 30 on page 46. Note that only the data-in pairs that are registered prior to the ^{t}WR period are written to the internal array, and any subsequent data-in should be masked with DM as shown in Figures 29 and 30. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

Figure 21: WRITE Burst



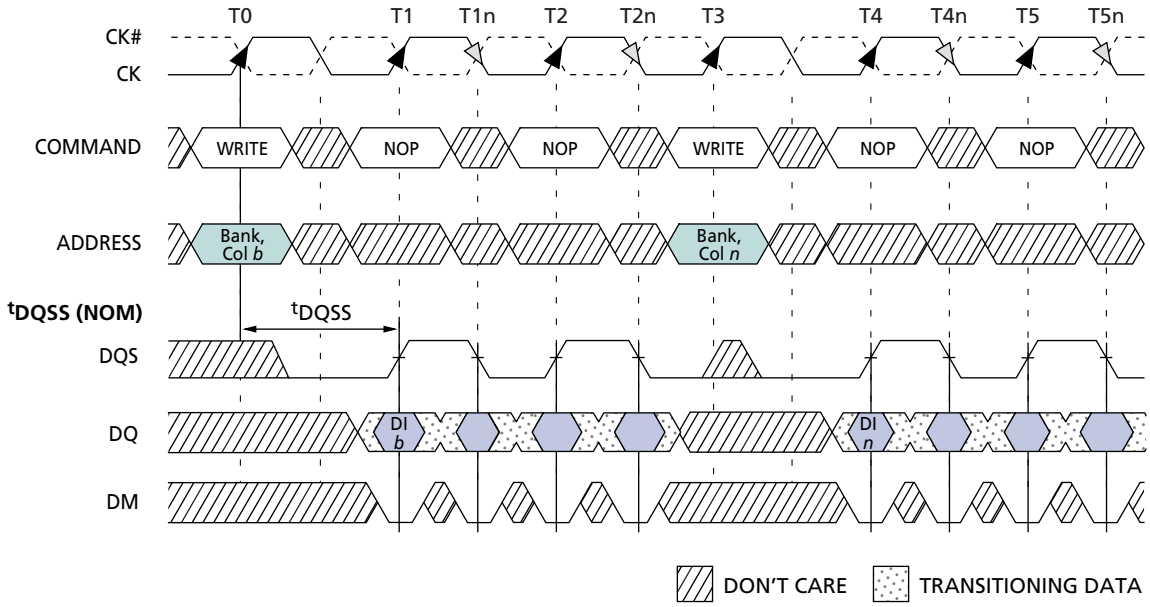
Notes:
1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. An uninterrupted burst of 4 is shown.
4. A10 is LOW with the WRITE command (auto precharge is disabled).

Figure 22: Consecutive WRITE-to-WRITE



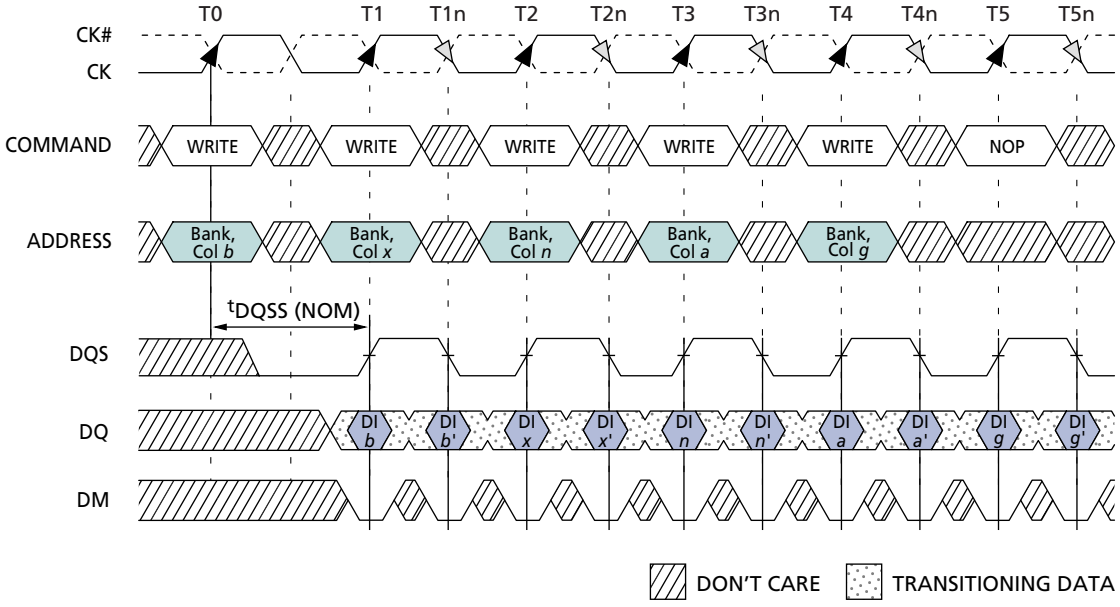
Notes:
1. DI *b*, etc., = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. An uninterrupted burst of 4 is shown.
5. Each WRITE command may be to any bank.

Figure 23: Nonconsecutive WRITE-to-WRITE



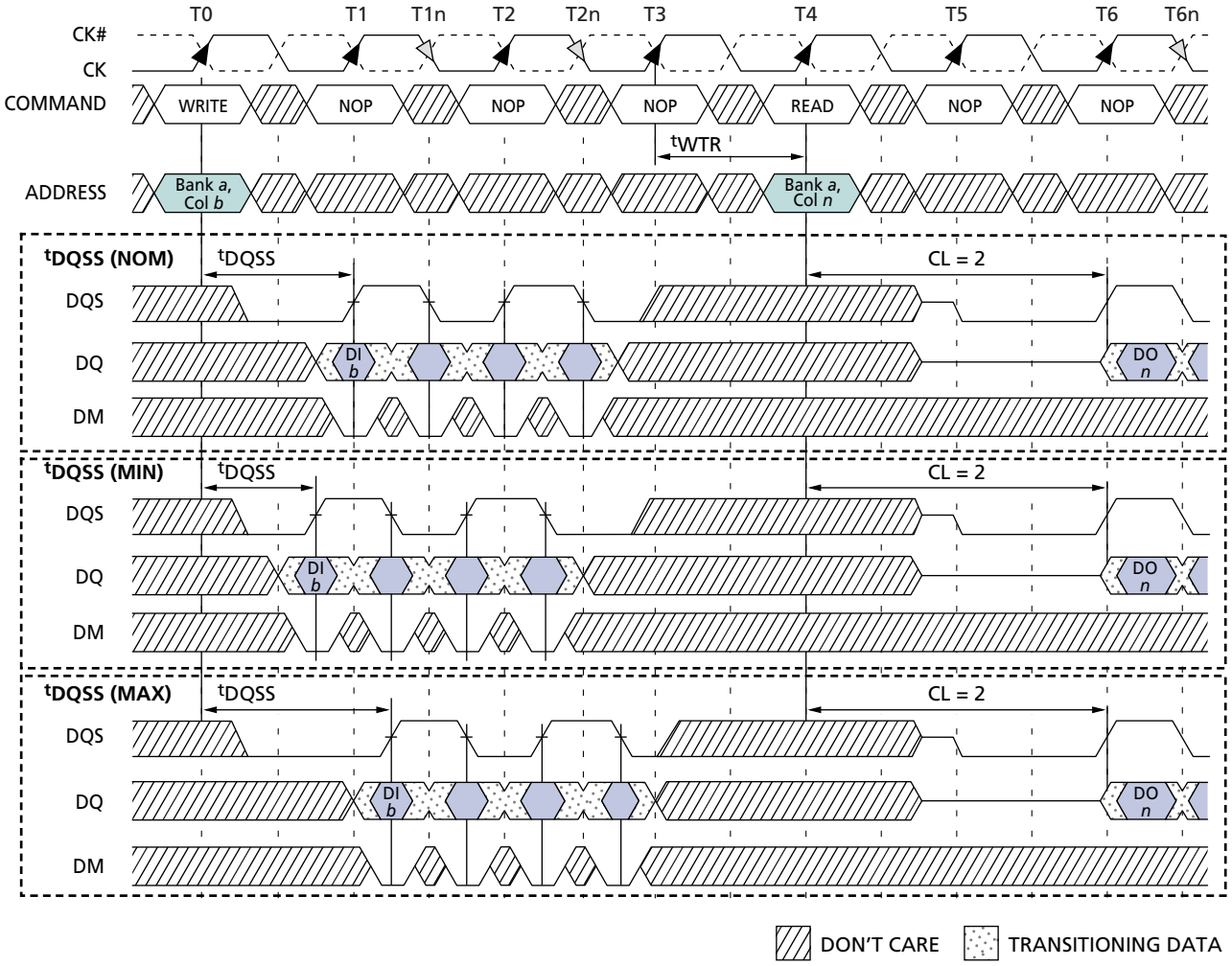
Notes: 1. DI *b*, etc., = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. An uninterrupted burst of 4 is shown.
5. Each WRITE command may be to any bank.

Figure 24: Random WRITE Cycles



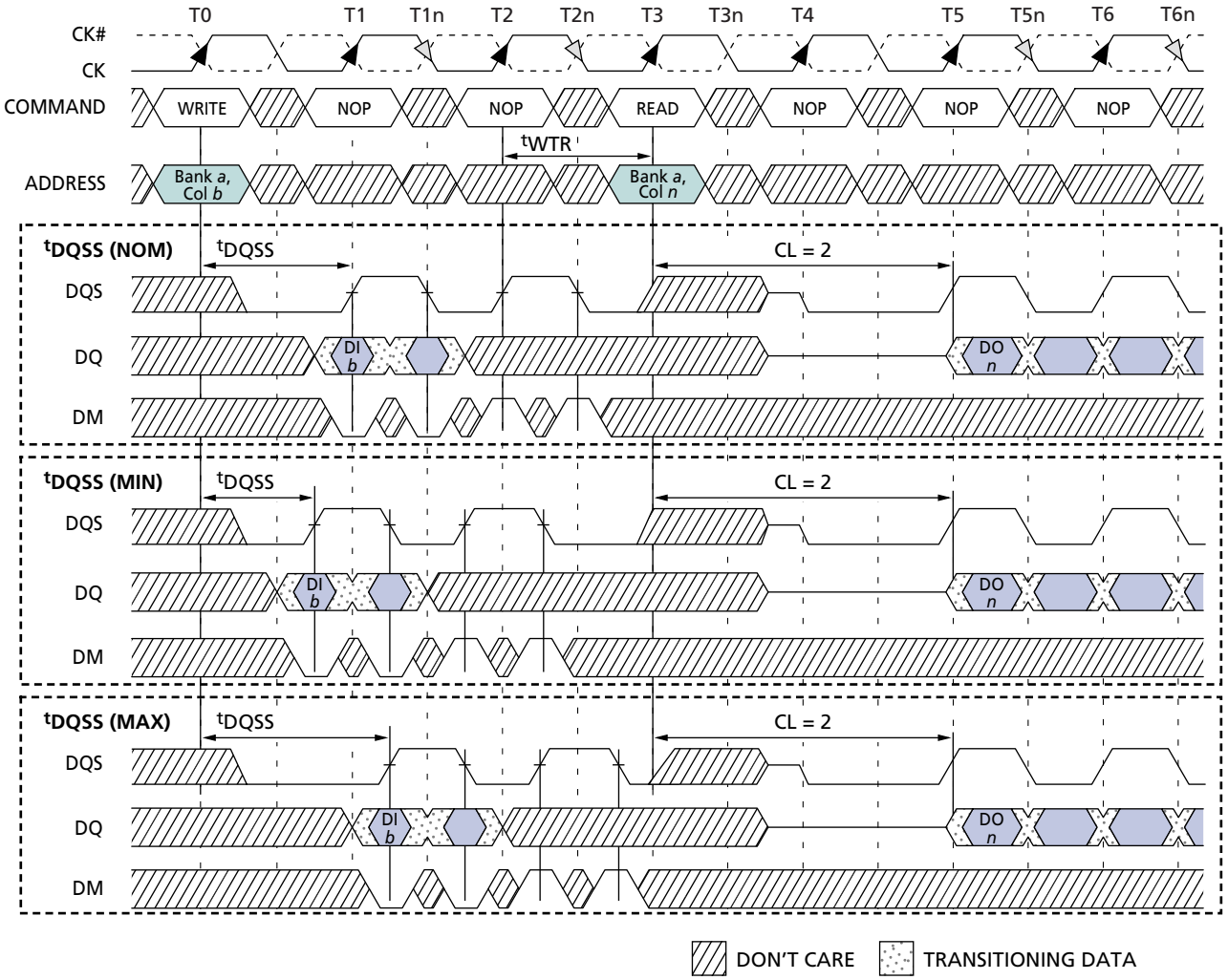
Notes: 1. DI *b*, etc., = data-in for column *b*, etc.
2. *b*', etc., = the next data-in following DI *b*, etc., according to the programmed burst order.
3. Programmed BL = 2, 4, or 8 in cases shown.
4. Each WRITE command may be to any bank.

Figure 25: WRITE-to-READ – Uninterrupting



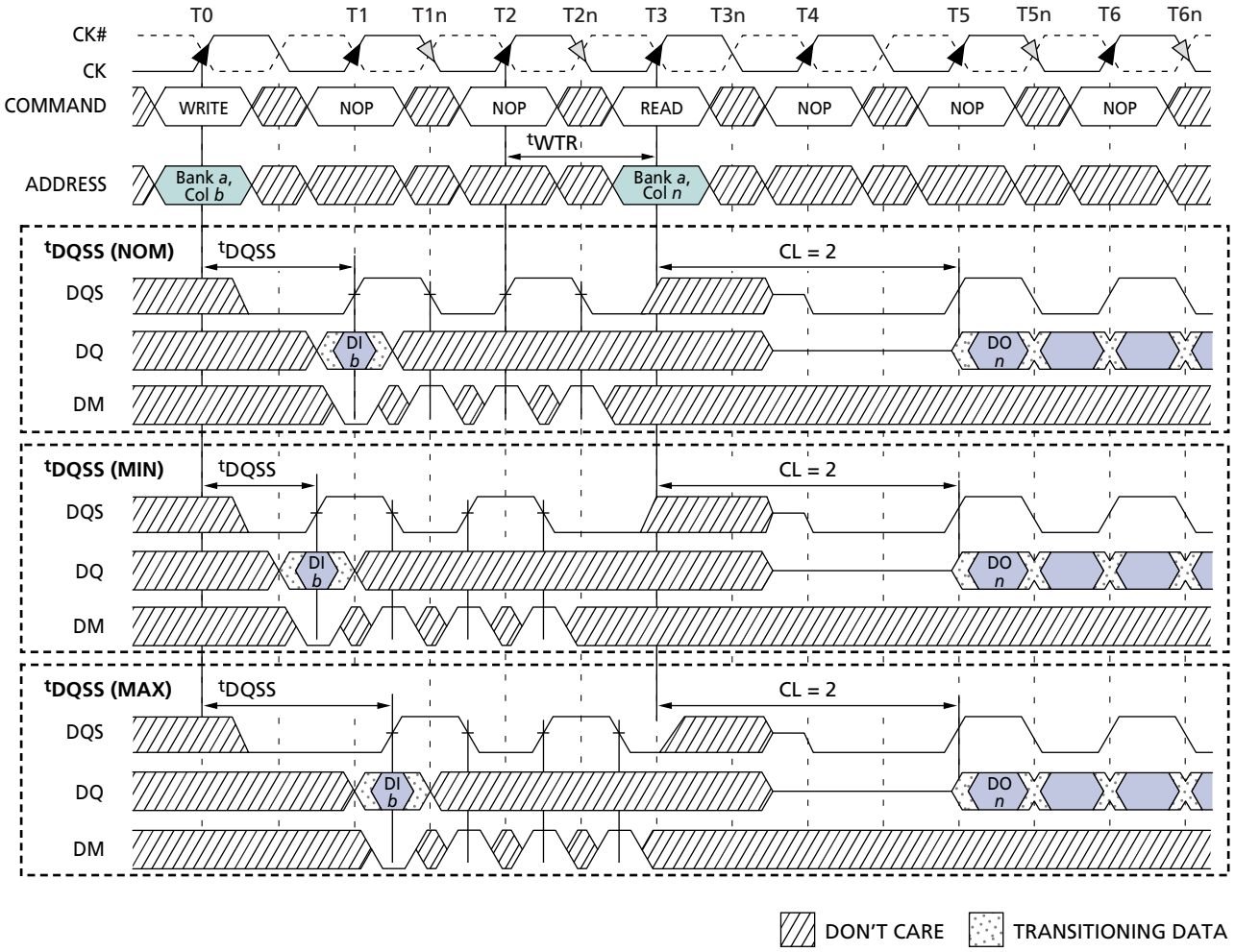
Notes:
1. DI *b* = data-in for column *b; DO n* = data-out for column *n*.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. An uninterrupted burst of 4 is shown.
4. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
5. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be directed to different devices, in which case, ^{t}WTR is not required and the READ command could be applied earlier.
6. A10 is LOW with the WRITE command (auto precharge is disabled).

Figure 26: WRITE-to-READ – Interrupting



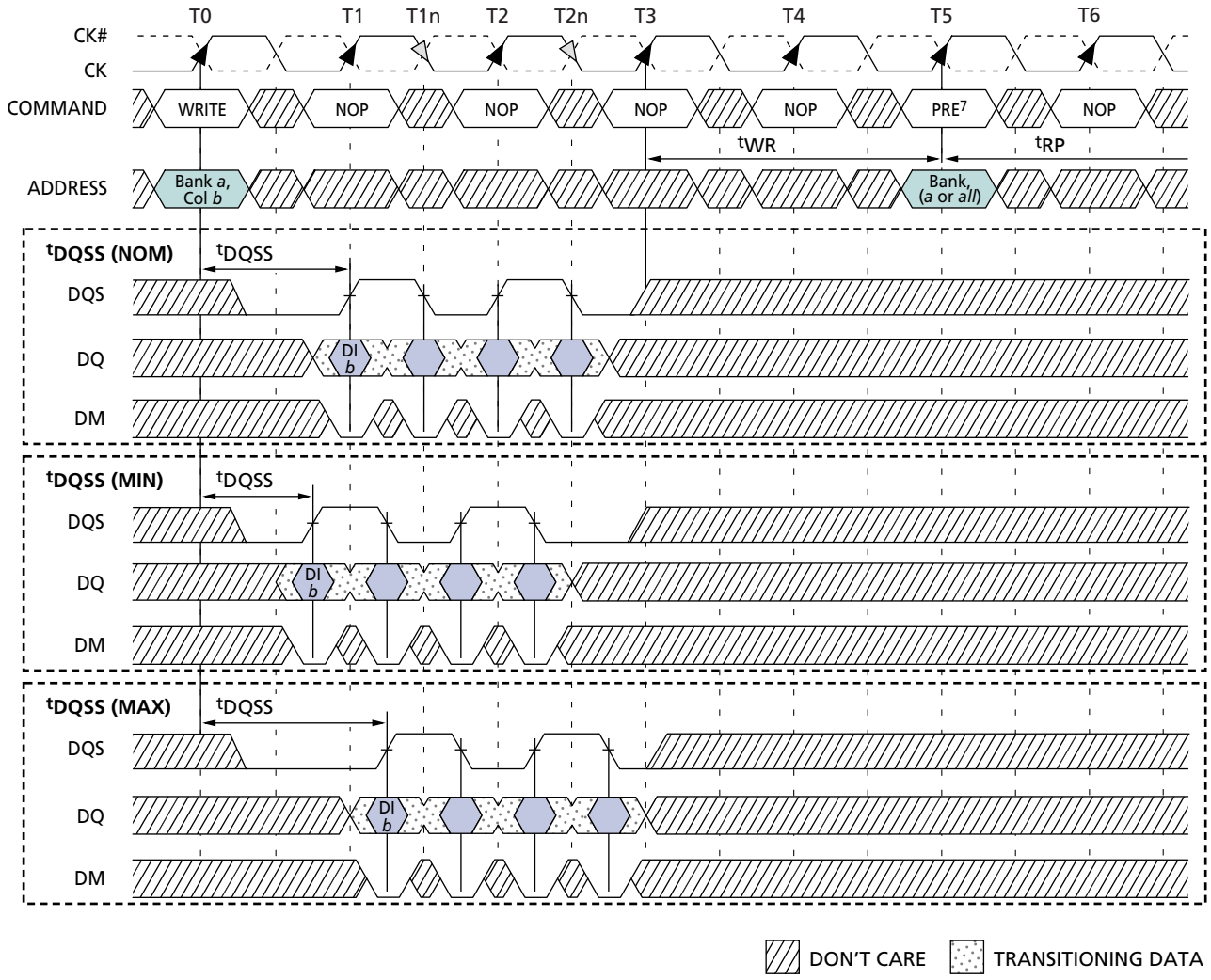
Notes:
1. DI *b* = data-in for column*;, DO n* = data-out for column *n*.
2. An interrupted burst of 4 is shown; two data elements are written.
3. One subsequent element of data-in is applied in the programmed order following DI *b*.
4. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. DQS is required at T2 and T2n (nominal case) to register DM.
7. If the burst of 8 was used, DM and DQS would be required at T3 and T3n because the READ command would not mask these two data elements.

Figure 27: WRITE to READ – Odd Number of Data, Interrupting



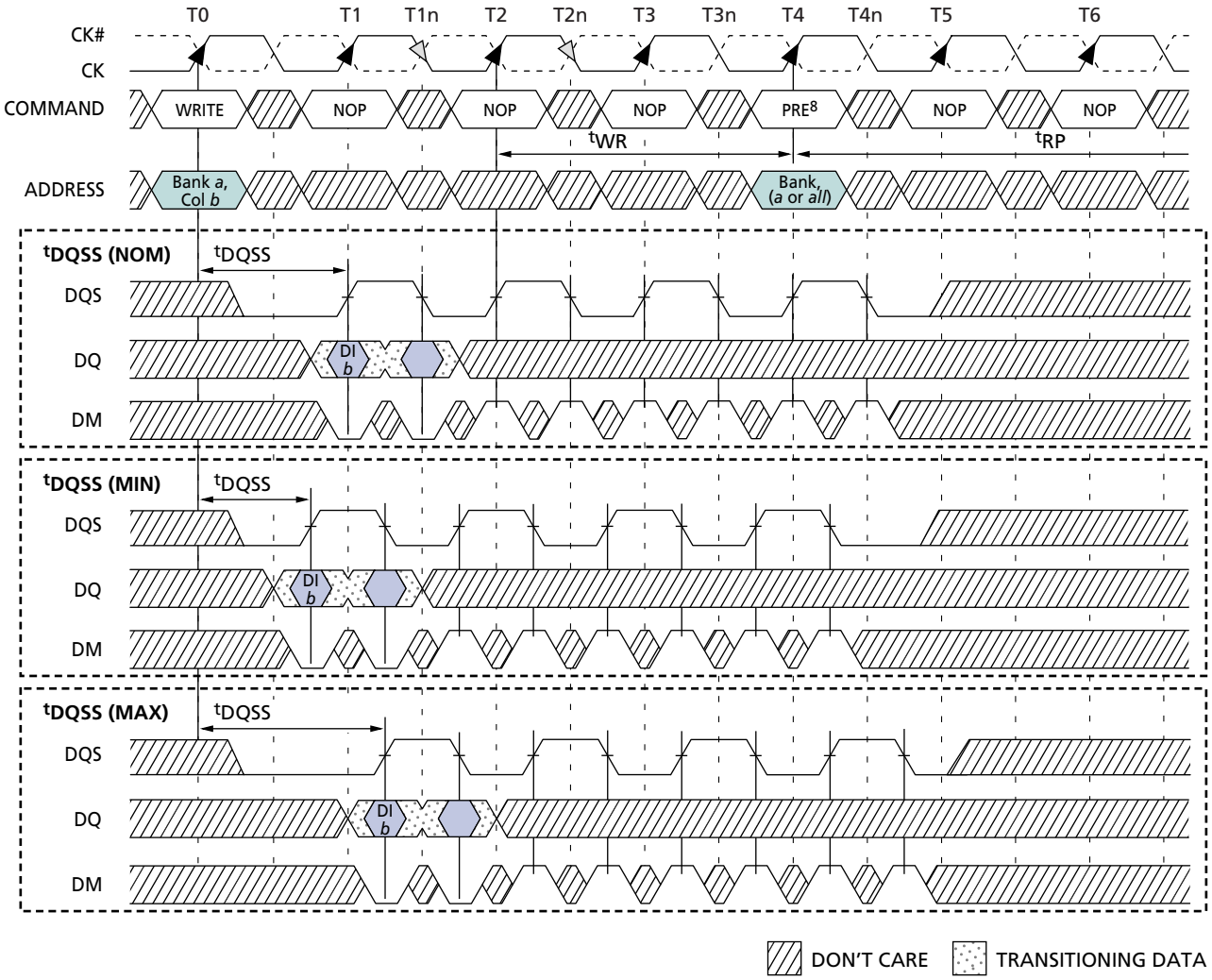
Notes:
1. DI *b* = data-in for column *b; DO n* = data-out for column *n*.
2. An interrupted burst of 4 is shown; one data element is written.
3. ^{t}WTR is referenced from the first positive CK edge after the last desired data-in pair (not the last two data elements).
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T1n, T2, and T2n (nominal case) to register DM.
6. If the burst of 8 was used, DM and DQS would be required at T3–T3n because the READ command would not mask these data elements.

Figure 28: WRITE-to-PRECHARGE – Uninterrupting



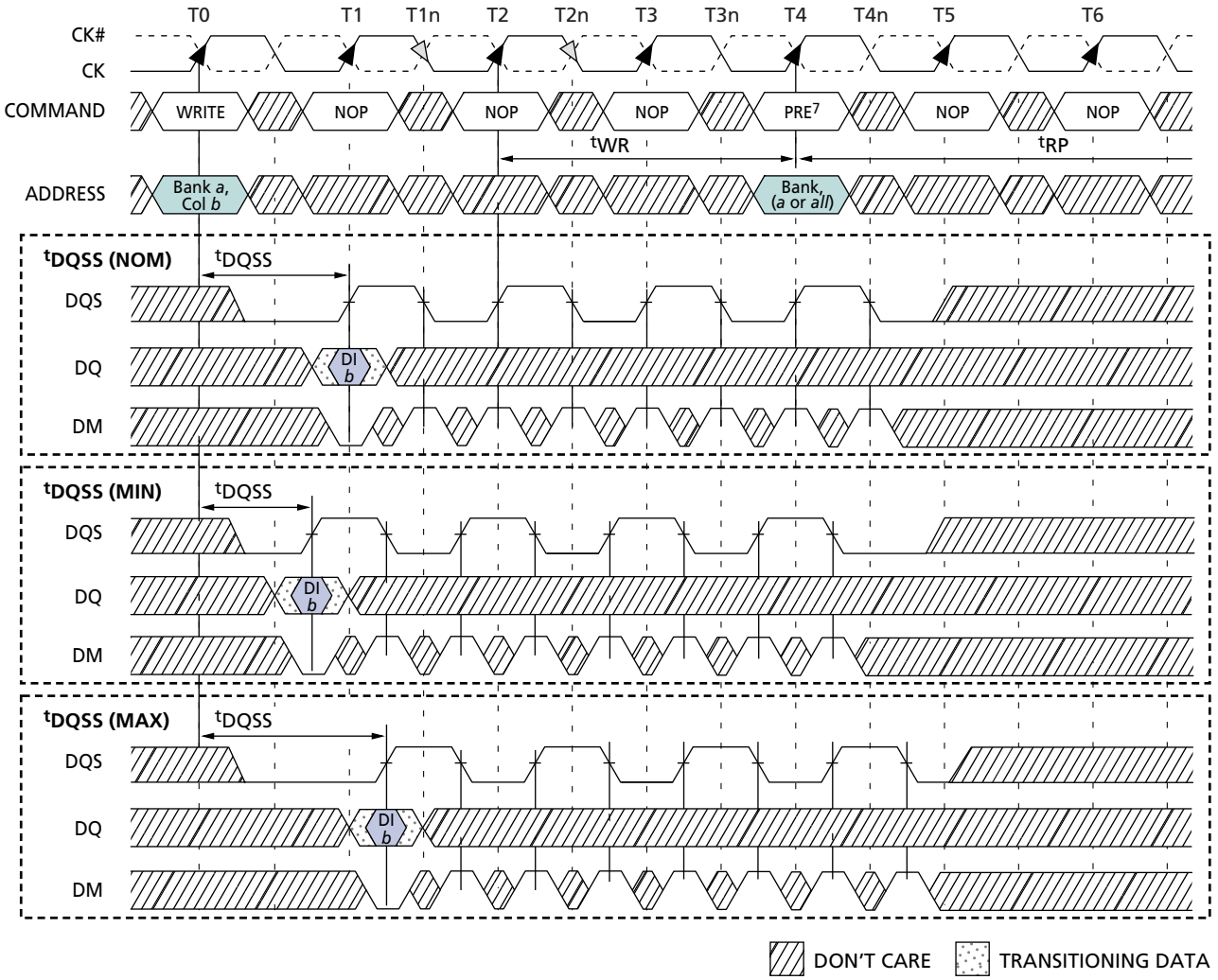
Notes:
1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. An uninterrupted burst of 4 is shown.
4. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
5. The PRECHARGE and WRITE commands are to the same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case, ^{t}WR is not required and the PRECHARGE command could be applied earlier.
6. A10 is LOW with the WRITE command (auto precharge is disabled).
7. PRE = PRECHARGE command.

Figure 29: WRITE-to-PRECHARGE – Interrupting



Notes:
1. DI *b* = data-in for column *b*.
2. Subsequent element of data-in is applied in the programmed order following DI *b*.
3. An interrupted burst of 8 is shown; two data elements are written.
4. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. DQS is required at T4 and T4n (nominal case) to register DM.
7. If the burst of 4 was used, DQS and DM would not be required at T3, T3n, T4, and T4n.
8. PRE = PRECHARGE command.

Figure 30: WRITE-to-PRECHARGE – Odd Number of Data – Interrupting

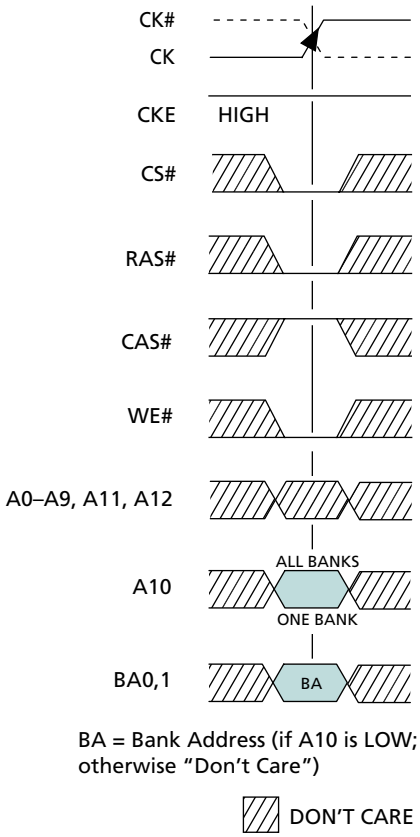


Notes:
1. DI *b* = data-in for column *b*.
2. An interrupted burst of 8 is shown; one data element is written.
3. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T4 and T4n (nominal case) to register DM.
6. If the burst of 4 was used, DQS and DM would not be required at T3, T3n, T4, and T4n.
7. PRE = PRECHARGE command.

PRECHARGE

The PRECHARGE command, as shown in Figure 31, is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 31: PRECHARGE Command



Power-Down (CKE Not Active)

Unlike SDR SDRAMs, DDR SDRAMs require CKE to be active at all times that an access is in progress, from the issuing of a READ or WRITE command until completion of the access. Thus, a clock suspend is not supported. For READs, an access completion is defined when the read postamble is satisfied; for WRITEs, an access completion is defined when the write recovery time (^{t}WR) is satisfied.

Power-down, shown in Figure 32, "Power-Down," on page 48, is entered when CKE is registered LOW and all of the criteria listed in Table 10, on page 48, are met. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK#, and CKE. For maximum power savings, the DLL is frozen during pre-

charge power-down mode. Exiting power-down requires the device to be at the same voltage and frequency as when it entered power-down. However, power-down duration is limited by the refresh requirements of the device (^{t}REFC).

While in power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, while all other input signals are "Don't Care." The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.

Figure 32: Power-Down

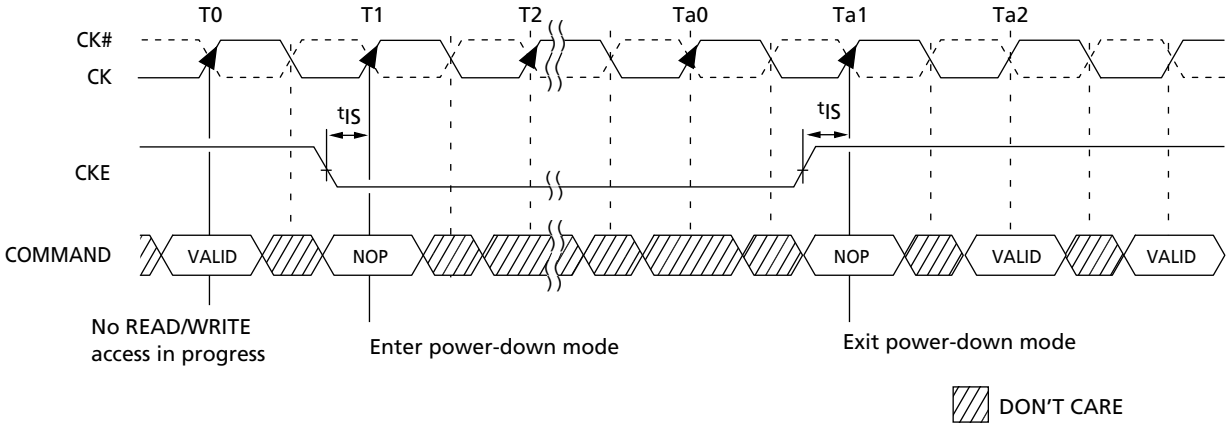


Table 10: Truth Table – CKE

CKE_{n-1}	CKE_n	Current State	$Command_n$	$Action_n$	Notes
L	L	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	
		Self Refresh	DESELECT or NOP	Exit Self Refresh	7
H	L	All Banks Idle	DESELECT or NOP	Precharge Power-Down Entry	
		Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
		All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See Table 11 on page 49		

Notes:
1. CKE_n is the logic state of CKE at clock edge *n*; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. CKE must not drop LOW during a column access. For a READ, this means CKE must stay HIGH until after the read postamble time; for a WRITE, CKE must stay HIGH until the WRITE recovery time (^{t}WR) has been met.
6. Once initialized, including during self refresh mode, V_{REF} must be powered within the specified range.
7. Upon exit of the self refresh mode, the DLL is automatically enabled, but a DLL reset must still occur. A minimum of 200 clock cycles is needed before applying a READ command for the DLL to lock. DESELECT or NOP commands should be issued on any clock edges occurring during the ^{t}XSNR period.

Table 11: Truth Table – Current State Bank *n* – Command-to-Bank *n*

Notes: 1–6; notes appear below and on next page.

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8, 11

Notes:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Table 10 on page 48) and after ^{t}XSNR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and ^{t}RP has been met.
   - Row Active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 11, "Truth Table – Current State Bank n – Command-to-Bank n," on page 49 and according to Table 12, "Truth Table – Current State Bank n – Command-to-Bank m," on page 51.
   - Precharging: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. Once ^{t}RP is met, the bank will be in the idle state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. Once ^{t}RCD is met, the bank will be in the "row active" state.
   - Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.
   - Write w/Auto- Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.
   - Refreshing: Starts with registration of an AUTO REFRESH command and ends when ^{t}RFC is met. Once ^{t}RFC is met, the DDR SDRAM will be in the all banks idle state.

- Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. Once ^{t}MRD is met, the DDR SDRAM will be in the all banks idle state.
- Precharging All: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Table 12: Truth Table – Current State Bank *n* – Command-to-Bank *m*

Notes: 1–6; notes appear below and on next page.

Current State	CS#	RAS#	CAS#	WE#	Command/action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank *m*	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9, 3a
	L	L	H	L	PRECHARGE	
Write (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 3a
	L	L	H	L	PRECHARGE	

Notes:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Truth Table 2) and after ^{t}XSNR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and ^{t}RP has been met.
   - Row Active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated
   - Read with Auto Precharge Enabled: See following text – 3a
   - Write with Auto Precharge Enabled: See following text – 3a

   a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins.

This device supports concurrent auto precharge such that when a READ with auto precharge is enabled or a WRITE with auto precharge is enabled any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank, is summarized below.

Table 13: Minimum Delay Summary

CL_{RU} = CAS Latency (CL) rounded up to the next integer. BL = Bust length.

From Command	To Command	Minimum Delay (with Concurrent Auto Precharge)
WRITE w/AP	READ or READ w/AP	[1 + (BL/2)] * ^{t}CK + ^{t}WTR
	WRITE or WRITE w/AP	(BL/2) * ^{t}CK
	PRECHARGE	1 ^{t}CK
	ACTIVE	1 ^{t}CK
READ w/AP	READ or READ w/AP	(BL/2) * ^{t}CK
	WRITE or WRITE w/AP	[CL_{RU} + (BL/2)] *^{t}CK
	PRECHARGE	1 ^{t}CK
	ACTIVE	1 ^{t}CK

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

VDD Supply Voltage Relative to Vss . . . . . –1V to +3.6V
VDDQ Supply Voltage Relative to VSS . . . . . –1V to +3.6V
VREF and Inputs Voltage Relative to VSS . . . . . –1V to +3.6V
I/O Pins Voltage Relative to VSS . . . . . –0.5V to VDDQ +0.5V
Operating Temperature, T_A ambient, Commercial) . . . . . 0°C to +70°C
Operating Temperature, T_A (ambient, Industrial) . . . . . –40°C to +85°C
Storage Temperature (plastic) . . . . . –55°C to +150°C
Short Circuit Output Current 50mA

Table 14: DC Electrical Characteristics and Operating Conditions (-6, -6T, -75E, -75Z, -75)
0°C ≤ T_A ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V; notes: 1–5, 16; notes appear on pages 69–74.

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply Voltage	VDD	2.3	2.7	V	36, 41
I/O Supply Voltage	VDDQ	2.3	2.7	V	36, 41, 44
I/O Reference Voltage	VREF	0.49 x VDDQ	0.51 x VDDQ	V	6, 44
I/O Termination Voltage (system)	VTT	VREF - 0.04	VREF + 0.04	V	7, 44
Input High (Logic 1) Voltage	VIH(DC)	VREF + 0.15	VDD + 0.3	V	28
Input Low (Logic 0) Voltage	VIL(DC)	–0.3	VREF - 0.15	V	28
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ VDD, VREF PIN 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	II	–2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	–5	5	µA	
OUTPUT LEVELS: Full drive option - x4, x8, x16 High Current (VOUT = VDDQ - 0.373V, minimum VREF, minimum VTT)	IOH	–16.8	–	mA	37, 39
Low Current (VOUT = 0.373V, maximum VREF, maximum VTT)	IOL	16.8	–	mA	
OUTPUT LEVELS: Reduced drive option - x16 only High Current (VOUT = VDDQ - 0.763V, minimum VREF, minimum VTT)	IOHR	–9	–	mA	38, 39
Low Current (VOUT = 0.763V, maximum VREF, maximum VTT)	IOLR	9	–	mA	

Table 15: DC Electrical Characteristics and Operating Conditions (-5B DDR400)

0°C ≤ T_A ≤ +70°C; $V_{DD}Q$ = +2.6V ±0.1V, V_{DD} = +2.6V ±0.1V; notes: 1–5, 16, and 53; notes appear on page 69–74.

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply Voltage	V_{DD}	2.5	2.7	V	36, 41, 52
I/O Supply Voltage	$V_{DD}Q$	2.5	2.7	V	36, 41, 44, 52
I/O Reference Voltage	V_{REF}	0.49 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	6, 44
I/O Termination Voltage (system)	V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	7, 44
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 0.15	V_{DD} + 0.3	V	28
Input Low (Logic 0) Voltage	V_{IL}(DC)	–0.3	V_{REF} - 0.15	V	28
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} PIN 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	I_I	–2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ $V_{DD}Q$)	I_{OZ}	–5	5	µA	
OUTPUT LEVELS: Full drive option – x4, x8, x16 High Current (V_{OUT} = $V_{DD}Q$ - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OH}	–16.8	–	mA	37, 39
Low Current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OL}	16.8	–	mA	
OUTPUT LEVELS: Reduced drive option – x16 only High Current (V_{OUT} = $V_{DD}Q$ - 0.763V, minimum V_{REF}, minimum V_{TT})	I_{OHR}	–9	–	mA	38, 39
Low Current (V_{OUT} = 0.763V, maximum V_{REF}, maximum V_{TT})	I_{OLR}	9	–	mA	

Table 16: AC Input Operating Conditions

0°C ≤ T_A ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V (VDDQ = +2.6V ±0.1V, VDD = +2.6V ±0.1V for DDR400); notes: 1–5, 14, 16; notes appear on pages 69–74.

Parameter/Condition	Symbol	Min	Max	Units	Notes
Input High (Logic 1) Voltage	VIH(AC)	VREF + 0.310	–	V	14, 28, 40
Input Low (Logic 0) Voltage	VIL(AC)	–	VREF - 0.310	V	14, 28, 40
I/O Reference Voltage	VREF(AC)	0.49 x VDDQ	0.51 x VDDQ	V	6

Figure 33: Input Voltage Waveform

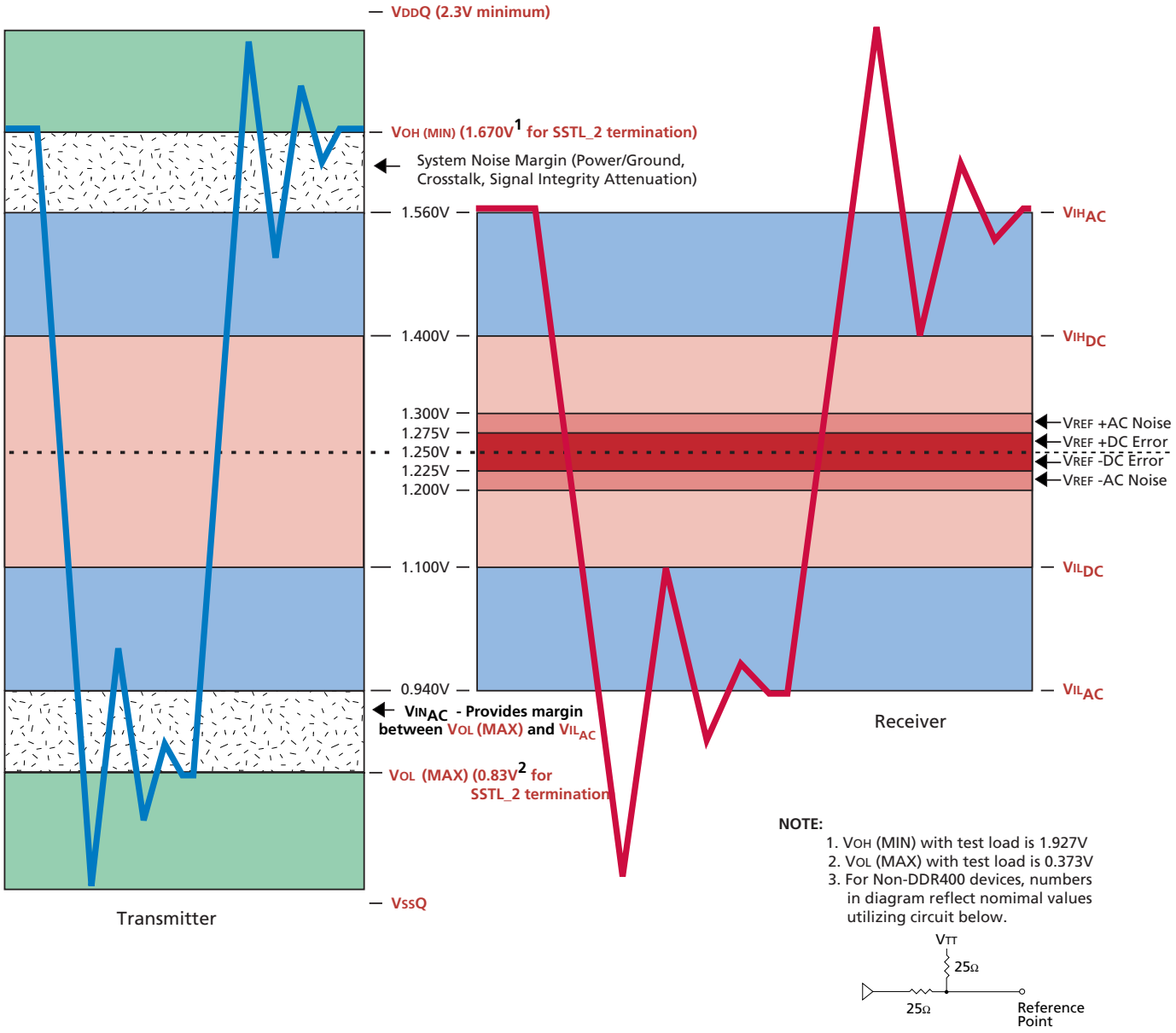
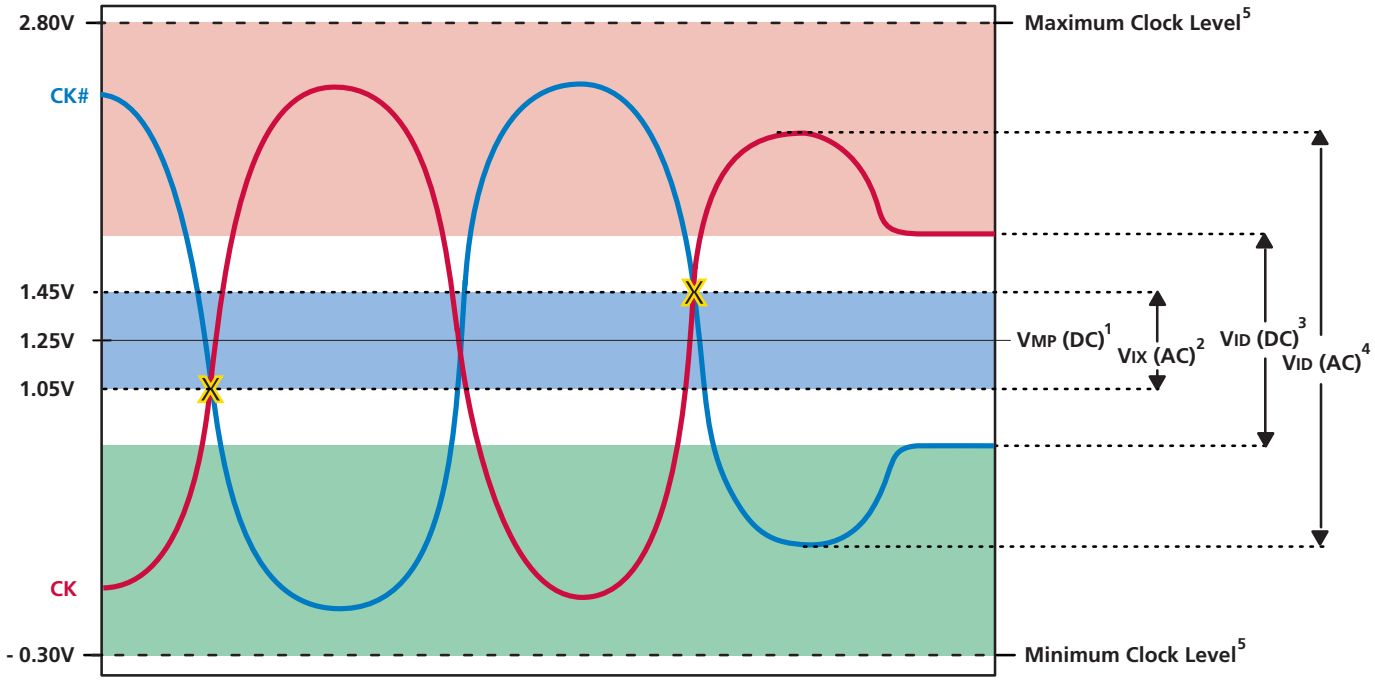


Table 17: Clock Input Operating Conditions

0°C ≤ T_A ≤ +70°C; $V_{DD}Q$ = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V ($V_{DD}Q$ = +2.6V ±0.1V, V_{DD} = +2.6V ±0.1V for DDR400); notes: 1–5, 15, 16, 30; notes appear on pages 69–74.

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock Input Midpoint Voltage; CK and CK#	$V_{MP}(DC)$	1.15	1.35	V	6, 9
Clock Input Voltage Level; CK and CK#	$V_{IN}(DC)$	–0.3	$V_{DD}Q$ + 0.3	V	6
Clock Input Differential Voltage; CK and CK#	$V_{ID}(DC)$	0.36	$V_{DD}Q$ + 0.6	V	6, 8
Clock Input Differential Voltage; CK and CK#	$V_{ID}(AC)$	0.7	$V_{DD}Q$ + 0.6	V	8
Clock Input Crossing Point Voltage; CK and CK#	$V_{IX}(AC)$	0.5 x $V_{DD}Q$ - 0.2	0.5 x $V_{DD}Q$ + 0.2	V	9

Figure 34: SSTL_2 Clock Input



Notes:
1. This provides a minimum of 1.15V to a maximum of 1.35V and is always half of $V_{DD}Q$.
2. CK and CK# must cross in this region.
3. CK and CK# must meet at least V_{ID}(DC) MIN when static and is centered around V_{MP}(DC).
4. CK and CK# must have a minimum 700mv peak-to-peak swing.
5. CK or CK# may not be more positive than $V_{DD}Q$ + 0.3V or more negative than V_{SS} - 0.3V.
6. For AC operation, all DC clock requirements must also be satisfied.
7. Numbers in diagram reflect nominal values for non-DDR400 devices.

Table 18: Capacitance (x4, x8 TSOP)
Note: 13; notes appear on pages 69–74.

Parameter	Symbol	Min	Max	Units	Notes
Delta Input/Output Capacitance: DQ0–DQ3 (x4), DQ0–DQ7 (x8)	DC_{IO}	–	0.50	pF	24
Delta Input Capacitance: Command and Address	DC_{I1}	–	0.50	pF	29
Delta Input Capacitance: CK, CK#	DC_{I2}	–	0.25	pF	29
Input/Output Capacitance: DQs, DQS, DM	C_{IO}	4.0	5.0	pF	
Input Capacitance: Command and Address	C_{I1}	2.0	3.0	pF	
Input Capacitance: CK, CK#	C_{I2}	2.0	3.0	pF	
Input Capacitance: CKE	C_{I3}	2.0	3.0	pF	

Table 19: Capacitance (x16 TSOP)
Note: 13; notes appear on pages 69–74.

Parameter	Symbol	Min	Max	Units	Notes
Delta Input/Output Capacitance: DQ0–DQ7, LDQS, LDM	DC_{IOL}	–	0.50	pF	24
Delta Input/Output Capacitance: DQ8–DQ15, UDQS, UDM	DC_{IOU}	–	0.50	pF	24
Delta Input Capacitance: Command and Address	DC_{I1}	–	0.50	pF	29
Delta Input Capacitance: CK, CK#	DC_{I2}	–	0.25	pF	29
Input/Output Capacitance: DQ, LDQS, UDQS, LDM, UDM	C_{IO}	4.0	5.0	pF	
Input Capacitance: Command and Address	C_{I1}	2.0	3.0	pF	
Input Capacitance: CK, CK#	C_{I2}	2.0	3.0	pF	
Input Capacitance: CKE	C_{I3}	2.0	3.0	pF	

Table 20: IDD Specifications and Conditions (x4, x8; -5B)

0°C ≤ T_A ≤ +70°C; ($V_{DD}Q$ = +2.6V ±0.1V, V_{DD} = +2.6V ±0.1V); notes: 1–5, 10, 12, 14, 46; notes appear on pages 69–74; see also Table 26, "Idd Test Cycle Times," on page 64.

			Max		
Parameter/condition		**Symbol**	**-5B**	**Units**	**Notes**
OPERATING CURRENT: One bank; active precharge; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles		I_{DD0}	135	mA	22, 47
OPERATING CURRENT: One bank; active-read precharge; burst = 4; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); I_{OUT} = 0mA; address and control inputs changing once per clock cycle		I_{DD1}	170	mA	22, 47
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; $^tCK = ^tCK$ (MIN); CKE = (LOW)		I_{DD2P}	4	mA	23, 32, 49
IDLE STANDBY CURRENT: CS# = HIGH; all banks are idle; $^tCK = ^tCK$ (MIN); CKE = HIGH; address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS, and DM		I_{DD2F}	60	mA	50
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; $^tCK = ^tCK$ (MIN); CKE = LOW		I_{DD3P}	40	mA	23, 32, 49
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; one bank active; $^tRC = ^tRAS$ (MAX); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle		I_{DD3N}	70	mA	22
OPERATING CURRENT: Burst = 2; READs; continuous burst; one bank active; address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); I_{OUT} = 0mA		I_{DD4R}	200	mA	22, 47
OPERATING CURRENT: Burst = 2; WRITEs; continuous burst; one bank active; address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	195	mA	22
AUTO REFRESH BURST CURRENT:	$^tREFC = ^tRC$ (MIN)	I_{DD5}	260	mA	49
	^tREFC = 7.8µs	I_{DD5A}	6	mA	27, 49
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	I_{DD6}	4	mA	11
	Low power (L)	I_{DD6A}	2	mA	11
OPERATING CURRENT: Four-bank interleaving READs (Burst = 4) with auto precharge, ^tRC = minimum ^tRC allowed; $^tCK = ^tCK$ (MIN); address and control inputs change only during active READ or WRITE commands		I_{DD7}	470	mA	22, 48

Table 21: IDD Specifications and Conditions (x4, x8; -6/-6T/-75E)

0°C ≤ T_A ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V; notes: 1–5, 10, 12, 14, 46; notes appear on pages 69–74; see also Table 26, "Idd Test Cycle Times," on page 64.

			Max			
Parameter/Condition		**Symbol**	**-6/6T**	**-75E**	**Units**	**Notes**
OPERATING CURRENT: One bank; active precharge; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles		IDD0	125	125	mA	22, 47
OPERATING CURRENT: One bank; active-read precharge; burst = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); IOUT = 0mA; address and control inputs changing once per clock cycle		IDD1	170	160	mA	22, 47
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; ^tCK = ^tCK (MIN); CKE = (LOW)		IDD2P	4	4	mA	23, 32, 49
IDLE STANDBY CURRENT: CS# = HIGH; all banks are idle; ^tCK = ^tCK (MIN); CKE = HIGH; address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS, and DM		IDD2F	50	45	mA	50
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		IDD3P	30	25	mA	23, 32, 49
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; one bank active; ^tRC = ^tRAS (MAX); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle		IDD3N	60	50	mA	22
OPERATING CURRENT: Burst = 2; READs; continuous burst; one bank active; address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); IOUT = 0mA		IDD4R	175	150	mA	22, 47
OPERATING CURRENT: Burst = 2; WRITEs; continuous burst; one bank active; address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	175	150	mA	22
AUTO REFRESH BURST CURRENT:	^tREFC = ^tRC (MIN)	IDD5	255	235	mA	49
	^tREFC = 7.8µs	IDD5A	6	6	mA	27, 49
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	IDD6	4	4	mA	11
	Low power (L)	IDD6A	2	2	mA	11
OPERATING CURRENT: Four-bank interleaving READs (Burst = 4) with auto precharge, ^tRC = minimum ^tRC allowed; ^tCK = ^tCK (MIN); address and control inputs change only during active READ or WRITE commands		IDD7	410	350	mA	22, 48

Table 22: IDD Specifications and Conditions (x4, x8; -75Z/-75)

0°C ≤ T_A ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V; Notes: 1–5, 10, 12, 14, 46; notes appear on pages 69–74; see also Table 26, "Idd Test Cycle Times," on page 64.

			Max			
Parameter/Condition		**Symbol**	**-75Z**	**-75**	**Units**	**Notes**
OPERATING CURRENT: One bank; active precharge; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles		IDD0	120	120	mA	22, 47
OPERATING CURRENT: One bank; active-read precharge; burst = 4; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); IOUT = 0mA; address and control inputs changing once per clock cycle		IDD1	145	145	mA	22, 47
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; $^tCK = ^tCK$ (MIN); CKE = (LOW)		IDD2P	4	4	mA	23, 32, 49
IDLE STANDBY CURRENT: CS# = HIGH; all banks are idle; $^tCK = ^tCK$ (MIN); CKE = HIGH; address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS, and DM		IDD2F	45	45	mA	50
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; $^tCK = ^tCK$ (MIN); CKE = LOW		IDD3P	25	30	mA	23, 32, 49
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; one bank active; $^tRC = ^tRAS$ (MAX); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle		IDD3N	50	50	mA	22
OPERATING CURRENT: Burst = 2; READs; continuous burst; one bank active; address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); IOUT = 0mA		IDD4R	150	150	mA	22, 47
OPERATING CURRENT: Burst = 2; WRITEs; continuous burst; one bank active; address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	150	150	mA	22
AUTO REFRESH BURST CURRENT:	$^tREFC = ^tRC$ (MIN)	IDD5	235	245	mA	49
	^tREFC = 7.8µs	IDD5A	6	6	mA	27, 49
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	IDD6	4	4	mA	11
	Low power (L)	IDD6A	2	2	mA	11
OPERATING CURRENT: Four-bank interleaving READs (Burst = 4) with auto precharge, ^tRC = minimum ^tRC allowed; $^tCK = ^tCK$ (MIN); address and control inputs change only during active READ or WRITE commands		IDD7	350	365	mA	22, 48

Table 23: IDD Specifications and Conditions (x16; -5B)

0°C ≤ T_A ≤ +70°C; ($V_{DD}Q$ = +2.6V ±0.1V, V_{DD} = +2.6V ±0.1V); notes: 1–5, 10, 12, 14, 46; notes appear on pages 69–74; see also Table 26, "Idd Test Cycle Times," on page 64.

			Max		
Parameter/Condition		**Symbol**	**-5B**	**Units**	**Notes**
OPERATING CURRENT: One bank; active precharge; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles		I_{DD0}	135	mA	22, 47
OPERATING CURRENT: One bank; active-read precharge; burst = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); I_{OUT} = 0mA; address and control inputs changing once per clock cycle		I_{DD1}	185	mA	22, 47
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; ^tCK = ^tCK (MIN); CKE = (LOW)		I_{DD2P}	4	mA	23, 32, 49
IDLE STANDBY CURRENT: CS# = HIGH; all banks are idle; ^tCK = ^tCK (MIN); CKE = HIGH; address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS, and DM		I_{DD2F}	60	mA	50
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		I_{DD3P}	40	mA	23, 32, 49
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; one bank active; ^tRC = ^tRAS (MAX); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle		I_{DD3N}	70	mA	22
OPERATING CURRENT: Burst = 2; READs; continuous burst; one bank active; address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); I_{OUT} = 0mA		I_{DD4R}	260	mA	22, 47
OPERATING CURRENT: Burst = 2; WRITEs; continuous burst; one bank active; address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	215	mA	22
AUTO REFRESH BURST CURRENT:	^tREFC = ^tRC (MIN)	I_{DD5}	260	mA	49
	^tREFC = 7.8µs	I_{DD5A}	6	mA	27, 49
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	I_{DD6}	4	mA	11
	Low power (L)	I_{DD6A}	2	mA	11
OPERATING CURRENT: Four-bank interleaving READs (Burst = 4) with auto precharge, ^tRC = minimum ^tRC allowed; ^tCK = ^tCK (MIN); address and control inputs change only during active READ or WRITE commands		I_{DD7}	510	mA	22, 48

Table 24: IDD Specifications and Conditions (x16; -6/-6T/-75E)

0°C ≤ T_A ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V; notes: 1–5, 10, 12, 14, 46; notes appear on pages 69–74; see also Table 26, "Idd Test Cycle Times," on page 64.

			Max			
Parameter/Condition		**Symbol**	**-6/6T**	**-75E**	**Units**	**Notes**
OPERATING CURRENT: One bank; active precharge; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles		IDD0	125	125	mA	22, 47
OPERATING CURRENT: One bank; active-read precharge; burst = 4; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); IOUT = 0mA; address and control inputs changing once per clock cycle		IDD1	180	170	mA	22, 47
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; $^tCK = ^tCK$ (MIN); CKE = (LOW)		IDD2P	4	4	mA	23, 32, 49
IDLE STANDBY CURRENT: CS# = HIGH; all banks are idle; $^tCK = ^tCK$ (MIN); CKE = HIGH; address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS, and DM		IDD2F	50	45	mA	50
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; $^tCK = ^tCK$ (MIN); CKE = LOW		IDD3P	30	25	mA	23, 32, 49
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; one bank active; $^tRC = ^tRAS$ (MAX); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle		IDD3N	60	50	mA	22
OPERATING CURRENT: Burst = 2; READs; continuous burst; one bank active; address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); IOUT = 0mA		IDD4R	220	185	mA	22, 47
OPERATING CURRENT: Burst = 2; WRITEs; continuous burst; one bank active; address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	195	160	mA	22
AUTO REFRESH BURST CURRENT:	$^tREFC = ^tRC$ (MIN)	IDD5	255	235	mA	49
	^tREFC = 7.8µs	IDD5A	6	6	mA	27, 49
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	IDD6	4	4	mA	11
	Low power (L)	IDD6A	2	2	mA	11
OPERATING CURRENT: Four-bank interleaving READs (Burst = 4) with auto precharge, ^tRC = minimum ^tRC allowed; $^tCK = ^tCK$ (MIN); address and control inputs change only during active READ or WRITE commands		IDD7	440	380	mA	22, 48

Table 25: IDD Specifications and Conditions (x16; -75Z/-75)

0°C ≤ T_A ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V

Notes: 1–5, 10, 12, 14, 46; notes appear on pages 69–74; see also Table 26, "Idd Test Cycle Times," on page 64.

			Max			
Parameter/Condition		**Symbol**	**-75Z**	**-75**	**Units**	**Notes**
OPERATING CURRENT: One bank; active precharge; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles		IDD0	120	120	mA	22, 47
OPERATING CURRENT: One bank; active-read precharge; burst = 4; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); IOUT = 0mA; address and control inputs changing once per clock cycle		IDD1	155	155	mA	22, 47
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; $^tCK = ^tCK$ (MIN); CKE = (LOW)		IDD2P	4	4	mA	23, 32, 49
IDLE STANDBY CURRENT: CS# = HIGH; all banks are idle; $^tCK = ^tCK$ (MIN); CKE = HIGH; address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS, and DM		IDD2F	45	45	mA	50
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; $^tCK = ^tCK$ (MIN); CKE = LOW		IDD3P	25	30	mA	23, 32, 49
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; one bank active; $^tRC = ^tRAS$ (MAX); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle		IDD3N	50	50	mA	22
OPERATING CURRENT: Burst = 2; READs; continuous burst; one bank active; address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); IOUT = 0mA		IDD4R	185	185	mA	22, 47
OPERATING CURRENT: Burst = 2; WRITEs; continuous burst; one bank active; address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	160	160	mA	22
AUTO REFRESH BURST CURRENT:	$^tREFC = ^tRC$(MIN)	IDD5	235	245	mA	49
	^tREFC = 7.8µs	IDD5A	6	6	mA	27, 49
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	IDD6	4	4	mA	11
	Low power (L)	IDD6A	2	2	mA	11
OPERATING CURRENT: Four-bank interleaving READs (Burst = 4) with auto precharge, ^tRC = minimum ^tRC allowed; $^tCK = ^tCK$ (MIN); address and control inputs change only during active READ or WRITE commands		IDD7	380	400	mA	22, 48

Table 26: IDD Test Cycle Times
Values reflect number of clock cycles for each test.

IDD Test	Speed Grade	Clock Cycle Time	tRRD	tRCD	tRAS	tRP	tRC	tRFC	tREFI	CL
IDD0	-75/75Z	7.5ns	n/a	n/a	6	3	9	n/a	n/a	n/a
	-75E	7.5ns	n/a	n/a	6	2	8	n/a	n/a	n/a
	-6/-6T	6ns	n/a	n/a	7	3	10	n/a	n/a	n/a
	-5B	5ns	n/a	n/a	8	3	11	n/a	n/a	n/a
IDD1	-75	7.5ns	n/a	n/a	6	3	9	n/a	n/a	2.5
	-75Z	7.5ns	n/a	n/a	6	3	9	n/a	n/a	2
	-75E	7.5ns	n/a	n/a	6	2	8	n/a	n/a	2
	-6/-6T	6ns	n/a	n/a	7	3	10	n/a	n/a	2.5
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	3
IDD4R	-75	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2.5
	-75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2.5
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	3
IDD4W	-75	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
IDD5	-75/75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	10	10	n/a
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	9	9	n/a
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	12	12	n/a
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	14	14	n/a
IDD5A	-75/75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	10	1,030	n/a
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	9	1,030	n/a
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	12	1,288	n/a
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	14	1,546	n/a
IDD7	-75	7.5ns	2/4	3	n/a	3	10	n/a	n/a	2.5
	-75Z	7.5ns	2/4	3	n/a	3	10	n/a	n/a	2
	-75E	7.5ns	2	3	n/a	2	8	n/a	n/a	2
	-6/-6T	6ns	2/4	3	n/a	3	10	n/a	n/a	2.5
	-5B	5ns	2/4	3	n/a	3	11	n/a	n/a	3

Table 27: Electrical Characteristics and Recommended AC Operating Conditions (-5B)

Notes: 1–5, 14–17, 33; notes on pages 69–74; 0°C ≤ T_A ≤ +70°C; ($V_{DD}Q$ = +2.6V ±0.1V, V_{DD} = +2.6V ±0.1V)

AC Characteristics			-5B			
Parameter		**Symbol**	**Min**	**Max**	**Units**	**Notes**
Access window of DQs from CK/CK#		^tAC	–0.70	+0.70	ns	
CK high-level width		^tCH	0.45	0.55	^tCK	30
CK low-level width		^tCL	0.45	0.55	^tCK	30
Clock cycle time	CL = 3	^tCK (3)	5	7.5	ns	51
	CL = 2.5	^tCK (2.5)	6	13	ns	45, 51
	CL = 2	^tCK (2)	7.5	13	ns	45, 51
DQ and DM input hold time relative to DQS		^tDH	0.40	–	ns	26, 31
DQ and DM input setup time relative to DQS		^tDS	0.40	–	ns	26, 31
DQ and DM input pulse width (for each input)		^tDIPW	1.75	–	ns	31
Access window of DQS from CK/CK#		^tDQSCK	–0.6	+0.6	ns	
DQS input high pulse width		^tDQSH	0.35	–	^tCK	
DQS input low pulse width		^tDQSL	0.35	–	^tCK	
DQS–DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ	–	0.4	ns	25, 26
WRITE command to first DQS latching transition		^tDQSS	0.72	1.28	^tCK	
DQS falling edge to CK rising – setup time		^tDSS	0.2	–	^tCK	
DQS falling edge from CK rising – hold time		^tDSH	0.2	–	^tCK	
Half clock period		^tHP	^tCH,^tCL	–	ns	34
Data-out high-impedance window from CK/CK#		^tHZ	–	+0.7	ns	18, 42
Data-out low-impedance window from CK/CK#		^tLZ	–0.7	–	ns	18, 42
Address and control input hold time (fast slew rate)		^tIH_F	0.60	–	ns	
Address and control input setup time (fast slew rate)		^tIS_F	0.60	–	ns	
Address and control input hold time (slow slew rate)		^tIH_S	0.60	–	ns	14
Address and control input setup time (slow slew rate)		^tIS_S	0.60	–	ns	14
Address and Control input pulse width (for each input)		^tIPW	2.2	–	ns	
LOAD MODE REGISTER command cycle time		^tMRD	10	–	ns	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP -^tQHS	–	ns	25, 26
Data hold skew factor		^tQHS	–	0.5	ns	
ACTIVE to PRECHARGE command		^tRAS	40	70,000	ns	35
ACTIVE to READ with auto precharge command		^tRAP	15	–	ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		^tRC	55	–	ns	
AUTO REFRESH command period		^tRFC	70	–	ns	49
ACTIVE to READ or WRITE delay		^tRCD	15	–	ns	
PRECHARGE command period		^tRP	15	–	ns	
DQS read preamble		^tRPRE	0.9	1.1	^tCK	43
DQS read postamble		^tRPST	0.4	0.6	^tCK	43
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	10	–	ns	
DQS write preamble		^tWPRE	0.25	–	^tCK	
DQS write preamble setup time		^tWPRES	0	–	ns	20, 21
DQS write postamble		^tWPST	0.4	0.6	^tCK	19
Write recovery time		^tWR	15	–	ns	
Internal WRITE to READ command delay		^tWTR	2	–	^tCK	
Data valid output window (DVW)		N/A	^tQH - ^tDQSQ		ns	25
REFRESH to REFRESH command interval		^tREFC	–	70.3	µs	23
Average periodic refresh interval		^tREFI	–	7.8	µs	23
Terminating voltage delay to V_{DD}		^tVTD	0	–	ns	
Exit SELF REFRESH to non-READ command		^tXSNR	70	–	ns	
Exit SELF REFRESH to READ command		^tXSRD	200	–	^tCK	

Table 28: Electrical Characteristics and Recommended AC Operating Conditions (-6/-6T/-75E)

Notes: 1–5, 14–17, 33; notes appear on pages 69–74; 0°C ≤ T_A ≤ +70°C; $V_{DD}Q$ = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V

AC Characteristics			-6 (FBGA)		-6T (TSOP)		-75E			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Units	Notes
Access window of DQs from CK/CK#		^tAC	–0.70	+0.70	–0.70	+0.70	–0.75	+0.75	ns	
CK high-level width		^tCH	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	30
CK low-level width		^tCL	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	30
Clock cycle time	CL = 2.5	^tCK (2.5)	6	13	6	13	7.5	13	ns	45, 51
	CL = 2	^tCK (2)	7.5	13	7.5	13	7.5	13	ns	45, 51
DQ and DM input hold time relative to DQS		^tDH	0.45	–	0.45	–	0.5	–	ns	26, 31
DQ and DM input setup time relative to DQS		^tDS	0.45	–	0.45	–	0.5	–	ns	26, 31
DQ and DM input pulse width (for each input)		^tDIPW	1.75	–	1.75	–	1.75	–	ns	31
Access window of DQS from CK/CK#		^tDQSCK	–0.6	+0.6	–0.6	+0.6	–0.75	+0.75	ns	
DQS input high pulse width		^tDQSH	0.35	–	0.35	–	0.35	–	^tCK	
DQS input low pulse width		^tDQSL	0.35	–	0.35	–	0.35	–	^tCK	
DQS–DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ	–	0.4	–	0.45	–	0.5	ns	25, 26
WRITE command to first DQS latching transition		^tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	^tCK	
DQS falling edge to CK rising – setup time		^tDSS	0.2	–	0.2	–	0.2	–	^tCK	
DQS falling edge from CK rising – hold time		^tDSH	0.2	–	0.2	–	0.2	–	^tCK	
Half clock period		^tHP	^tCH, ^tCL	–	^tCH, ^tCL	–	^tCH, ^tCL	–	ns	34
Data-out high-impedance window from CK/CK#		^tHZ	–	+0.7	–	+0.7	–	+0.75	ns	18, 42
Data-out low-impedance window from CK/CK#		^tLZ	–0.7	–	–0.7	–	–0.75	–	ns	18, 42
Address and control input hold time (fast slew rate)		^tIH_F	0.75	–	0.75	–	0.90	–	ns	
Address and control input setup time (fast slew rate)		^tIS_F	0.75	–	0.75	–	0.90	–	ns	
Address and control input hold time (slow slew rate)		^tIH_S	0.8	–	0.8	–	1	–	ns	14
Address and control input setup time (slow slew rate)		^tIS_S	0.8	–	0.8	–	1	–	ns	14
Address and Control input pulse width (for each input)		^tIPW	2.2	–	2.2	–	2.2	–	ns	
LOAD MODE REGISTER command cycle time		^tMRD	12	–	12	–	15	–	ns	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP -^tQHS	–	^tHP -^tQHS	–	^tHP -^tQHS	–	ns	25, 26
Data hold skew factor		^tQHS	–	0.5	–	0.55	–	0.75	ns	
ACTIVE to PRECHARGE command		^tRAS	42	70,000	42	70,000	40	120,000	ns	35, 53
ACTIVE to READ with auto precharge command		^tRAP	15	–	15	–	15	–	ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		^tRC	60	–	60	–	60	–	ns	
AUTO REFRESH command period		^tRFC	72	–	72	–	75	–	ns	49
ACTIVE to READ or WRITE delay		^tRCD	15	–	15	–	15	–	ns	
PRECHARGE command period		^tRP	15	–	15	–	15	–	ns	
DQS read preamble		^tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	^tCK	43
DQS read postamble		^tRPST	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	43
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	12	–	12	–	15	–	ns	
DQS write preamble		^tWPRE	0.25	–	0.25	–	0.25	–	^tCK	
DQS write preamble setup time		^tWPRES	0	–	0	–	0	–	ns	20, 21
DQS write postamble		^tWPST	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	19
Write recovery time		^tWR	15	–	15	–	15	–	ns	
Internal WRITE to READ command delay		^tWTR	1	–	1	–	1	–	^tCK	
Data valid output window (DVW)		n/a	^tQH - ^tDQSQ		^tQH - ^tDQSQ		^tQH - ^tDQSQ		ns	25
REFRESH to REFRESH command interval		^tREFC	–	70.3	–	70.3	–	70.3	µs	23
Average periodic refresh interval		^tREFI	–	7.8	–	7.8	–	7.8	µs	23
Terminating voltage delay to V_{DD}		^tVTD	0	–	0	–	0	–	ns	
Exit SELF REFRESH to non-READ command		^tXSNR	75	–	75	–	75	–	ns	
Exit SELF REFRESH to READ command		^tXSRD	200	–	200	–	200	–	^tCK	

Table 29: Electrical Characteristics and Recommended AC Operating Conditions (-75Z/-75)

Notes: 1–5, 14–17, 33; notes appear on pages 69–74; 0°C ≤ T_A ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V

AC Characteristics			-75Z		-75			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Access window of DQs from CK/CK#		^{t}AC	–0.75	+0.75	–0.75	+0.75	ns	
CK high-level width		^{t}CH	0.45	0.55	0.45	0.55	^{t}CK	30
CK low-level width		^{t}CL	0.45	0.55	0.45	0.55	^{t}CK	30
Clock cycle time	CL = 2.5	^{t}CK (2.5)	7.5	13	7.5	13	ns	45, 51
	CL = 2	^{t}CK (2)	7.5	13	10	13	ns	45, 51
DQ and DM input hold time relative to DQS		^{t}DH	0.50	–	0.50	–	ns	26, 31
DQ and DM input setup time relative to DQS		^{t}DS	0.50	–	0.50	–	ns	26, 31
DQ and DM input pulse width (for each input)		^{t}DIPW	1.75	–	1.75	–	ns	31
Access window of DQS from CK/CK#		^{t}DQSCK	–0.75	+0.75	–0.75	+0.75	ns	
DQS input high pulse width		^{t}DQSH	0.35	–	0.35	–	^{t}CK	
DQS input low pulse width		^{t}DQSL	0.35	–	0.35	–	^{t}CK	
DQS–DQ skew, DQS to last DQ valid, per group, per access		^{t}DQSQ	–	0.5	–	0.5	ns	25, 26
WRITE command to first DQS latching transition		^{t}DQSS	0.75	1.25	0.75	1.25	^{t}CK	
DQS falling edge to CK rising – setup time		^{t}DSS	0.20	–	0.20	–	^{t}CK	
DQS falling edge from CK rising – hold time		^{t}DSH	0.20	–	0.20	–	^{t}CK	
Half clock period		^{t}HP	^{t}CH,^{t}CL	–	^{t}CH,^{t}CL	–	ns	34
Data-out high-impedance window from CK/CK#		^{t}HZ	–	+0.75	–	+0.75	ns	18, 42
Data-out low-impedance window from CK/CK#		^{t}LZ	-0.75	–	-0.75	–	ns	18, 42
Address and control input hold time (fast slew rate)		^{t}IH$_F$	0.90	–	0.90	–	ns	
Address and control input setup time (fast slew rate)		^{t}IS$_F$	0.90	–	0.90	–	ns	
Address and control input hold time (slow slew rate)		^{t}IH$_S$	1	–	1	–	ns	14
Address and control input setup time (slow slew rate)		^{t}IS$_S$	1	–	1	–	ns	14
Address and Control input pulse width (for each input)		^{t}IPW	2.2	–	2.2	–	ns	
LOAD MODE REGISTER command cycle time		^{t}MRD	15	–	15	–	ns	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		^{t}QH	^{t}HP -^{t}QHS	–	^{t}HP -^{t}QHS	–	ns	25, 26
Data hold skew factor		^{t}QHS	–	0.75	–	0.75	ns	
ACTIVE to PRECHARGE command		^{t}RAS	40	120,000	40	120,000	ns	35
ACTIVE to READ with auto precharge command		^{t}RAP	20	–	20	–	ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		^{t}RC	65	–	65	–	ns	
AUTO REFRESH command period		^{t}RFC	75	–	75	–	ns	49
ACTIVE to READ or WRITE delay		^{t}RCD	20	–	20	–	ns	
PRECHARGE command period		^{t}RP	20	–	20	–	ns	
DQS read preamble		^{t}RPRE	0.9	1.1	0.9	1.1	^{t}CK	43
DQS read postamble		^{t}RPST	0.4	0.6	0.4	0.6	^{t}CK	43
ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	15	–	15	–	ns	
DQS write preamble		^{t}WPRE	0.25	–	0.25	–	^{t}CK	
DQS write preamble setup time		^{t}WPRES	0	–	0	–	ns	20, 21
DQS write postamble		^{t}WPST	0.4	0.6	0.4	0.6	^{t}CK	19
Write recovery time		^{t}WR	15	–	15	–	ns	
Internal WRITE to READ command delay		^{t}WTR	1	–	1	–	^{t}CK	
Data valid output window (DVW)		n/a	^{t}QH - ^{t}DQSQ		^{t}QH - ^{t}DQSQ		ns	25
REFRESH to REFRESH command interval		^{t}REFC	–	70.3	–	70.3	µs	23
Average periodic refresh interval		^{t}REFI	–	7.8	–	7.8	µs	23
Terminating voltage delay to VDD		^{t}VTD	0	–	0	–	ns	
Exit SELF REFRESH to non-READ command		^{t}XSNR	75	–	75	–	ns	
Exit SELF REFRESH to READ command		^{t}XSRD	200	–	200	–	^{t}CK	

Table 30: Input Slew Rate Derating Values for Addresses and Commands

0°C ≤ T_A ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V; notes: 14; notes appear on pages 69–74.

Speed	Slew Rate	^tIS	^tIH	Units
-75/-75Z/-75E	0.50 V/ns ≤ Slew Rate < 1.0 V/ns	1.00	1	ns
-75/-75Z/-75E	0.40 V/ns ≤ Slew Rate < 0.5 V/ns	1.05	1	ns
-75/-75Z/-75E	0.30 V/ns ≤ Slew Rate < 0.4 V/ns	1.15	1	ns

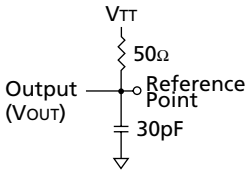
Table 31: Input Slew Rate Derating Values for DQ, DQS, and DM

0°C ≤ T_A ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V; notes: 31; notes appear on pages 69-74.

Speed	Slew Rate	^tDS	^tDH	Units
-75/-75Z/-75E	0.50 V/ns ≤ Slew Rate < 1.0 V/ns	0.50	0.50	ns
-75/-75Z/-75E	0.40 V/ns ≤ Slew Rate < 0.5 V/ns	0.55	0.55	ns
-75/-75Z/-75E	0.30 V/ns ≤ Slew Rate < 0.4 V/ns	0.60	0.60	ns

Notes

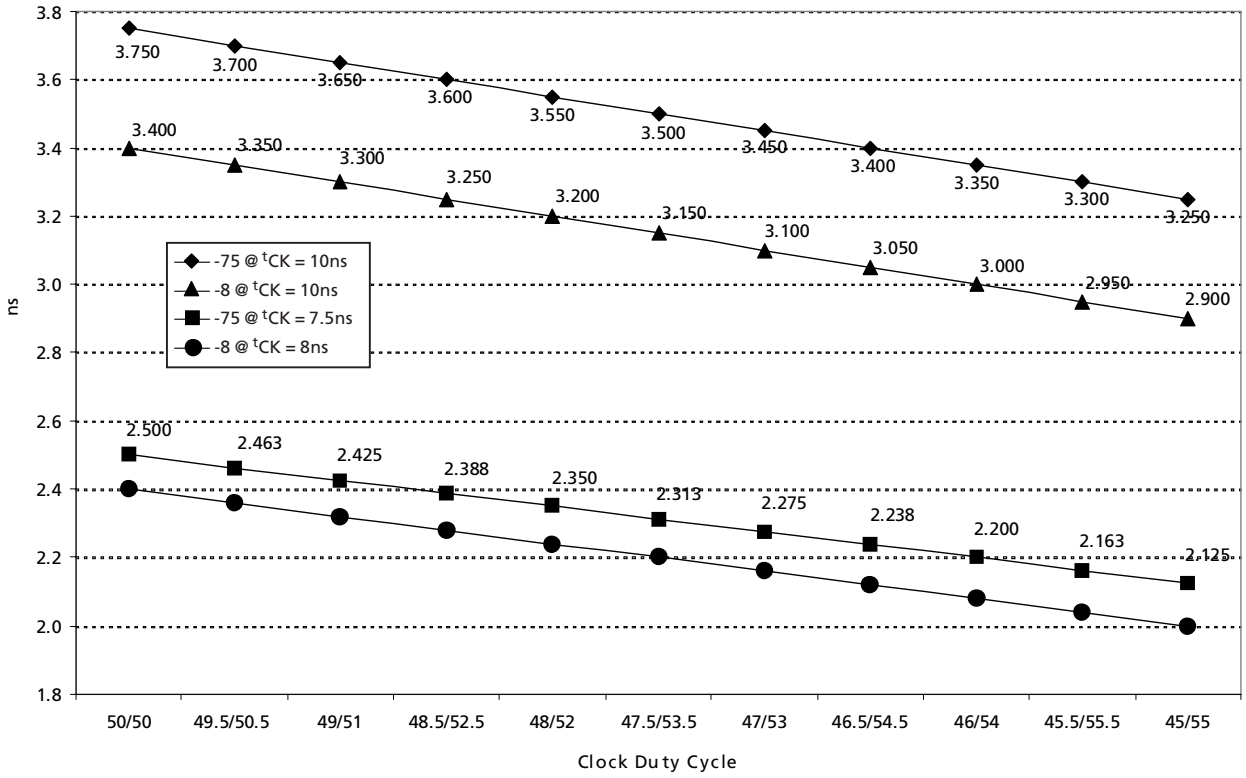
1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs (except for I_{DD} measurements) measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1 V/ns in the range between V_{IL}(AC) and V_{IH}(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from V_{DDQ}/2, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT}, a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
9. The value of V_{IX} and V_{MP} are expected to equal V_{DDQ}/2 of the transmitting device and must track variations in the DC level of the same.
10. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle times at CL = 3 for -5B, CL = 2.5 for -6/-6T and -75, and CL = 2 for -75E/-75Z speeds with the outputs open.
11. Enables on-chip refresh and address counters.
12. I_{DD} specifications are tested after the device is properly initialized and is averaged at the defined cycle rate.
13. This parameter is sampled. V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V, V_{REF} = V_{SS}, f = 100 MHz, T_A = 25°C, V_{OUT} (DC) = V_{DDQ}/2, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting that they are matched in loading.
14. For slew rates < 1 V/ns and ≥ 0.5 V/ns. If slew rate is less than 0.5 V/ns, timing must be derated; ^{t}IS has an additional 50ps per each 100 mV/ns reduction in slew rate from the 500 mV/ns, while ^{t}IH is unaffected. If the slew rate exceeds 4.5 V/ns, functionality is uncertain. For -5B, -6, and -6T, slew rates must be greater than or equal to 0.5 V/ns.
15. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.

16. Inputs are not recognized as valid until V_{REF} stabilizes. Once initialized, including self-refresh mode, V_{REF} must be powered within the specified range. Exception: during the period before V_{REF} stabilizes, CKE = 0.3 x $V_{DD}Q$ is recognized as LOW.
17. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
18. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as data valid transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
19. The intent of the "Don't Care" state after completion of the postamble is that the DQS-driven signal should either be HIGH, LOW, or High-Z and that any signal transition within the input switching region must follow valid input requirements. If DQS transitions HIGH, above DC V_{IH} (MIN) then it must not transition LOW, below DC V_{IH}, prior to $^{t}DQSH$ (MIN).
20. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
21. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on $^{t}DQSS$.
22. ^{t}RC (MIN) or ^{t}RFC (MIN) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
23. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, an AUTO REFRESH command must be asserted at least once every 70.3µs; burst-refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
24. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
25. The data valid window is derived by achieving other specifications: ^{t}HP ($^{t}CK/2$), $^{t}DQSQ$, and ^{t}QH ($^{t}QH = {}^{t}HP - {}^{t}QHS$). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty-cycle variation of 45/55, because functionality is uncertain when operating beyond a 45/55 ratio. Figure 35 on page 71 shows data valid window derating curves for duty cycles ranging between 50/50 and 45/55.
26. Referenced to each output group: x4 = DQS with DQ0–DQ3; x8 = DQS with DQ0–DQ7; x16 = LDQS with DQ0–DQ7; and UDQS with DQ8–DQ15.
27. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
28. To maintain a valid level, the transitioning edge of the input must:
    a. Sustain a constant slew rate from the current AC level through to the target AC level, V_{IL} (AC) or V_{IH} (AC).
    b. Reach at least the target AC level.
    c. After the AC target level is reached, continue to maintain at least the target DC level, V_{IL} (DC) or V_{IH} (DC).
29. The Input capacitance per pin group will not differ by more than this maximum amount for any given device.

Figure 35: Derating Data Valid Window (^{t}QH – ^{t}DQSQ)
Examples are for speed grades through -75.



30. CK and CK# input slew rate must be ≥ 1 V/ns (≥ 2 V/ns if measured differentially).
31. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 0.5 V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 0.1 V/ns reduction in slew rate. For -5B, -6, and -6T speed grades, slew rate must be ≥ 0.5 V/ns. If slew rate exceeds 4 V/ns, functionality is uncertain.
32. V_{DD} must not vary more than four percent if CKE is not active while any bank is active.
33. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
34. ^{t}HP (MIN) is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK# inputs, collectively during bank active.
35. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS (MIN) can be satisfied prior to the internal PRECHARGE command being issued.
36. Any positive glitch must be less than 1/3 of the clock cycle and not more than +400mV or 2.9V (+300mV or 2.9V maximum for -5B), whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2V, (2.4V for -5B) whichever is more positive. The average cannot be below the +2.5V (2.6V for -5B) minimum.
37. Normal output drive curves:
    a. The full variation in driver pull-down current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V-I curve of Figure 36.

b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 36.
c. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 37.
d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 37.
e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4 for device drain-to-source voltages from 0.1V to 1.0V and at the same voltage and temperature. The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent for device drain-to-source voltages from 0.1V to 1.0V.

Figure 36: Full Drive Pull-Down Characteristics

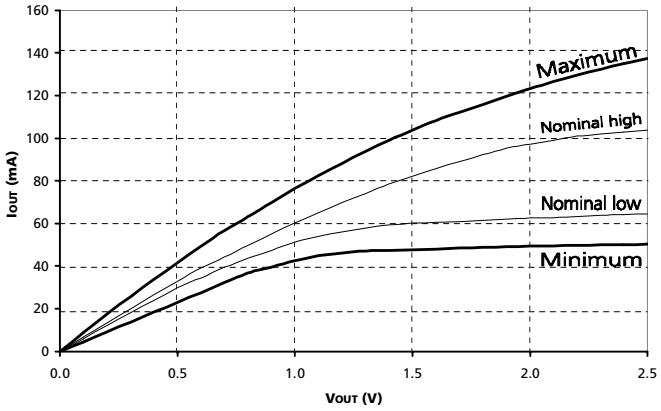
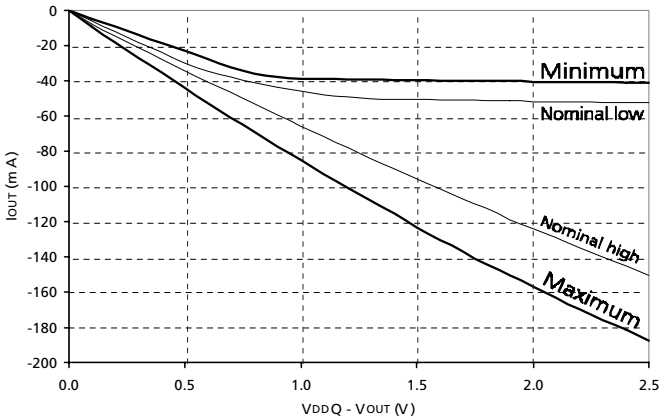


Figure 37: Full Drive Pull-Up Characteristics



38. Reduced output drive curves:
    a. The full variation in driver pull-down current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V-I curve of Figure 38.
    b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 38.
    c. The full variation in driver pull-up current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V-I curve of Figure 39.
    d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 39.
    e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4 for device drain-to-source voltages from 0.1V to 1.0V and at the same voltage and temperature.
    f. The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent for device drain-to-source voltages from 0.1V to 1.0V.

Figure 38: Reduced Drive Pull-Down Characteristics

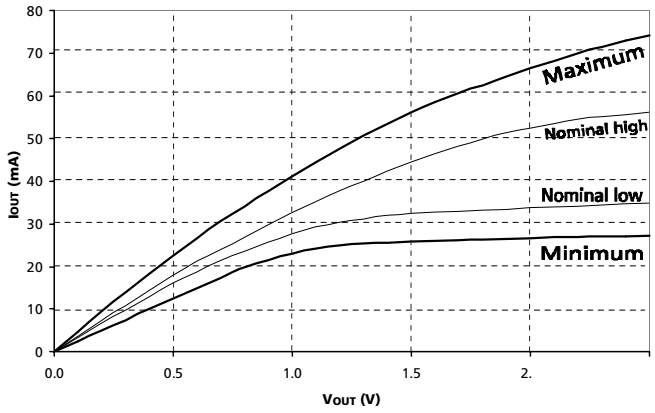
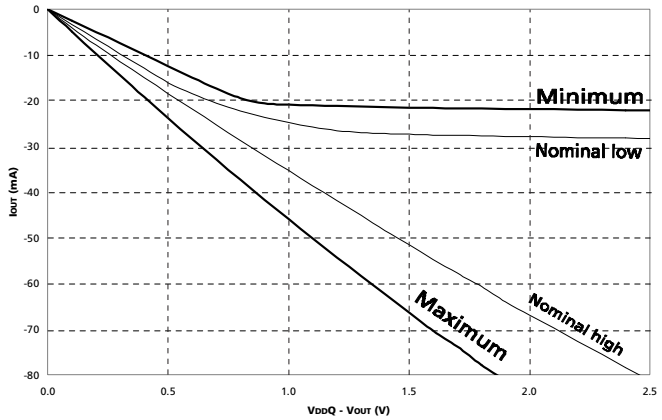


Figure 39: Reduced Drive Pull-Up Characteristics



39. The voltage levels used are derived from a minimum V_{DD} level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
40. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = –1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
41. V_{DD} and $V_{DD}Q$ must track each other.
42. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition. ^{t}LZ (MIN) will prevail over ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.
43. ^{t}RPST end point and ^{t}RPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (^{t}RPST), or begins driving (^{t}RPRE).
44. During initialization, $V_{DD}Q$, V_{TT}, and V_{REF} must be equal to or less than V_{DD} + 0.3V. Alternatively, V_{TT} may be 1.35V maximum during power-up, even if V_{DD}/$V_{DD}Q$ are 0V, provided a minimum of 42Ω of series resistance is used between the V_{TT} supply and the input pin.
45. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
46. When an input signal is indicated to be HIGH or LOW, it is defined as a steady state logic HIGH or LOW.
47. Random addressing changing; 50 percent of data changing at every transfer.
48. Random addressing changing; 100 percent of data changing at every transfer.
49. CKE must be active (HIGH) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}RFC has been satisfied.
50. I_{DD}2N specifies the DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level. I_{DD}2Q is similar to I_{DD}2F except I_{DD}2Q specifies the address and control inputs to remain stable. Although I_{DD}2F, I_{DD}2N, and I_{DD}2Q are similar, I_{DD}2F is “worst case.”
51. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset followed by 200 clock cycles before any READ command.
52. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz. Any noise above 20 MHz at the DRAM generated from any source other than that of the DRAM itself may not exceed the DC voltage range of 2.6V ±100mV.
53. The -6/-6T speed grades will operate with ^{t}RAS (MIN) = 40ns and ^{t}RAS (MAX) = 120,000ns at any slower frequency.

Output Drive Characteristics

Table 32: Normal Output Drive Characteristics

Voltage (V)	Pull-Down CurrenT (mA)				Pull-Up Current (mA)			
	Nominal Low	Nominal High	Min	Max	Nominal Low	Nominal High	Min	Max
0.1	6.0	6.8	4.6	9.6	–6.1	–7.6	–4.6	–10.0
0.2	12.2	13.5	9.2	18.2	–12.2	–14.5	–9.2	–20.0
0.3	18.1	20.1	13.8	26.0	–18.1	–21.2	–13.8	–29.8
0.4	24.1	26.6	18.4	33.9	–24.0	–27.7	–18.4	–38.8
0.5	29.8	33.0	23.0	41.8	–29.8	–34.1	–23.0	–46.8
0.6	34.6	39.1	27.7	49.4	–34.3	–40.5	–27.7	–54.4
0.7	39.4	44.2	32.2	56.8	–38.1	–46.9	–32.2	–61.8
0.8	43.7	49.8	36.8	63.2	–41.1	–53.1	–36.0	–69.5
0.9	47.5	55.2	39.6	69.9	–43.8	–59.4	–38.2	–77.3
1.0	51.3	60.3	42.6	76.3	–46.0	–65.5	–38.7	–85.2
1.1	54.1	65.2	44.8	82.5	–47.8	–71.6	–39.0	–93.0
1.2	56.2	69.9	46.2	88.3	–49.2	–77.6	–39.2	–100.6
1.3	57.9	74.2	47.1	93.8	–50.0	–83.6	–39.4	–108.1
1.4	59.3	78.4	47.4	99.1	–50.5	–89.7	–39.6	–115.5
1.5	60.1	82.3	47.7	103.8	–50.7	–95.5	–39.9	–123.0
1.6	60.5	85.9	48.0	108.4	–51.0	–101.3	–40.1	–130.4
1.7	61.0	89.1	48.4	112.1	–51.1	–107.1	–40.2	–136.7
1.8	61.5	92.2	48.9	115.9	–51.3	–112.4	–40.3	–144.2
1.9	62.0	95.3	49.1	119.6	–51.5	–118.7	–40.4	–150.5
2.0	62.5	97.2	49.4	123.3	–51.6	–124.0	–40.5	–156.9
2.1	62.8	99.1	49.6	126.5	–51.8	–129.3	–40.6	–163.2
2.2	63.3	100.9	49.8	129.5	–52.0	–134.6	–40.7	–169.6
2.3	63.8	101.9	49.9	132.4	–52.2	–139.9	–40.8	–176.0
2.4	64.1	102.8	50.0	135.0	–52.3	–145.2	–40.9	–181.3
2.5	64.6	103.8	50.2	137.3	–52.5	–150.5	–41.0	–187.6
2.6	64.8	104.6	50.4	139.2	–52.7	–155.3	–41.1	–192.9
2.7	65.0	105.4	50.5	140.8	–52.8	–160.1	–41.2	–198.2

Note: The above characteristics are specified under best, worst, and nominal process variations/ conditions.

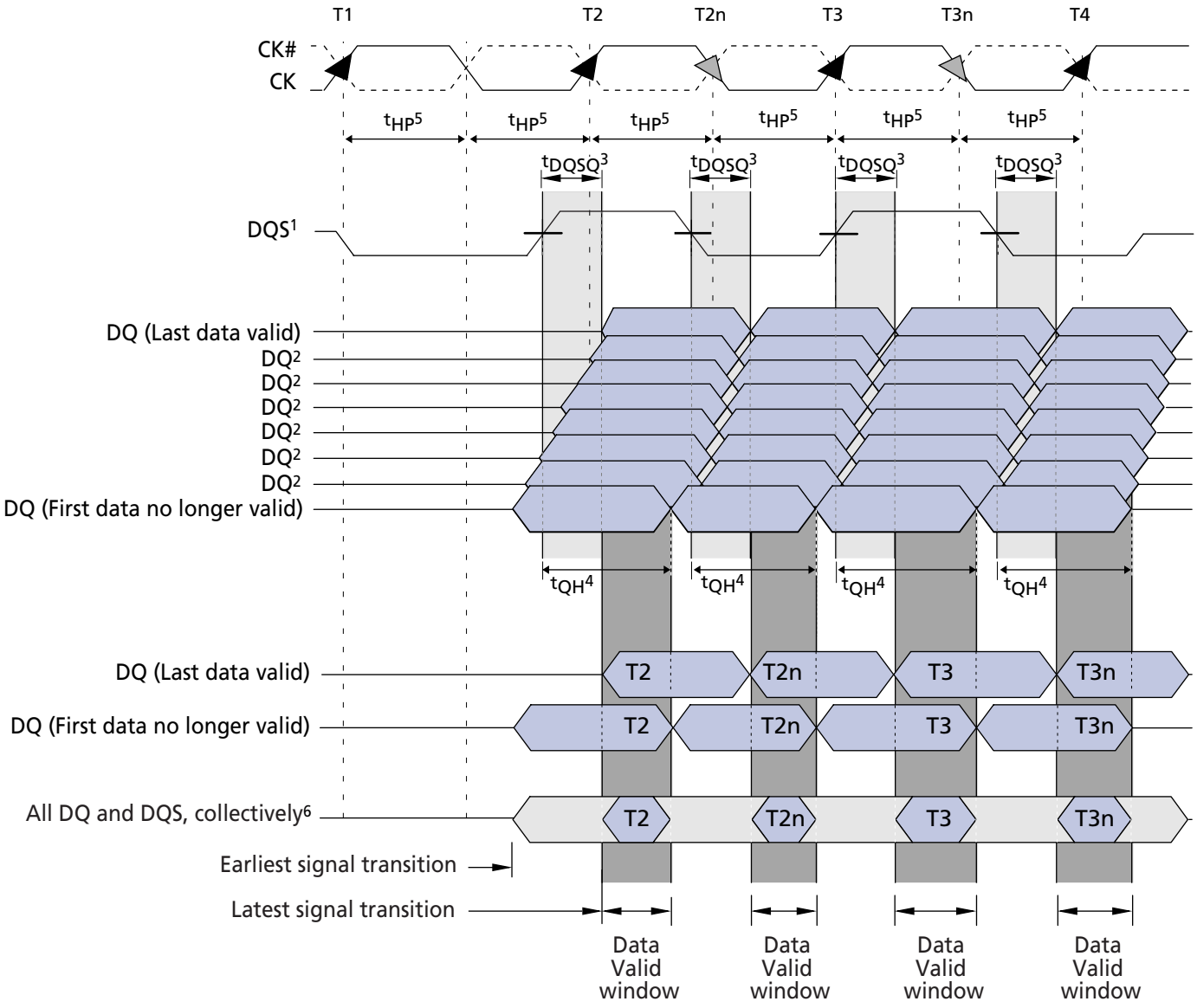
Table 33: Reduced Output Drive Characteristics

Voltage (V)	Pull-Down CurrenT (mA)				Pull-Up Current (mA)			
	Nominal Low	Nominal High	Min	Max	Nominal Low	Nominal High	Min	Max
0.1	3.4	3.8	2.6	5.0	–3.5	–4.3	–2.6	–5.0
0.2	6.9	7.6	5.2	9.9	–6.9	–7.8	–5.2	–9.9
0.3	10.3	11.4	7.8	14.6	–10.3	–12.0	–7.8	–14.6
0.4	13.6	15.1	10.4	19.2	–13.6	–15.7	–10.4	–19.2
0.5	16.9	18.7	13.0	23.6	–16.9	–19.3	–13.0	–23.6
0.6	19.9	22.1	15.7	28.0	–19.4	–22.9	–15.7	–28.0
0.7	22.3	25.0	18.2	32.2	–21.5	–26.5	–18.2	–32.2
0.8	24.7	28.2	20.8	35.8	–23.3	–30.1	–20.4	–35.8
0.9	26.9	31.3	22.4	39.5	–24.8	–33.6	–21.6	–39.5
1.0	29.0	34.1	24.1	43.2	–26.0	–37.1	–21.9	–43.2
1.1	30.6	36.9	25.4	46.7	–27.1	–40.3	–22.1	–46.7
1.2	31.8	39.5	26.2	50.0	–27.8	–43.1	–22.2	–50.0
1.3	32.8	42.0	26.6	53.1	–28.3	–45.8	–22.3	–53.1
1.4	33.5	44.4	26.8	56.1	–28.6	–48.4	–22.4	–56.1
1.5	34.0	46.6	27.0	58.7	–28.7	–50.7	–22.6	–58.7
1.6	34.3	48.6	27.2	61.4	–28.9	–52.9	–22.7	–61.4
1.7	34.5	50.5	27.4	63.5	–28.9	–55.0	–22.7	–63.5
1.8	34.8	52.2	27.7	65.6	–29.0	–56.8	–22.8	–65.6
1.9	35.1	53.9	27.8	67.7	–29.2	–58.7	–22.9	–67.7
2.0	35.4	55.0	28.0	69.8	–29.2	–60.0	–22.9	–69.8
2.1	35.6	56.1	28.1	71.6	–29.3	–61.2	–23.0	–71.6
2.2	35.8	57.1	28.2	73.3	–29.5	–62.4	–23.0	–73.3
2.3	36.1	57.7	28.3	74.9	–29.5	–63.1	–23.1	–74.9
2.4	36.3	58.2	28.3	76.4	–29.6	–63.8	–23.2	–76.4
2.5	36.5	58.7	28.4	77.7	–29.7	–64.4	–23.2	–77.7
2.6	36.7	59.2	28.5	78.8	–29.8	–65.1	–23.3	–78.8
2.7	36.8	59.6	28.6	79.7	–29.9	–65.8	–23.3	–79.7

Note: The above characteristics are specified under best, worst, and nominal process variations/ conditions.

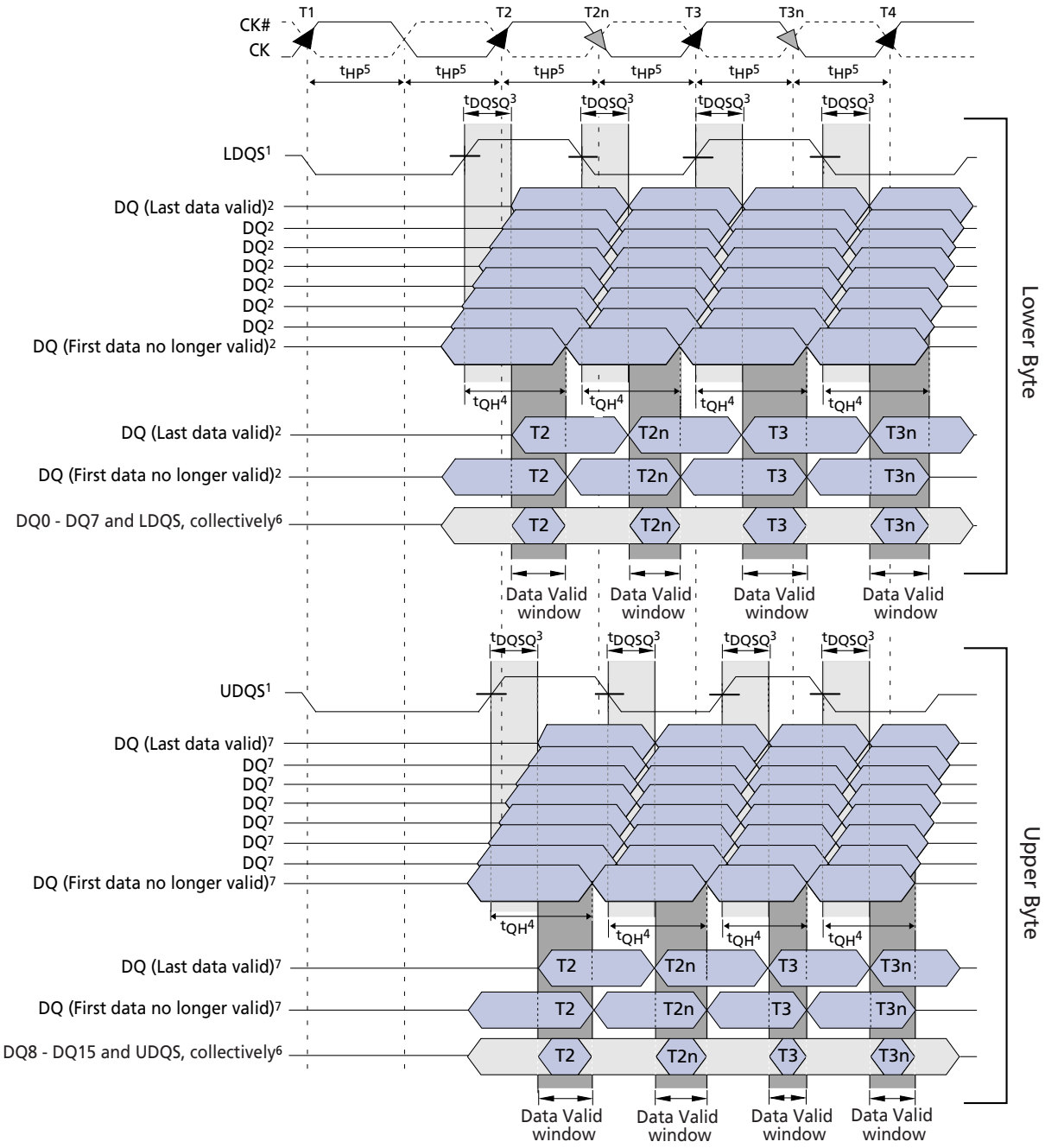
Data Output Timing Diagrams

Figure 40: x4, x8 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



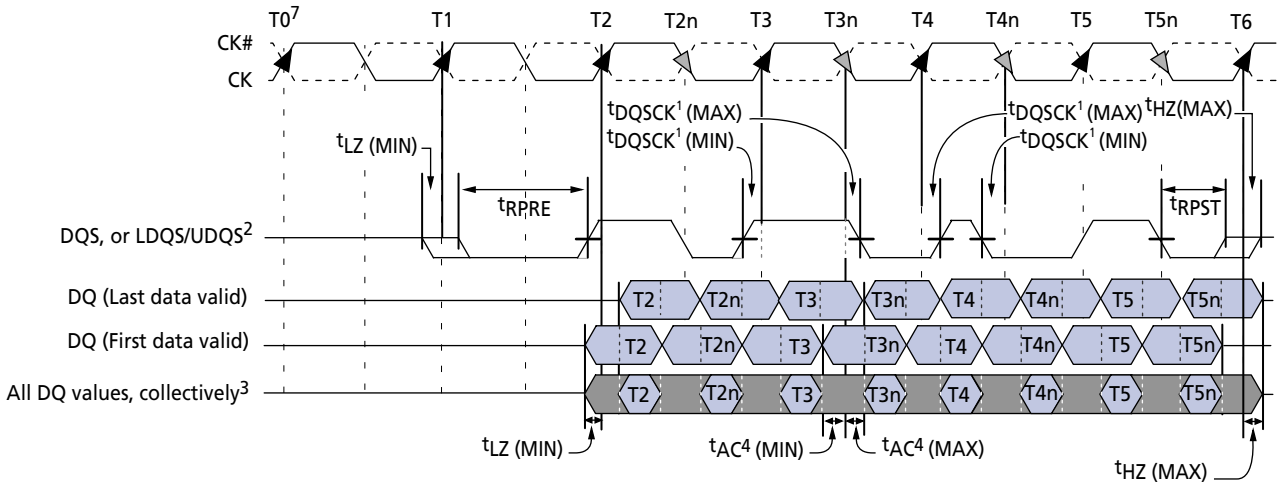
Notes:
1. DQ transitioning after DQS transition define ^{t}DQSQ window. DQS transitions at T2 and at T2n are "early DQS," at T3, "nominal DQS," and at T3n, "late DQS."
2. For a x4, only two DQ apply.
3. ^{t}DQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
4. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
5. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transition collectively when a bank is active.
6. The data valid window is derived for each DQS transitions and is defined as ^{t}QH minus ^{t}DQSQ.

Figure 41: x16 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



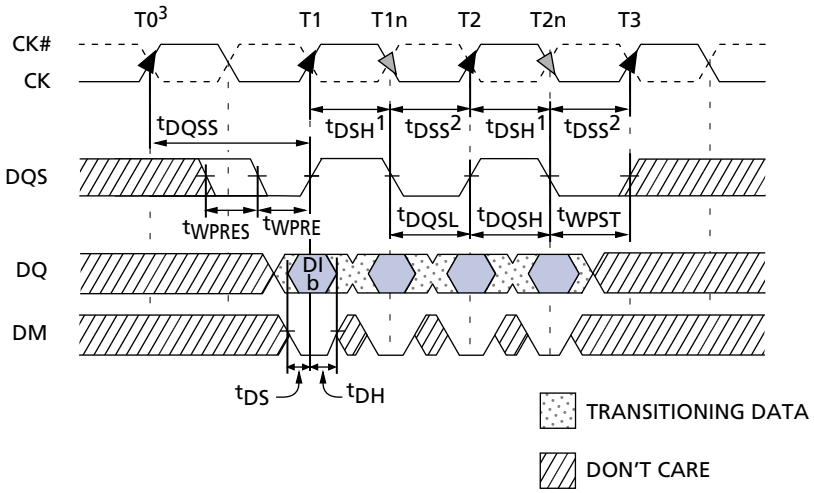
Notes:
1. DQ transitioning after DQS transition define ^{t}DQSQ window. LDQS defines the lower byte and UDQS defines the upper byte.
2. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
3. ^{t}DQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
4. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
5. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transition collectively when a bank is active.
6. The data valid window is derived for each DQS transition and is ^{t}QH minus ^{t}DQSQ.
7. DQ8, DQ9, DQ10, D11, DQ12, DQ13, DQ14, or DQ15.

Figure 42: Data Output Timing – ^{t}AC and ^{t}DQSCK



Notes:
1. ^{t}DQSCK is the DQS output window relative to CK and is the "long-term" component of DQS skew.
2. DQ transitioning after DQS transition define ^{t}DQSQ window.
3. All DQ must transition by ^{t}DQSQ after DQS transitions, regardless of ^{t}AC.
4. ^{t}AC is the DQ output window relative to CK, and is the "long-term" component of DQ skew.
5. ^{t}LZ (MIN) and ^{t}AC (MIN) are the first valid signal transition.
6. ^{t}HZ (MAX),and ^{t}AC (MAX) are the latest valid signal transition.
7. READ command with CL = 2 issued at T0.

Figure 43: Data Input Timing



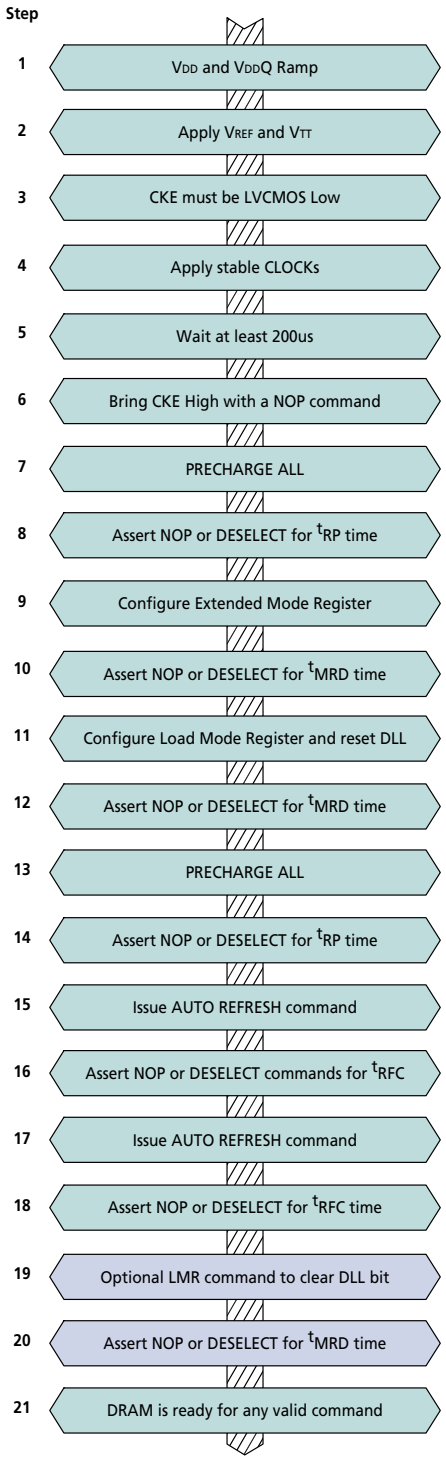
Notes: 1. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
2. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).
3. WRITE command issued at T0.
4. For x16, LDQS controls the lower byte and UDQS controls the upper byte.

Initialization

To ensure device operation the DRAM must be initialized as described below:

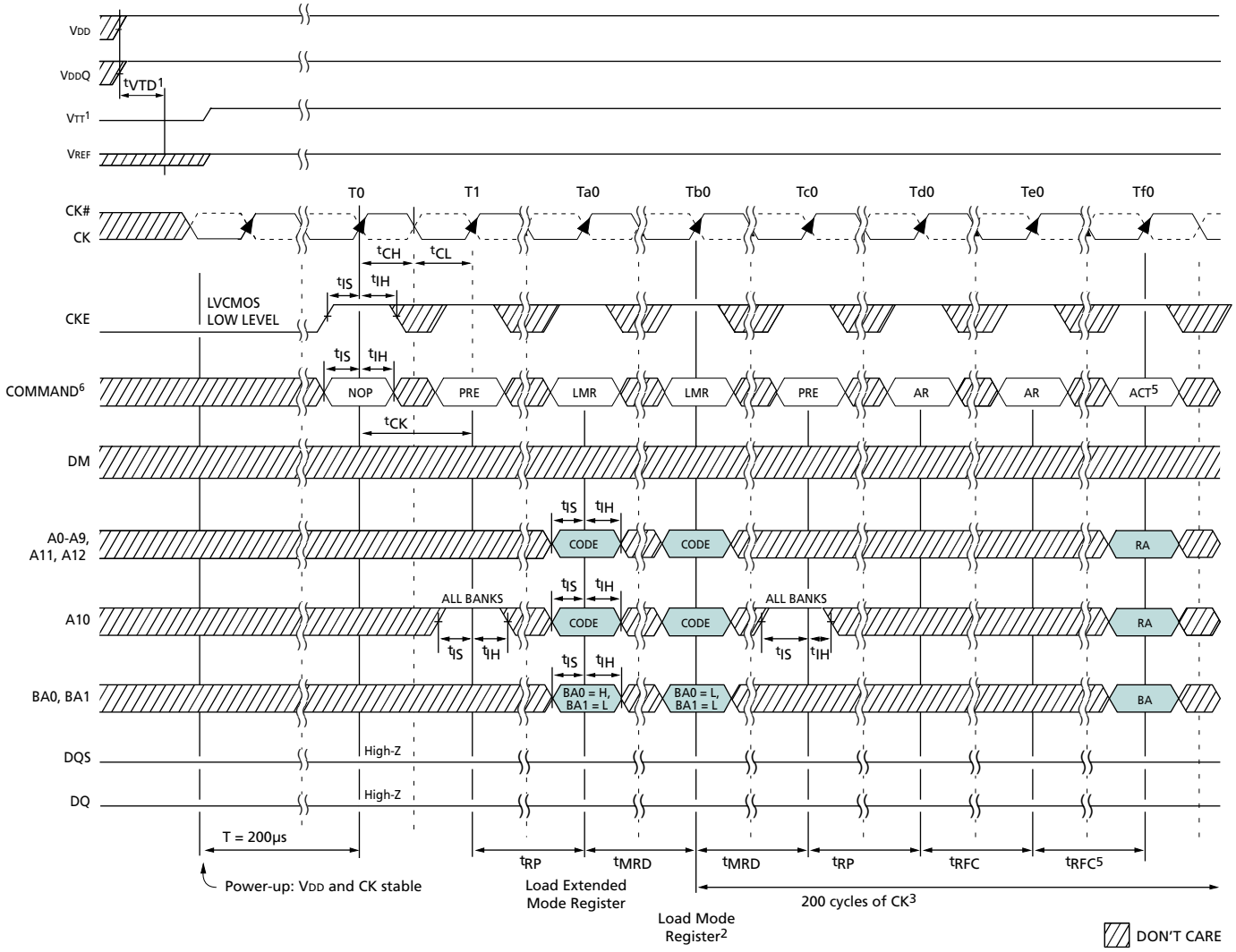
1. Simultaneously apply power to VDD and VDDQ.
2. Apply VREF and then VTT power.
3. Assert and hold CKE at a LVCMOS logic low.
4. Provide stable CLOCK signals.
5. Wait at least 200µs.
6. Bring CKE high and provide at least one NOP or DESELECT command. At this point the CKE input changes from a LVCMOS input to a SSTL2 input only and will remain a SSTL_2 input unless a power cycle occurs.
7. Perform a PRECHARGE ALL command.
8. Wait at least ^{t}RP time, during this time NOPs or DESELECT commands must be given.
9. Using the LMR command program the Extended Mode Register (E0 = 0 to enable the DLL and E1 = 0 for normal drive or E1 = 1 for reduced drive, E2 through En must be set to 0; where n = most significant bit).
10. Wait at least ^{t}MRD time, only NOPs or DESELECT commands are allowed.
11. Using the LMR command program the Mode Register to set operating parameters and to reset the DLL. Note at least 200 clock cycles are required between a DLL reset and any READ command.
12. Wait at least ^{t}MRD time, only NOPs or DESELECT commands are allowed.
13. Issue a PRECHARGE ALL command.
14. Wait at least ^{t}RP time, only NOPs or DESELECT commands are allowed.
15. Issue an AUTO REFRESH command (Note this may be moved prior to step 13).
16. Wait at least ^{t}RFC time, only NOPs or DESELECT commands are allowed.
17. Issue an AUTO REFRESH command (Note this may be moved prior to step 13).
18. Wait at least ^{t}RFC time, only NOPs or DESELECT commands are allowed.
19. Although not required by the Micron device, JEDEC requires a LMR command to clear the DLL bit (set M8 = 0). If a LMR command is issued the same operating parameters should be utilized as in step 11.
20. Wait at least ^{t}MRD time, only NOPs or DESELECT commands are allowed.
21. At this point the DRAM is ready for any valid command. Note 200 clock cycles are required between step 11 (DLL Reset) and any READ command.

Figure 44: Initialization Flow Diagram



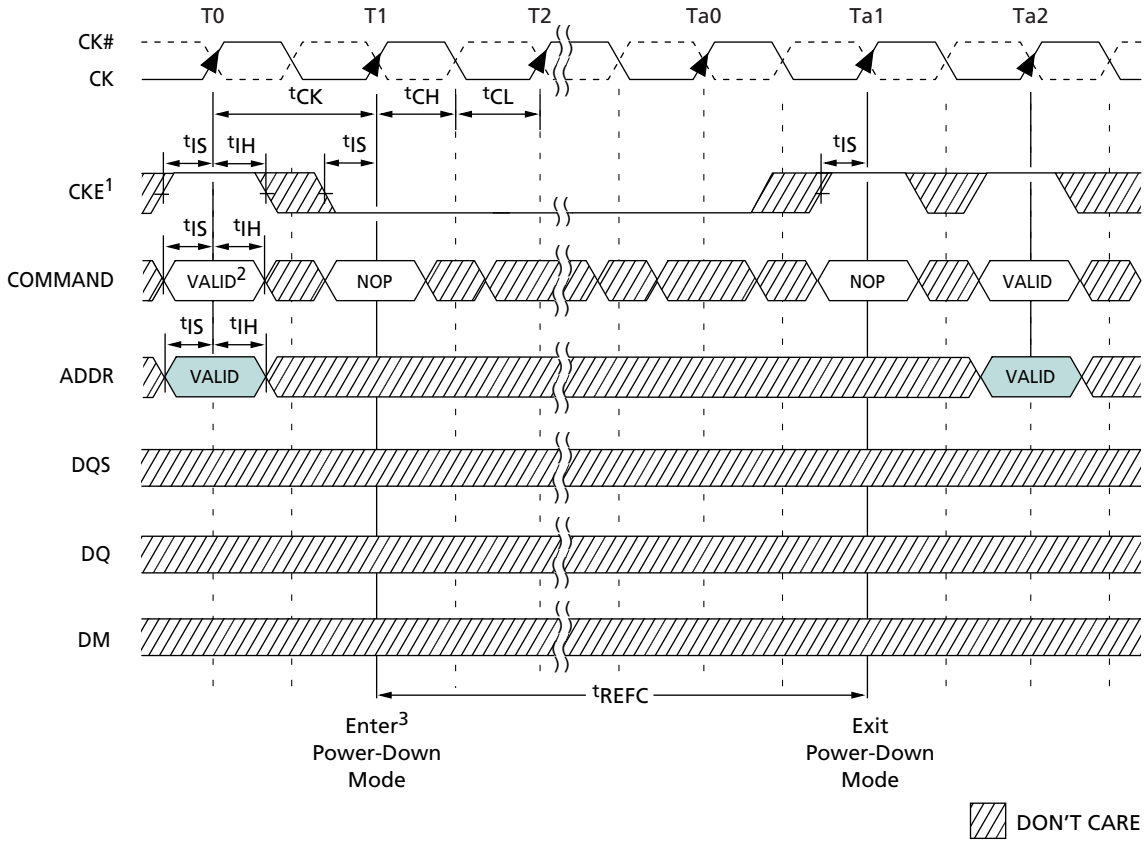
Timing Diagrams

Figure 45: Initialize and Load Mode Registers



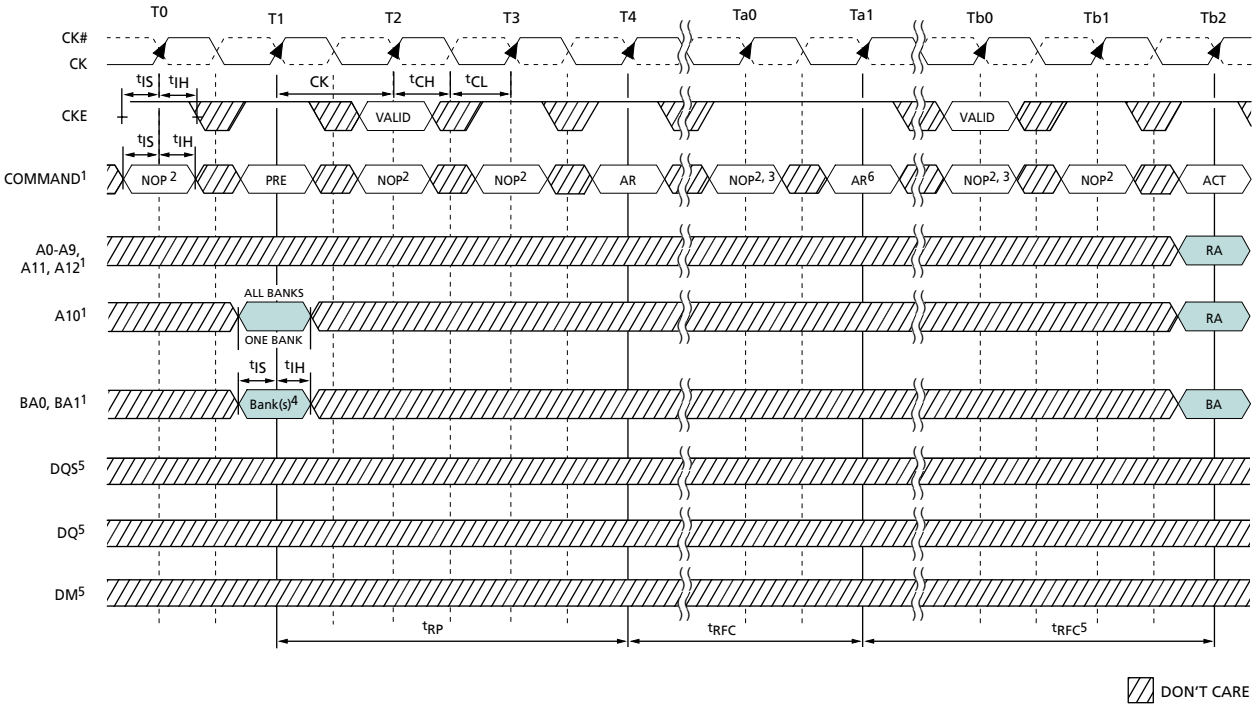
Notes:
1. VTT is not applied directly to the device; however, tVTD should be greater than or equal to zero to avoid device latch-up. VDDQ, VTT, and VREF must be equal to or less than VDD + 0.3V. Alternatively, VTT may be 1.35V maximum during power-up, even if VDD/VDDQ are 0V, provided a minimum of 42Ω of series resistance is used between the VTT supply and the input pin. Once initialized, VREF must always be powered within the specified range.
2. Reset the DLL with A8 = H while programming the operating parameters.
3. tMRD is required before any command can be applied, and 200 cycles of CK are required before a READ command can be issued.
4. The two AUTO REFRESH commands at Td0 and Te0 may be applied following the LOAD MODE REGISTER (LMR) command at Ta0.
5. Although not required by the Micron device, JEDEC specifies issuing another LMR command (A8 = L) prior to activating any bank. If another LMR command is issued, the same operating parameters must be used as previously issued.
6. PRE = PRECHARGE command; LMR = LOAD MODE REGISTER command; AR = AUTO REFRESH command; ACT = ACTIVE command; RA = Row Address; and BA = Bank Address.

Figure 46: Power-Down Mode



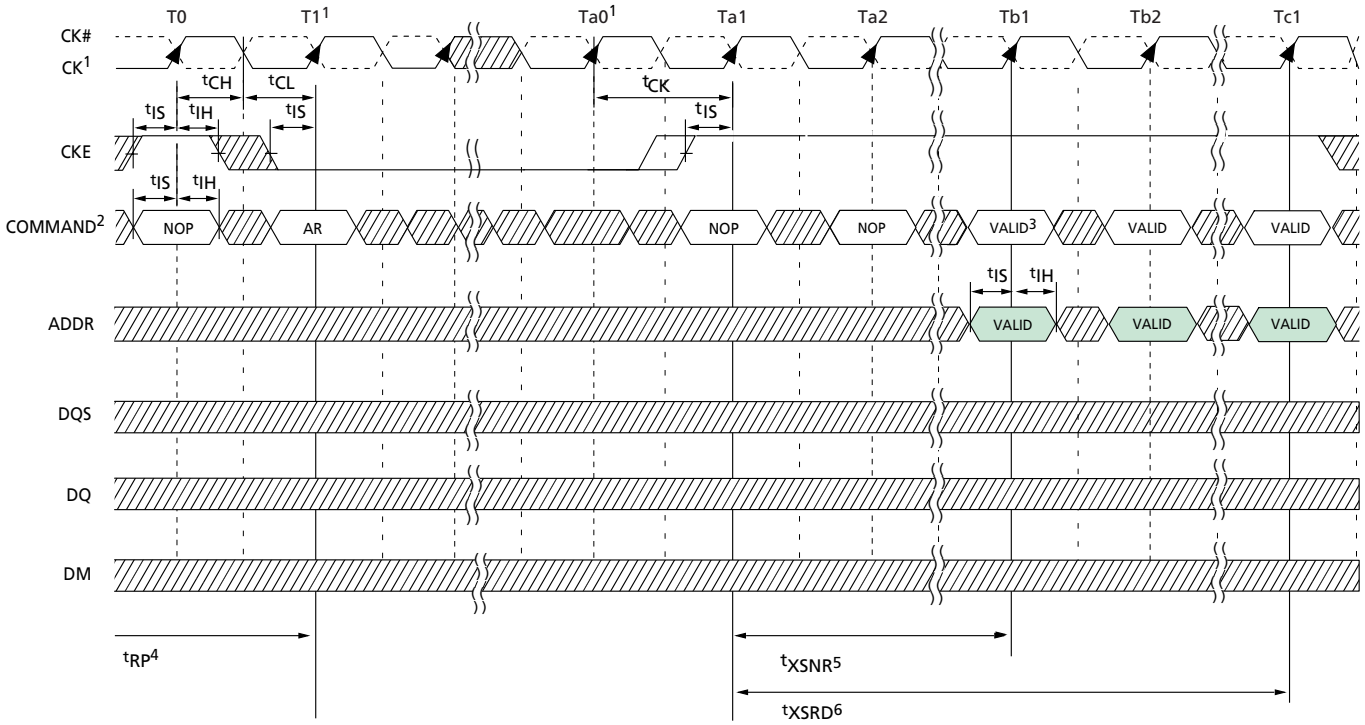
Notes: 1. Once initialized, VREF must always be powered within the specified range.
2. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
3. No column accesses are allowed to be in progress at the time power-down is entered.

Figure 47: Auto Refresh Mode



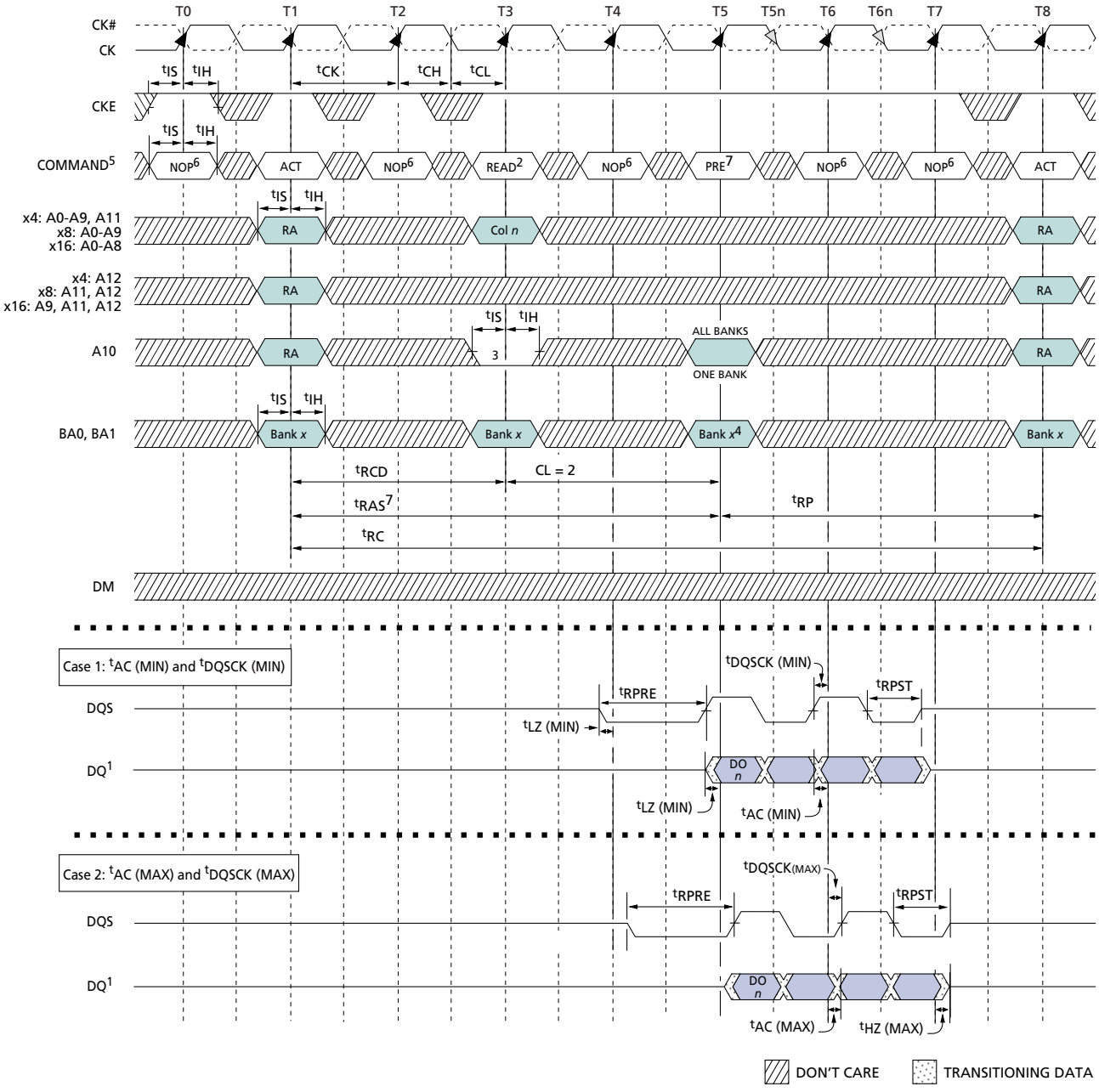
Notes:
1. PRE = PRECHARGE; ACT = ACTIVE; AR = AUTO REFRESH; RA = Row Address; and BA = Bank Address.
2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
3. NOP or COMMAND INHIBIT are the only commands allowed until after ^{t}RFC time; CKE must be active during clock positive transitions.
4. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks).
5. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.
6. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.

Figure 48: Self Refresh Mode



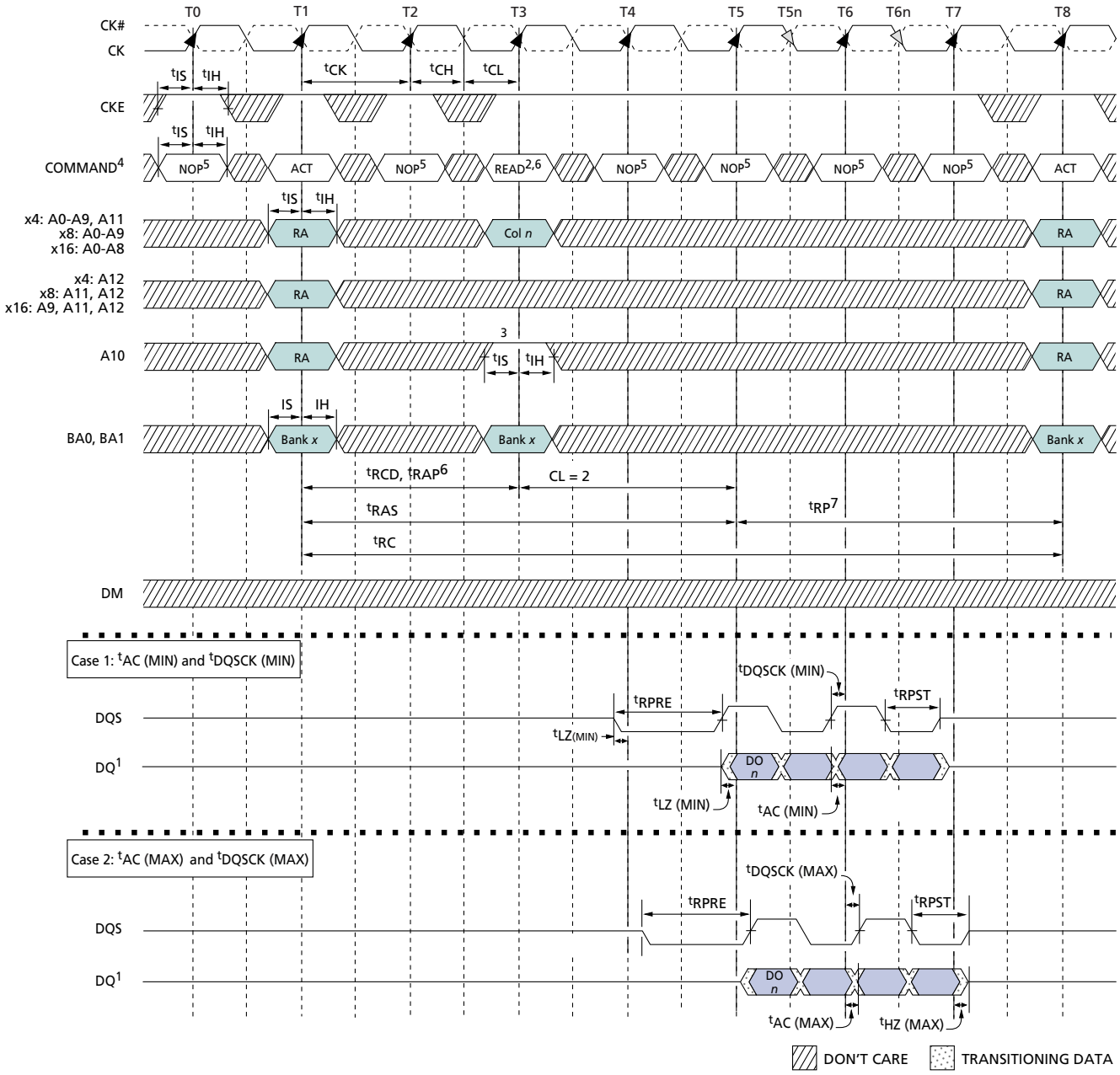
Notes:
1. Clock must be stable until after the SELF REFRESH command has been registered. A change in clock frequency is allowed before Ta0, provided it is within the specified ^{t}CK limits. Regardless, the clock must be stable before exiting self refresh mode. That is, the clock must be cycling within specifications by Ta0.
2. NOPs are interchangeable with DESELECT commands; AR = AUTO REFRESH command.
3. Auto refresh is not required at this point, but is highly recommended.
4. Device must be in the all banks idle state prior to entering self refresh mode.
5. ^{t}XSNR is required before any non-READ command can be applied; only NOP or DESELECT commands are allowed until Tb1.
6. ^{t}XSRD (200 cycles of a valid CK and CKE = high) is required before any READ command can be applied.
7. As a general rule, any time self refresh mode is exited, the DRAM may not re-enter the self refresh mode until all rows have been refreshed via the AUTO REFRESH command at the distributed refresh rate, ^{t}REFI, or faster. However, self refresh mode may be re-entered anytime after exiting, if the following conditions are all met:
   a. The DRAM had been in the self refresh mode for a minimum of 200ms prior to exiting.
   b. ^{t}XSNR and ^{t}XSRD are not violated.
   c. At least two AUTO REFRESH commands are performed during each ^{t}REFI interval while the DRAM remains out of self refresh mode.
8. If the clock frequency is changed during self refresh mode, a DLL reset is required upon exit.
9. Once initialized, including during self-refresh mode, V_{REF} must always be powered within the specified range.

Figure 49: Bank Read – Without Auto Precharge



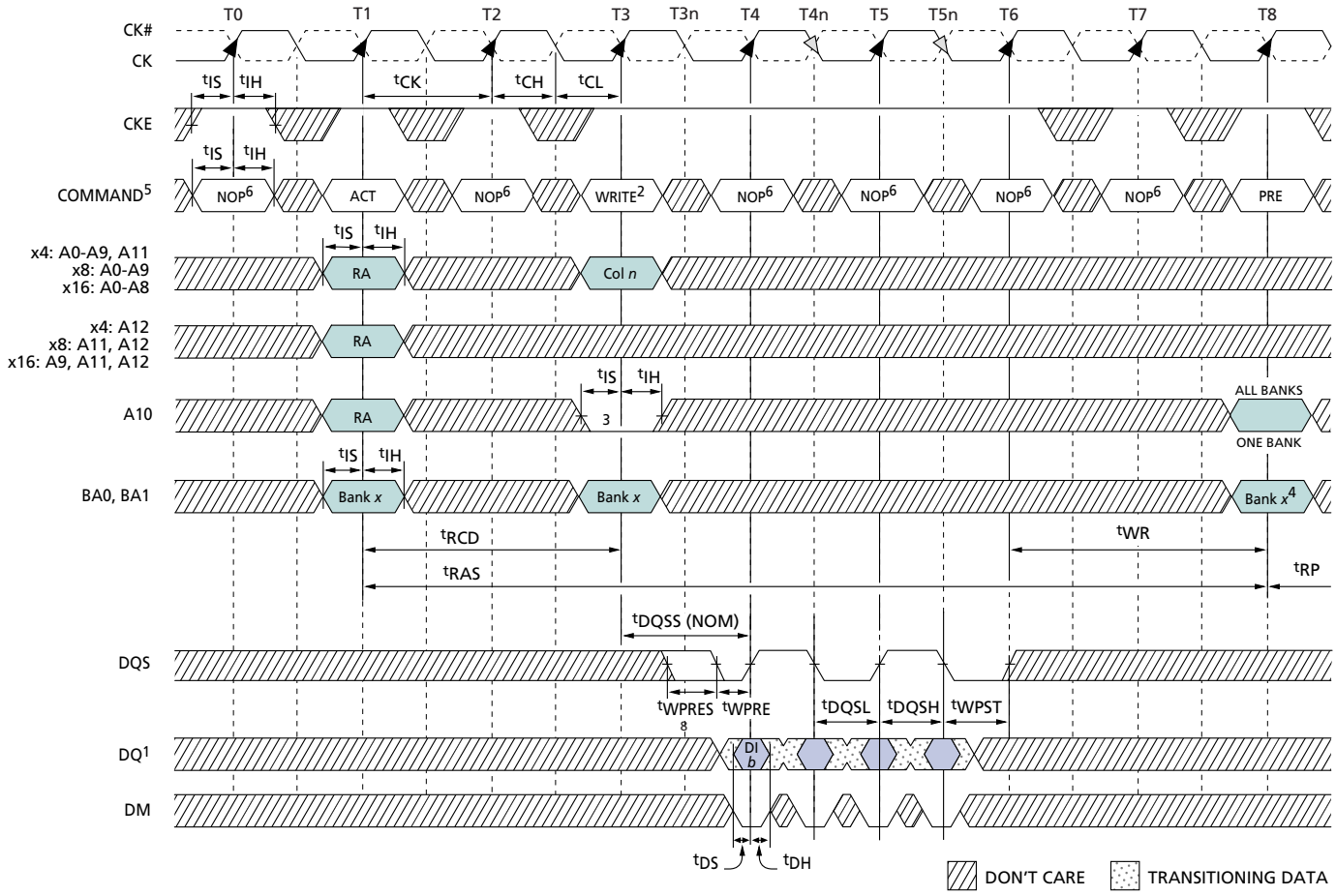
Notes:
1. DO*n* = data-out from column *n*; subsequent elements are provided in the programmed order.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE; ACT = ACTIVE; RA = Row Address; and BA = Bank Address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. The PRECHARGE command can only be applied at T5 if ^{t}RAS minimum is met.
8. Refer to Figure 40 on page 77, Figure 41 on page 78, and Figure 42 on page 79 for detailed DQS and DQ timing.

Figure 50: Bank Read – With Auto Precharge



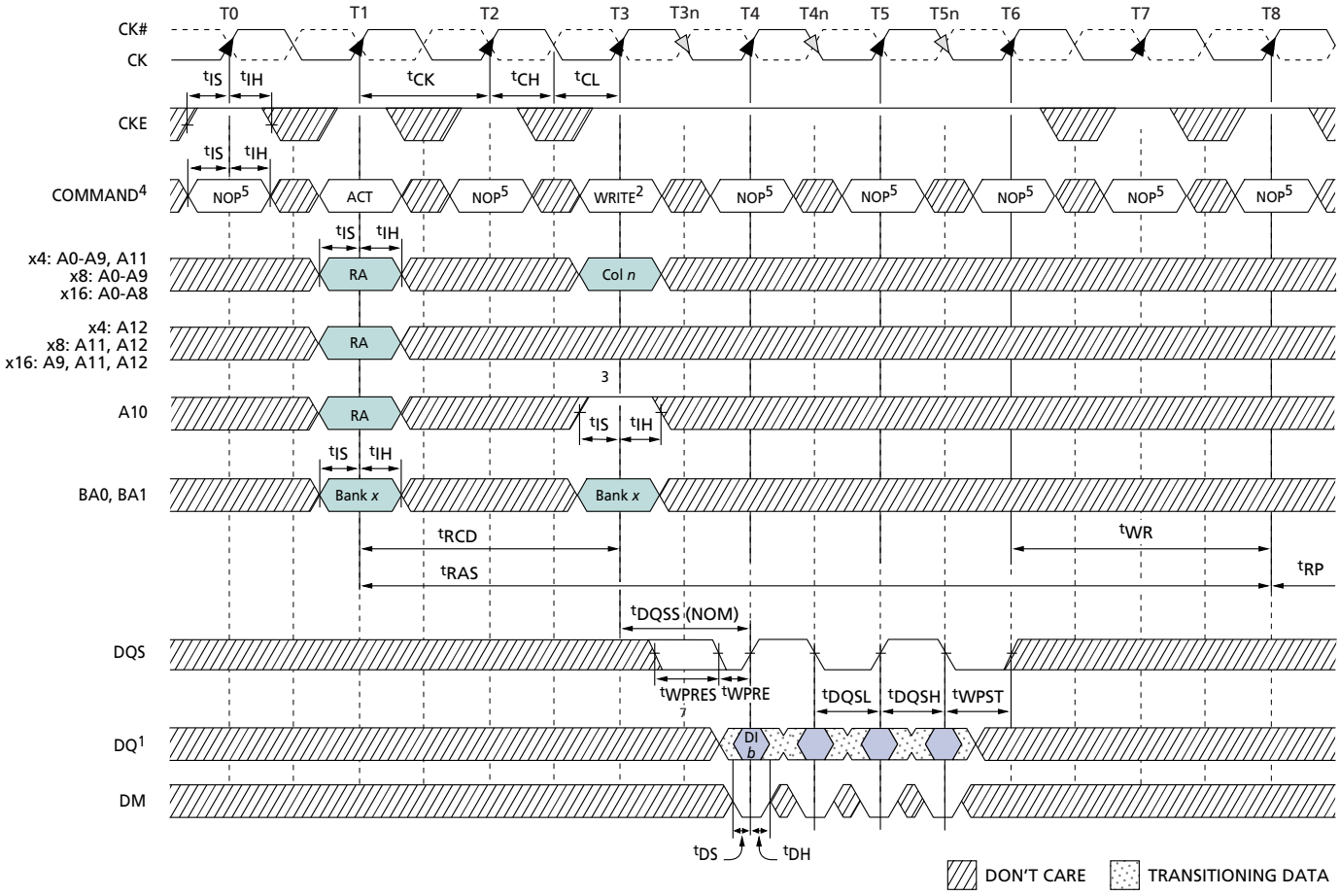
Notes:
1. DO*n* = data-out from column *n;* subsequent elements are provided in the programmed order.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. ACT = ACTIVE; RA = Row Address; and BA = Bank Address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. The READ command can only be applied at T3 if ^{t}RAP is satisfied at T3.
7. ^{t}RP starts only after ^{t}RAS has been satisfied.
8. Refer to Figure 40 on page 77, Figure 41 on page 78, and Figure 42 on page 79 for detailed DQS and DQ timing.

Figure 51: Bank Write – Without Auto Precharge



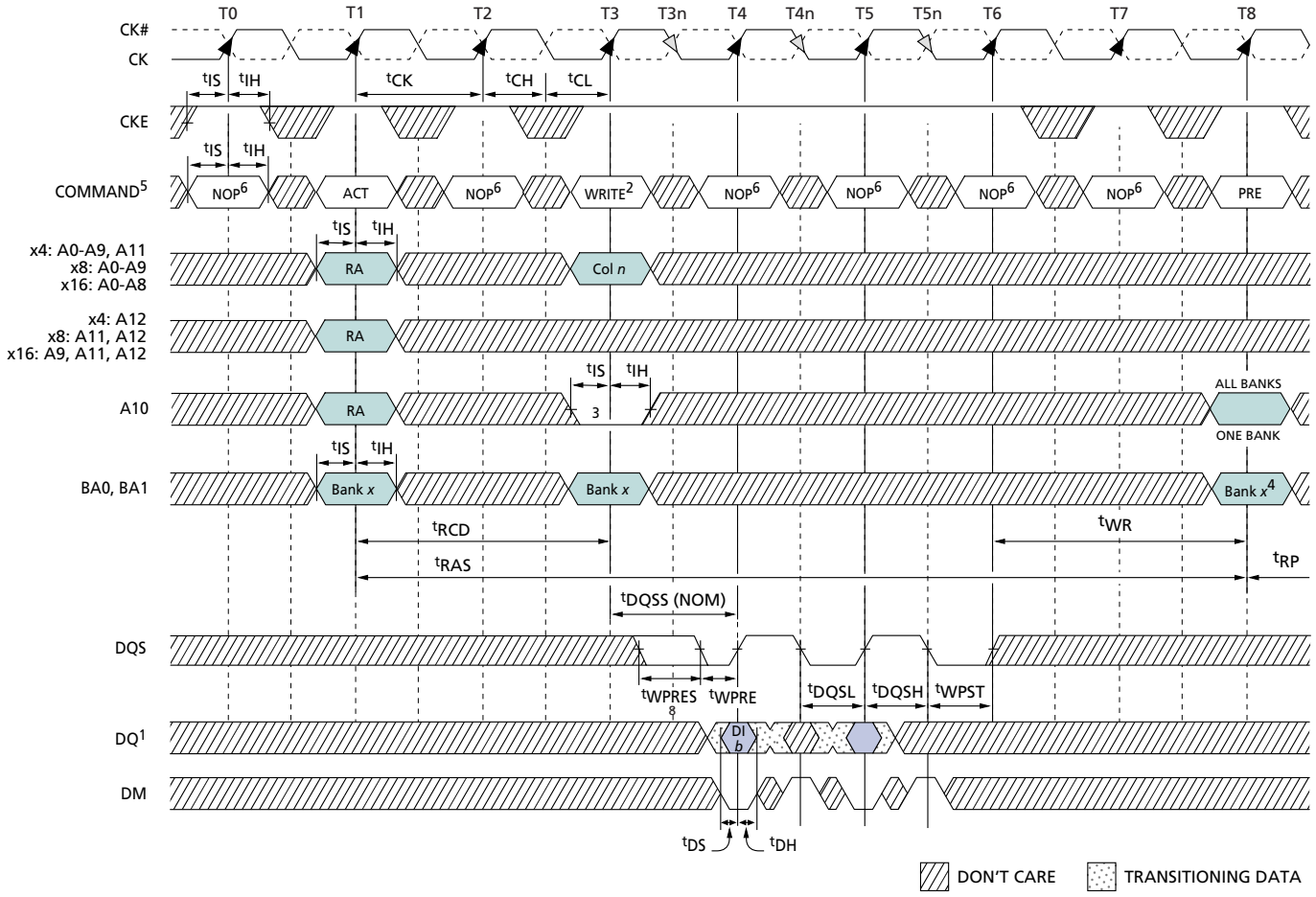
Notes:
1. DI *n* = data-in from column *n*; subsequent elements are provided in the programmed order.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T8.
5. PRE = PRECHARGE; ACT = ACTIVE; RA = Row Address; and BA = Bank Address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. See Figure 43, "Data Input Timing," on page 80, for detailed DQ timing.
8. Although not required by the Micron device, JEDEC specifies that DQS be a valid HIGH, LOW or some point on a valid transition on or before this clock edge (T3n).

Figure 52: Bank Write – With Auto Precharge



Notes:
1. DI*n* = data-out from column *n*; subsequent elements are provided in the programmed order.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. ACT = ACTIVE; RA = Row Address; and BA = Bank Address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. See Figure 43, "Data Input Timing," on page 80, for detailed DQ timing.
7. Although not required by the Micron device, JEDEC specifies that DQS be a valid HIGH, LOW or some point on a valid transition on or before this clock edge (T3n).

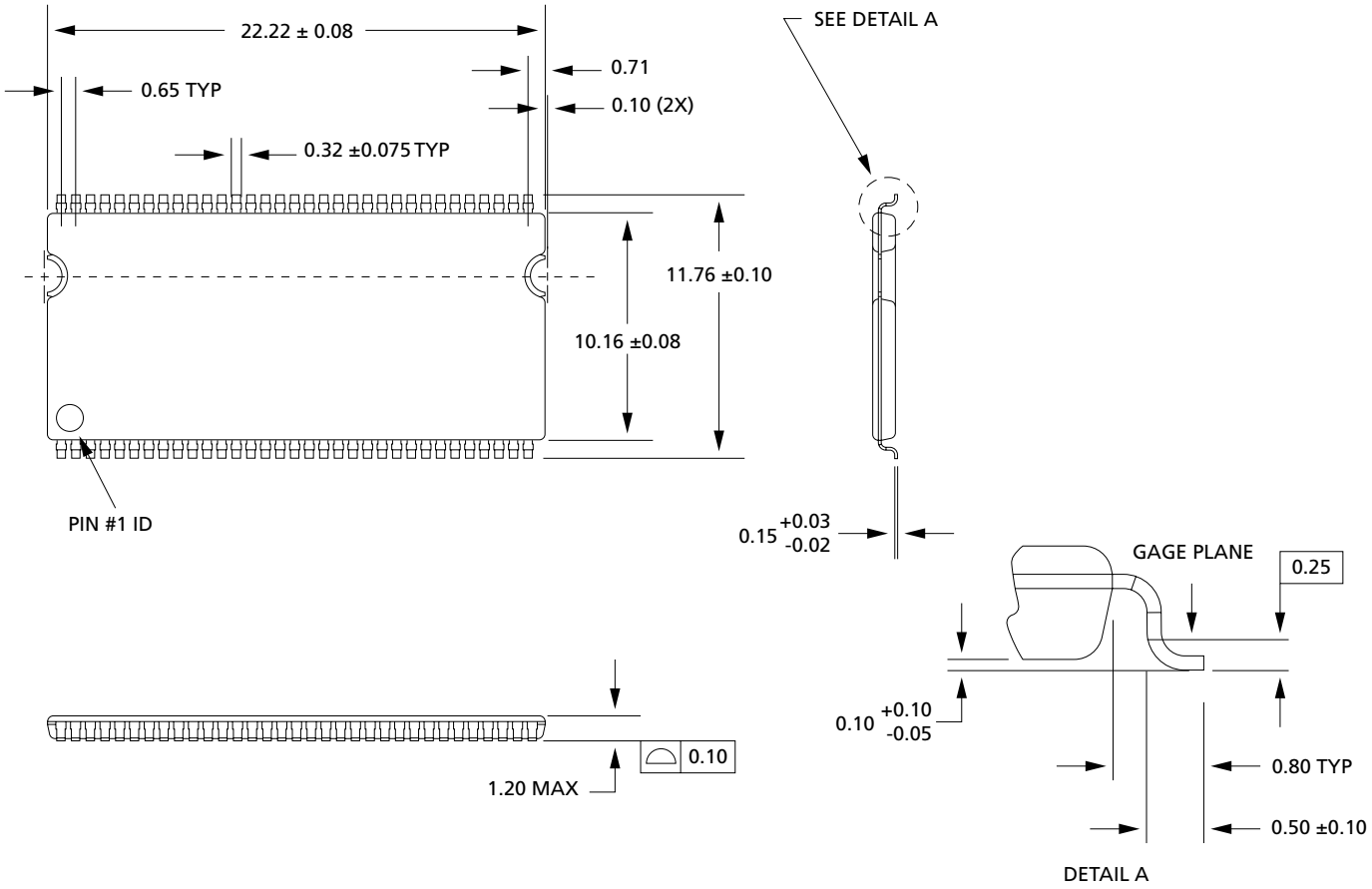
Figure 53: Write – DM Operation



Notes:
1. DI*n* = data-in from column *n*; subsequent elements are provided in the programmed order.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T8.
5. PRE = PRECHARGE; ACT = ACTIVE; RA = Row Address; and BA = Bank Address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. See Figure 43, "Data Input Timing," on page 80, for detailed DQ timing.
8. Although not required by the Micron device, JEDEC specifies that DQS be a valid HIGH, LOW or some point on a valid transition on or before this clock edge (T3n).

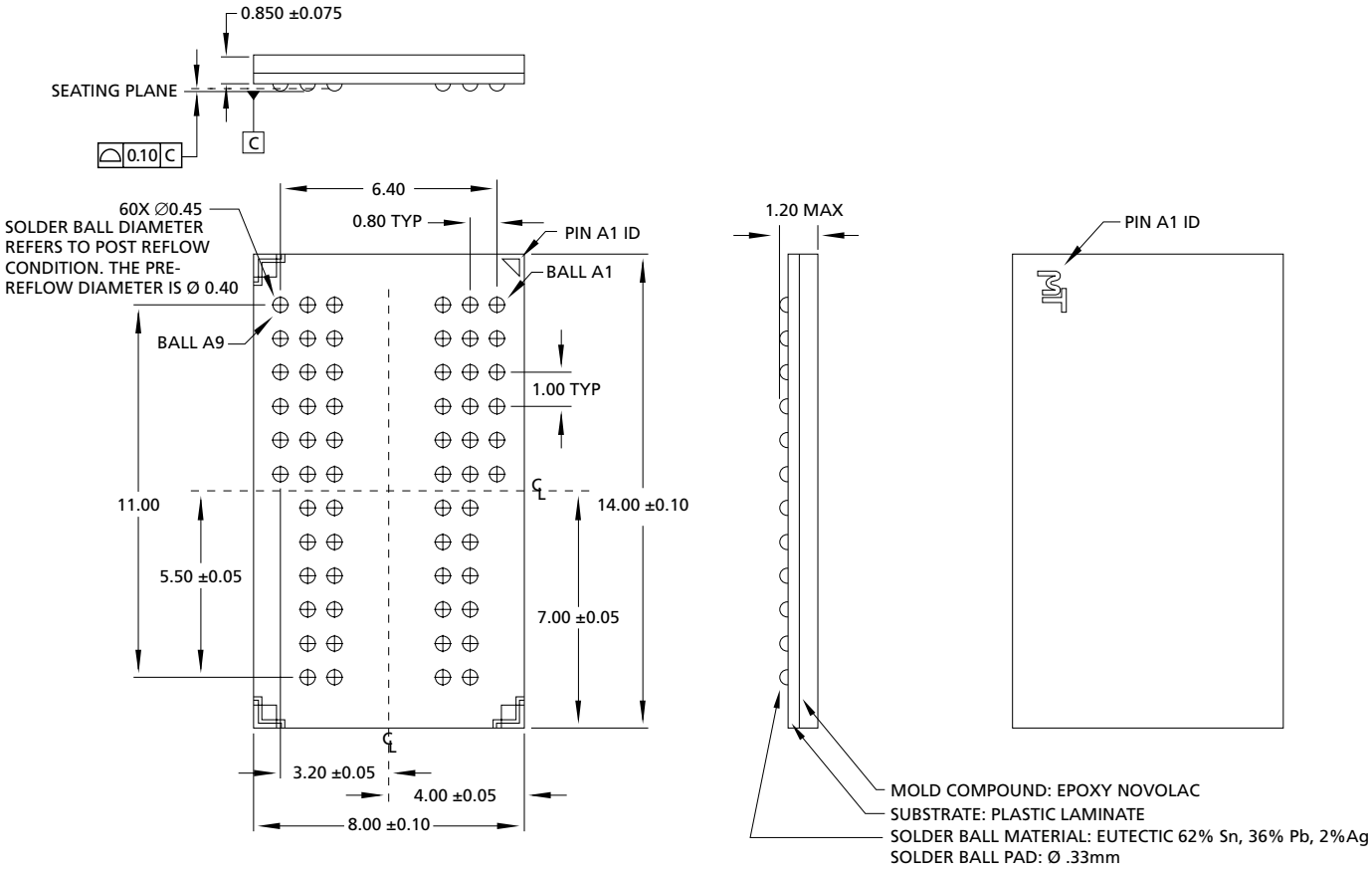
Package Drawings

Figure 54: 66-Pin Plastic TSOP (400 mil)



Notes: 1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

Figure 55: 60-Ball FBGA (8 x 14mm)



Notes: 1. All dimensions are in millimeters.
2. Topside part marking decoder can be found at www.micron.com/decoder.