

Document Title**128Kx8 bit Low Power CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	July 15, 2002	Preliminary
0.1	Revised - Deleted 32-TSOP1-0820R, 32-TSOP1-0813.4F/R Package Type. - Added Commercial product. - Added 55ns product(Vcc = 3.0V~3.6V)	December 4, 2002	Preliminary
0.2	Revised - Added Lead Free 32-SOP-525 Product - Added Lead Free 32-TSOP1-0820F Product	June 23, 2003	Preliminary
1.0	Finalized - Changed Icc from 3mA to 2mA - Changed Icc2 from 25mA to 20mA - Changed Isb1(Commercial) from 10μA to 6μA - Changed Isb1(industrial) from 10μA to 6μA - Changed Isb1(Automotive) from 20μA to 10μA - Changed IdR(Commercial) from 10μA to 6μA - Changed IdR(industrial) from 10μA to 6μA - Changed IdR(Automotive) from 20μA to 10μA	September 16, 2003	Final

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128Kx8 bit Super Low Power and Low Voltage full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 128K x 8
- Power Supply Voltage: 2.7~3.6V
- Low Data Retention Voltage: 1.5V(Min)
- Three state outputs
- Package Type: 32-SOP-525, 32-TSOP1-0820F
32-SOP-525, 32-TSOP1-0820F

GENERAL DESCRIPTION

The K6X1008T2D families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

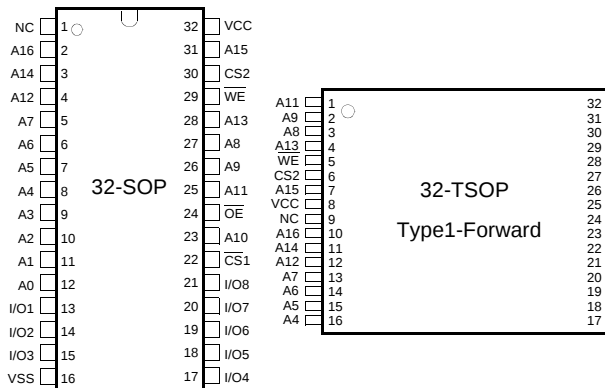
PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
K6X1008T2D-B	Commercial(0~70°C)	2.7~3.6V	55 ¹⁾ /70 ²⁾ /85ns	6μA	20mA	32-SOP-525 32-TSOP1-0820F 32-SOP-525 32-TSOP1-0820F
K6X1008T2D-F	Industrial(-40~85°C)					
K6X1008T2D-Q	Automotive(-40~125°C)		70 ²⁾ /85ns	10μA		

1. This parameter is measured in the voltage range of 3.0V~3.6V with 30pF test load.

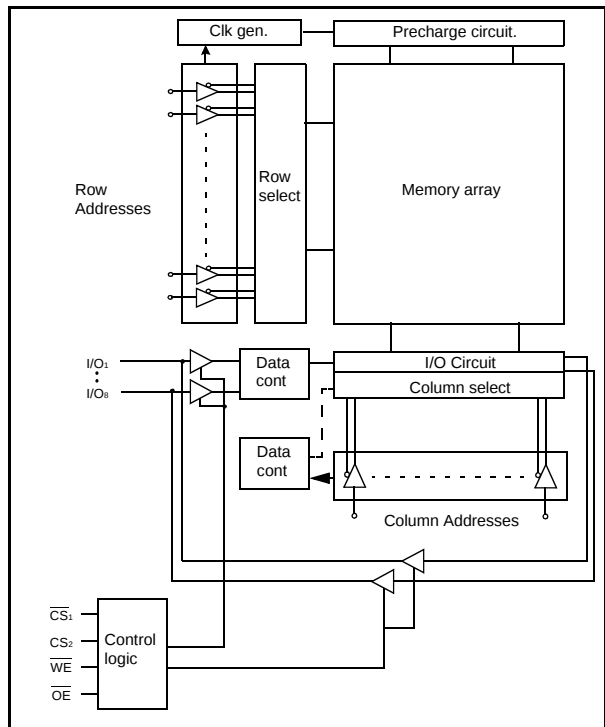
2. This parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function
A ₀ –A ₁₆	Address Inputs
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{CS}}_1, \text{CS}_2$	Chip Select Input
$\overline{\text{OE}}$	Output Enable Input
I/O ₁ –I/O ₈	Data Inputs/Outputs
V _{cc}	Power
V _{ss}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Products(0~70°C)		Industrial Products(-40~85°C)		Automotive Products(-40~125°C)	
Part Name	Function	Part Name	Function	Part Name	Function
K6X1008T2D-GB55 ¹⁾	32-SOP, 55ns, LL	K6X1008T2D-GF55 ¹⁾	32-SOP, 55ns, LL	K6X1008T2D-GQ70	32-SOP, 70ns, L
K6X1008T2D-GB70	32-SOP, 70ns, LL	K6X1008T2D-GF70	32-SOP, 70ns, LL	K6X1008T2D-GQ85	32-SOP, 85ns, L
K6X1008T2D-GB85	32-SOP, 85ns, LL	K6X1008T2D-GF85	32-SOP, 85ns, LL	K6X1008T2D-TQ70	32-TSOP-F, 70ns, L
K6X1008T2D-TB55 ^{1,2)}	32-TSOP-F, 55ns, LL	K6X1008T2D-TF55 ¹⁾	32-TSOP-F, 55ns, LL	K6X1008T2D-TQ85	32-TSOP-F, 85ns, L
K6X1008T2D-TB70	32-TSOP-F, 70ns, LL	K6X1008T2D-TF70	32-TSOP-F, 70ns, LL		
K6X1008T2D-TB85	32-TSOP-F, 85ns, LL	K6X1008T2D-TF85	32-TSOP-F, 85ns, LL		
K6X1008T2D-BB55 ^{1,2)}	32-SOP, 55ns, LL	K6X1008T2D-BF55 ^{1,2)}	32-SOP, 55ns, LL		
K6X1008T2D-BB70 ²⁾	32-SOP, 70ns, LL	K6X1008T2D-BF70 ²⁾	32-SOP, 70ns, LL		
K6X1008T2D-BB85 ²⁾	32-SOP, 85ns, LL	K6X1008T2D-BF85 ²⁾	32-SOP, 85ns, LL		
K6X1008T2D-PB55 ^{1,2)}	32-TSOP-F, 55ns, LL	K6X1008T2D-PF55 ^{1,2)}	32-TSOP-F, 55ns, LL		
K6X1008T2D-PB70 ²⁾	32-TSOP-F, 70ns, LL	K6X1008T2D-PF70 ²⁾	32-TSOP-F, 70ns, LL		
K6X1008T2D-PB85 ²⁾	32-TSOP-F, 85ns, LL	K6X1008T2D-PF85 ²⁾	32-TSOP-F, 85ns, LL		

1. Operating voltage range is 3.0V~3.6V

2. Lead Free Product

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.3V(Max. 3.9V)	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 3.9	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	K6X1008T2D-B
		-40 to 85	°C	K6X1008T2D-F
		-40 to 125	°C	K6X1008T2D-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.0/3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.6	V

Note:

- Commercial Product: T_A=0 to 70°C, Otherwise specified
Industrial Product: T_A=-40 to 85°C, Otherwise specified
Automotive Product: T_A=-40 to 125°C, Otherwise specified
- Overshoot: V_{CC}+3.0V in case of pulse width≤30ns.
- Undershoot: -3.0V in case of pulse width≤30ns.
- Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

- Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS1}$ =V _{IH} or CS ₂ =V _{IL} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL} , Read	-	-	2	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS1}$ ≤0.2V, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	3	mA	
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	-	20	mA	
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS1}$ =V _{IH} , CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	0.3	mA	
Standby Current(CMOS)	I _{SB1}	$\overline{CS1}$ ≥V _{CC} -0.2V, CS ₂ ≥V _{CC} -0.2V or CS ₂ ≤0.2V, Other inputs=0-V _{CC}	K6X1008T2D-B	-	-	6	μA
		K6X1008T2D-F	-	-	6	μA	
		K6X1008T2D-Q	-	-	10	μA	

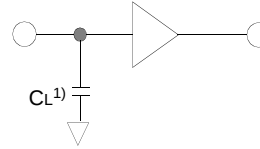
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (see right): $C_L = 100\text{pF} + 1\text{TTL}$
 $C_L = 30\text{pF} + 1\text{TTL}$ 

1. Including scope and jig capacitance

AC CHARACTERISTICS

(Vcc=2.7~3.6V, Commercial product: TA=0 to 70°C, Industrial product: TA=-40 to 85°C, Automotive product: TA=-40 to 125°C)

Parameter List		Symbol	Speed Bins						Units
			55ns ¹⁾		70ns		85ns		
			Min	Max	Min	Max	Min	Max	
Read	Read Cycle Time	t _{RC}	55	-	70	-	85	-	ns
	Address Access Time	t _{AA}	-	55	-	70	-	85	ns
	Chip Select to Output	t _{CO}	-	55	-	70	-	85	ns
	Output Enable to Valid Output	t _{OE}	-	25	-	35	-	40	ns
	Chip Select to Low-Z Output	t _{LZ}	10	-	10	-	10	-	ns
	Output Enable to Low-Z Output	t _{OLZ}	5	-	5	-	5	-	ns
	Chip Disable to High-Z Output	t _{HZ}	0	25	0	25	0	25	ns
	Output Disable to High-Z Output	t _{OHZ}	0	25	0	25	0	25	ns
	Output Hold from Address Change	t _{OH}	10	-	10	-	15	-	ns
Write	Write Cycle Time	t _{WC}	55	-	70	-	85	-	ns
	Chip Select to End of Write	t _{CW}	45	-	60	-	70	-	ns
	Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
	Address Valid to End of Write	t _{AW}	45	-	60	-	70	-	ns
	Write Pulse Width	t _{WP}	40	-	50	-	60	-	ns
	Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
	Write to Output High-Z	t _{WHZ}	0	25	0	25	0	30	ns
	Data to Write Time Overlap	t _{DW}	20	-	25	-	35	-	ns
	Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	ns
	End Write to Output Low-Z	t _{OW}	5	-	5	-	5	-	ns

1. Voltage range is 3.0V~3.6V for commercial and industrial product.

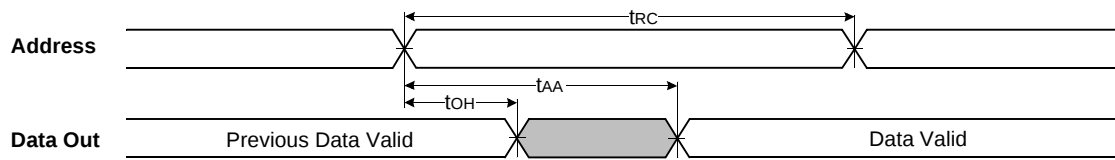
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	V _{DR}	$\overline{CS}_1 \geq V_{CC} - 0.2V^{1)}$	2.0	-	3.6	V
Data retention current	I _{DR}	$V_{CC} = 3.0V, \overline{CS}_1 \geq V_{CC} - 0.2V^{1)}$	K6X1008T2D-B	-	6	μA
			K6X1008T2D-F	-	6	μA
			K6X1008T2D-Q		10	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

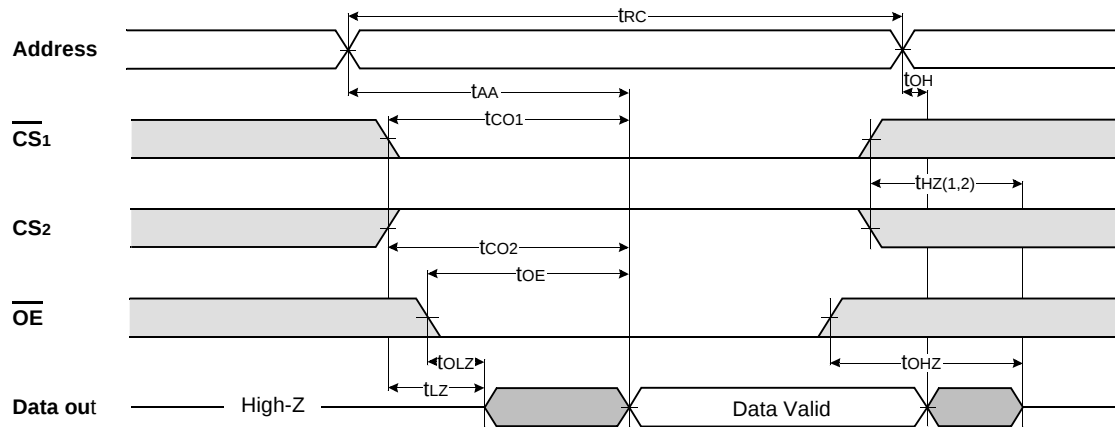
1. $\overline{CS}_1 \geq V_{CC} - 0.2V$, $\overline{CS}_2 \geq V_{CC} - 0.2V$, or $\overline{CS}_2 \leq 0.2V$

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$)



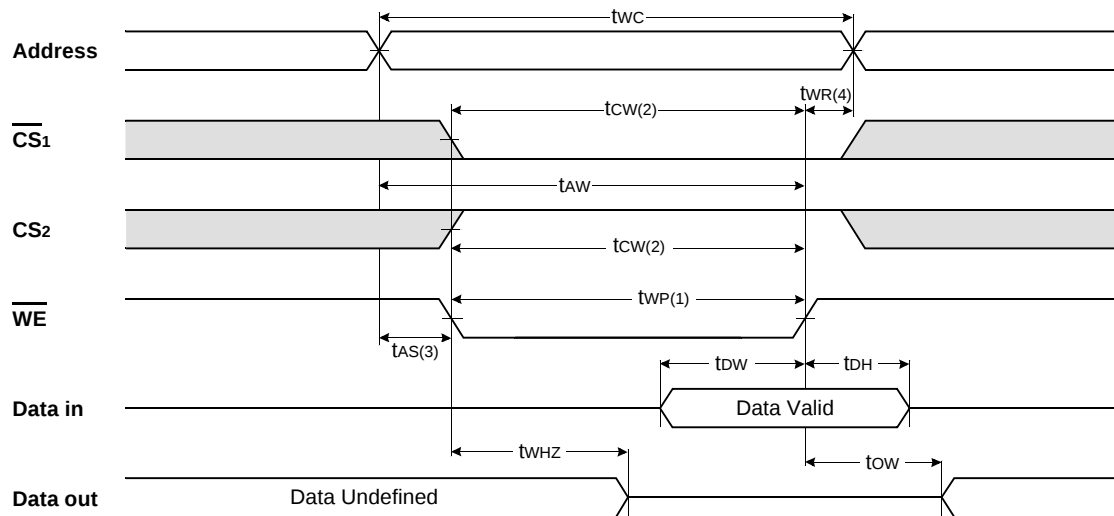
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



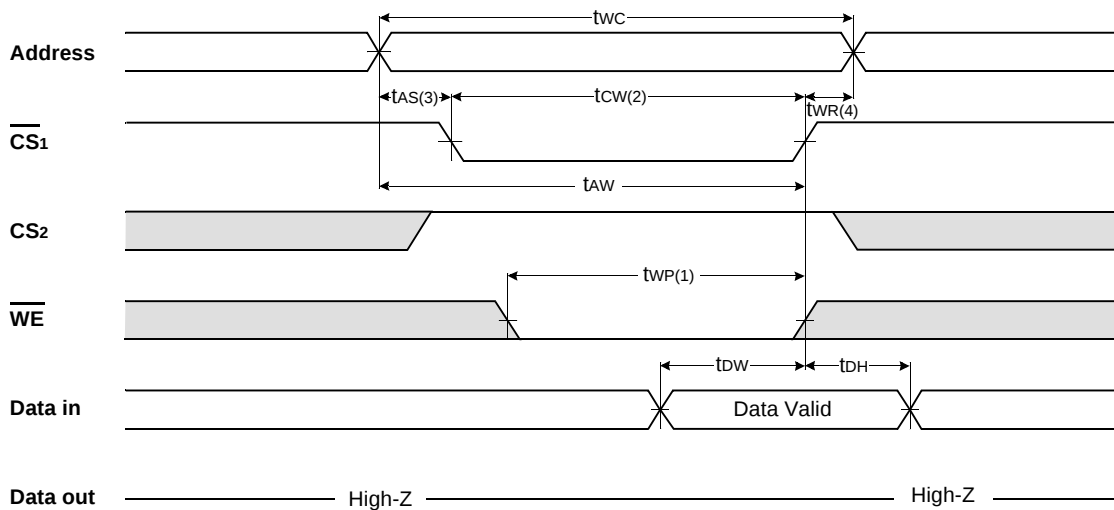
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

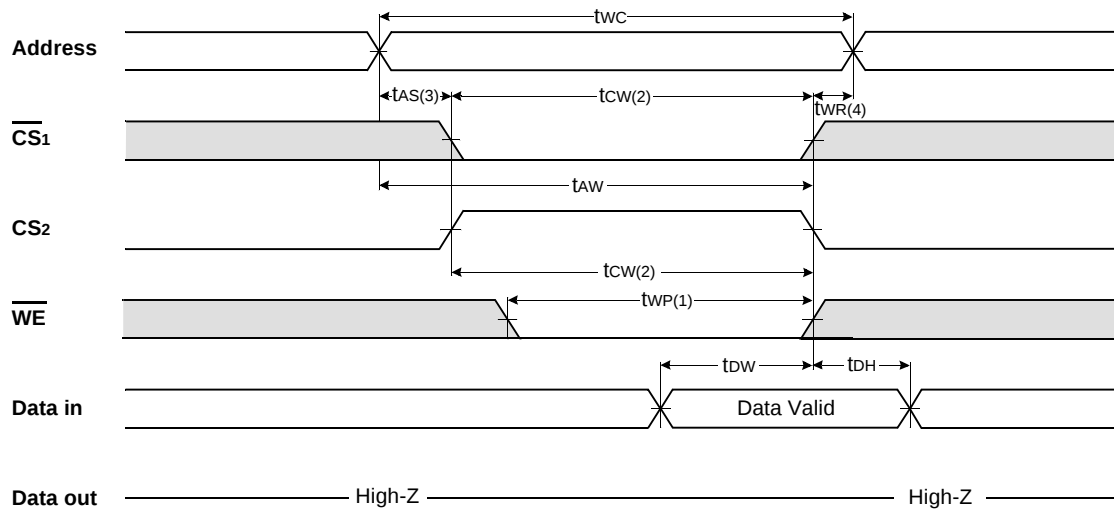
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS1}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

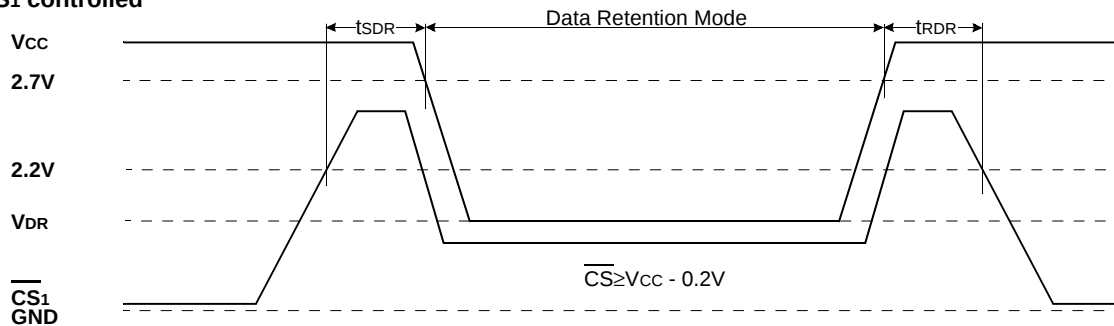


NOTES (WRITE CYCLE)

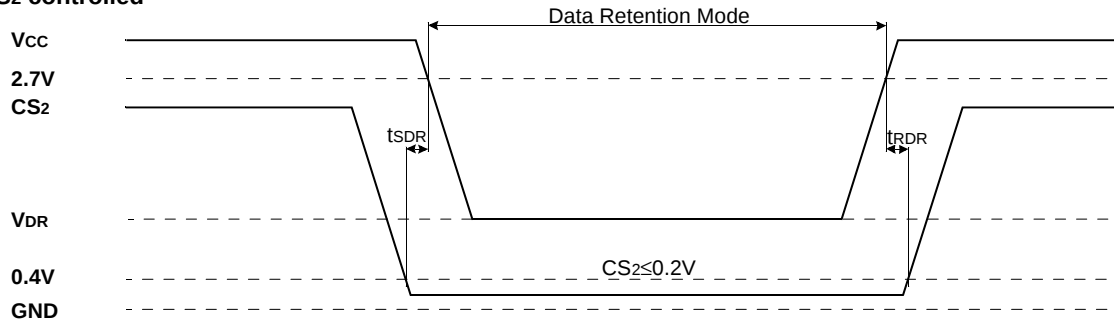
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS₂ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS₂ going high and WE going low: A write ends at the earliest transition among CS₁ going high, CS₂ going low and WE going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the CS₁ going low or CS₂ going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high t_{WR2} applied in case a write ends as CS₂ going to low.

DATA RETENTION WAVE FORM

CS₁ controlled



CS₂ controlled



CMOS SRAM

Units: millimeters(inches)

The drawing illustrates the mechanical specifications of a 32-pin Quad Flat Pack (QFP) package. It includes three views: a top view, a side view, and a detail view of the lead profile.

Top View Dimensions:

- Pin 1 to Pin 16 distance: 20.87 ± 0.30 mm, 0.822 MAX
- Pin 17 to Pin 32 distance: 20.47 ± 0.20 mm, 0.806 ± 0.008
- Pin 1 to Pin 17 distance: 14.12 ± 0.30 mm, 0.556 ± 0.012
- Pin 16 to Pin 32 distance: 11.43 ± 0.20 mm, 0.450 ± 0.008
- Pin 1 to Pin 16 distance: 2.74 ± 0.20 mm, 0.108 ± 0.008
- Pin 17 to Pin 32 distance: 3.00 ± 0.118 MAX
- Pin 1 to Pin 16 distance: 0.41 ± 0.100 mm, -0.050
- Pin 17 to Pin 32 distance: 0.16 ± 0.004 mm, -0.002
- Pin 1 to Pin 16 distance: 1.27 ± 0.050 mm
- Pin 17 to Pin 32 distance: 0.05 ± 0.002 MIN
- Pin 1 to Pin 16 distance: 0.71 ± 0.028 mm

Side View Dimensions:

- Package height: 13.34 ± 0.525 mm
- Lead height: 0.20 ± 0.10 mm, -0.05
- Lead thickness: 0.008 ± 0.002 mm
- Lead angle: 0.80 ± 0.20 mm, 0.031 ± 0.008
- Lead angle: $0-8^\circ$

Detail View Dimensions:

- Lead thickness: 0.10 MAX
- Lead thickness: 0.004 MAX

Technical drawing of a 16-pin D-sub connector. The drawing includes two views: a top view and a side view.

Top View Dimensions:

- Overall width: 20.00 ± 0.20 inches (508.0 ± 5.1 mm)
- Pin pitch (center-to-center): 0.008 ± 0.002 inches (0.203 ± 0.051 mm)
- Pin diameter: 0.020 ± 0.005 inches (0.508 ± 0.127 mm)
- Pin #1 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the left edge.
- Pin #16 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the left edge.
- Pin #32 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the right edge.
- Pin #17 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the right edge.
- Pin #1 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the left edge.
- Pin #16 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the left edge.
- Pin #32 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the right edge.
- Pin #17 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the right edge.

Side View Dimensions:

- Overall height: 8.40 ± 0.31 inches (213.3 ± 7.9 mm)
- Pin height: 0.315 ± 0.010 inches (8.0 ± 0.25 mm)
- Pin diameter: 0.020 ± 0.005 inches (0.508 ± 0.127 mm)
- Pin #1 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the left edge.
- Pin #16 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the left edge.
- Pin #32 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the right edge.
- Pin #17 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the right edge.
- Pin #1 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the left edge.
- Pin #16 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the left edge.
- Pin #32 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the right edge.
- Pin #17 location: 0.008 ± 0.002 inches (0.203 ± 0.051 mm) from the right edge.

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