Tape Carrier Package 12

12.1 Introduction To The Package Technology

As semiconductor devices become more complex they are being introduced into products that cover the spectrum of the marketplace. Portability of computing and information management is driving the reduction in size from desktop to laptop to notebook to palm top sized products. These products, require lightweight small footprint integrated packaging.

The Tape Carrier Package (TCP) format is one way to meet the small outline and high leadcount interconnection needs of high performance microprocessors. The TCP has been designed to offer reduced pitch, thin package profiles, smaller footprint on the printed circuit board, without compromising performance. Intel continues to provide packaging solutions which meet rigorous criteria for quality and performance. The Tape Carrier Package is no exception. Key package features include surface mount technology design, lead pitch of 0.25 mm, 48 mm tape format, polyimide-up for pick and place, and slide carrier handling. Shipped flat in slide carriers, the leads are designed to be formed into a “gull-wing” configuration and reflowed onto the PCB by one of several methods. Intel has done extensive optimization of the hot bar reflow process and suggestions for that process are included in this chapter. Satisfactory placement and rework capability has been demonstrated by industry sources using the hot gas reflow process. Industry data also exists which demonstrates process feasibility for laser reflow.

The TCP family has been characterized for thermal, electrical, and mechanical performance. Component and system level thermal testing has shown the TCP package to be capable of meeting system level thermal design needs. Additional potential board level enhancements have been identified and characterized to provide the most flexible design choices. A full suite of component and board level stress testing has been completed to ensure that the component meets Intel’s reliability targets. Evaluations of solder joints by stress testing, lead stiffness studies, and finite element modeling have demonstrated that the mounted component will meet field use conditions and lifetimes. The TCP package is capable of meeting a wide variety of design and use applications. Table 12-1 provides an overview of TCP package attributes.

Table 12-1. Plastic Package Attributes

Tape Carrier Package (TCP) Attributes	
Lead Count	320
Sq/Rect.	S
Lead Pitch (mm)	0.25
Package Thickness (mm)	0.75
Weight (gm)	0.5
Max. Footprint (mm)	24.0
Shipping Media: Tubes	 X
Comments/Footnotes	TCP components are shipped flat in slide carriers to protect the leads. The carriers are shipped in polyethylene sleeves which hold up to 50 carriers.

12.2 Package Geometry And Materials

12.2.1 Package Materials

The TCP component consists of the device interconnected to 3 layer (carrier film, adhesive, and metal) Tape Automated Bonding (TAB) tape. The tape carrier film is polyimide and an advanced epoxy-based adhesive system is used. The interconnects are copper. The tape metallization, including the Outer Lead Bond (OLB) area of the interconnections, is gold plated over a nickel flash. The silicon chip and Inner Lead Bond (ILB) area is encapsulated with a high temperature thermoset polymer coating. The backside of the chip is left uncoated for thermal connection to the printed circuit board (PCB). While lower lead count TAB devices are often shipped in tape and reel format, Intel has chosen to ship components as individual devices. The individual units are shipped in high temperature plastic slide carriers packed in coin stack tubes.

12.2.2 Package Outline Drawings

Figure 12-1 through Figure 12-6 show the outline drawings for a 24 mm TCP component and its slide carrier. The TCP package meets JEDEC outline specification UO-018 for tape format, lead length, and test pads. The carrier conforms to JEDEC criteria for handling media. One TCP component debussed, singulated, and in the carrier is viewed from the topside of the carrier and bottomside of the tape in Figure 12-1. This is the test pad side.

The opposite side view—topside of tape, topside of die, and bottomside of the carrier is seen in Figure 12-2.

The tape is in 48 mm format and includes test pads outboard of the OLB window (see Figure 12-3). Pads are 0.5 mm x 0.65mm on 0.40 mm pitch on two rows.

A cross section view of the TCP package is illustrated in Figure 12-4. The “five-sided” encapsulant covers the top surface of the device, the sides of the device, and the ILB area to the polyimide carrier ring. The tape bow or offset across the polyimide carrier film is product specific. Contact Intel Corporation for additional information. After forming and mounting to the PCB, the total height of the component above the PCB is less than 0.75 mm.

Details of the tooling holes can be seen in Figure 12-5. Intel uses the tooling holes shown in the upper left and lower right of Figure 12-1 for alignment during processing at Intel and should not be used during board assembly. The other two tooling holes have been left pristine for use during board assembly.

The OLB window has been designed to facilitate excise and form. The polyimide carrier film can be cut and a narrow strip left in place at the outer edge of the OLB area to act as a “Keeper Bar” to maintain lead coplanarity, and spacing, if so desired. The detail of the OLB Window area is shown in Figure 12-6.

Figure 12-1. One TCP Site in Carrier (Bottom View of Die)

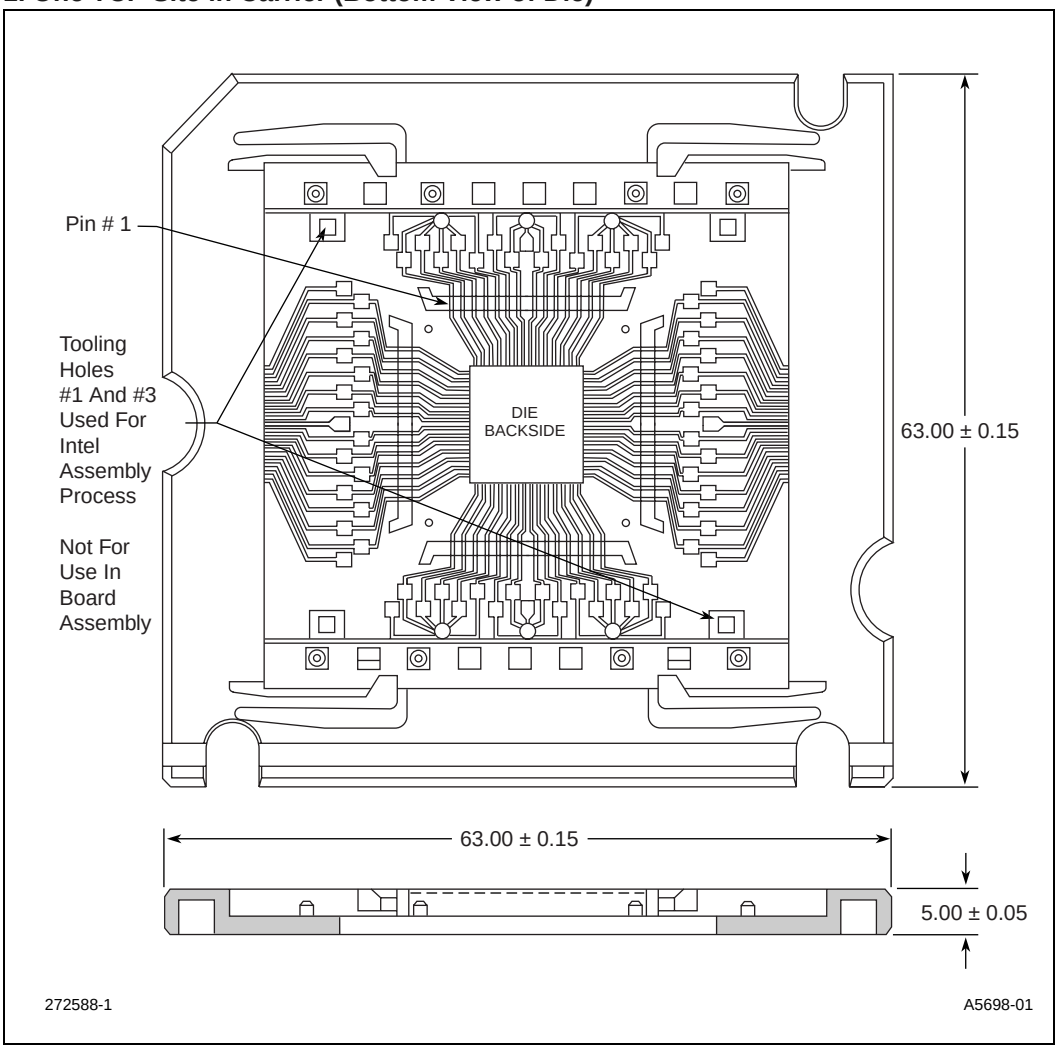


Figure 12-2. One TCP Site in Carrier (Top View of Die)

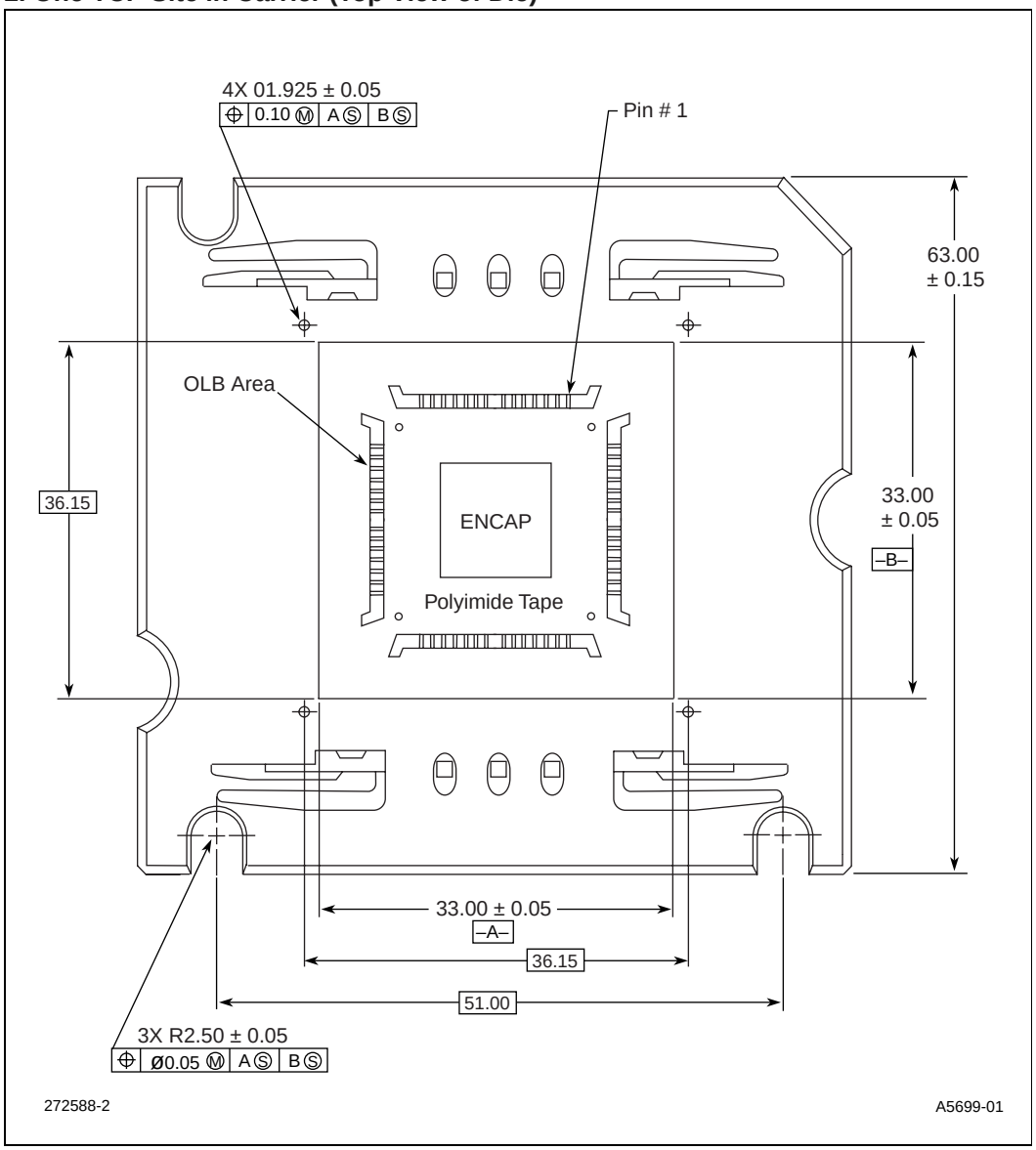


Figure 12-3. One TCP Site (Bottom View)

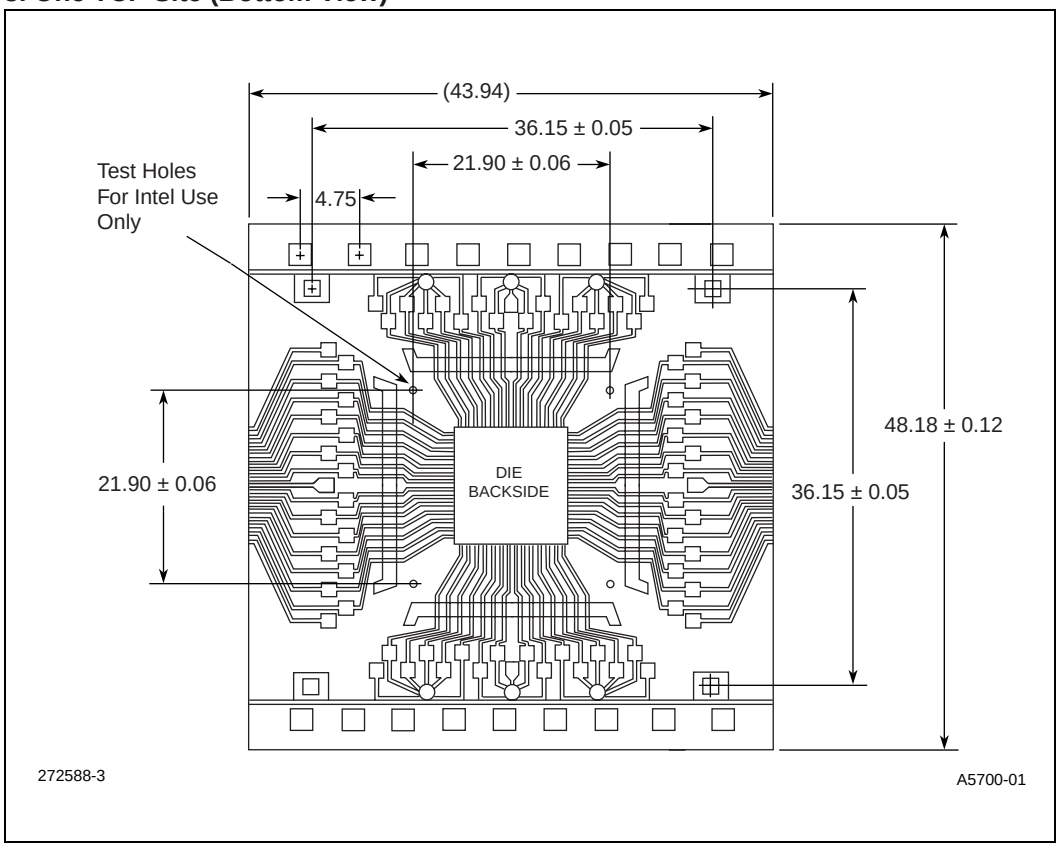


Figure 12-4. One TCP Site (Cross-Section Detail)

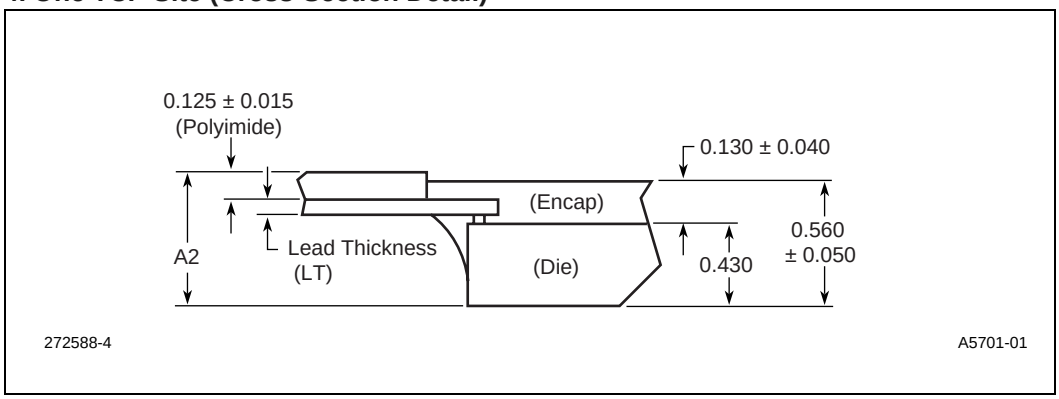


Figure 12-5. One TCP Site (Top View)

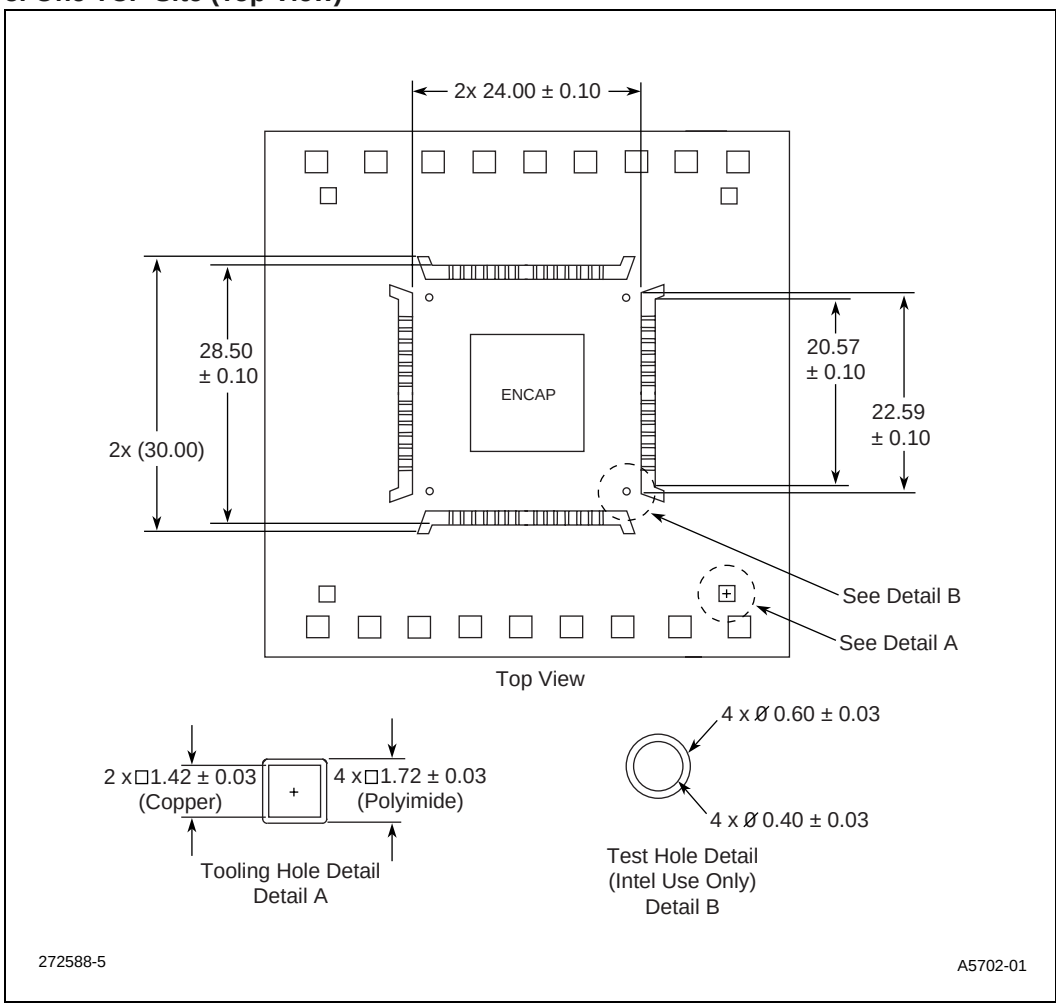


Figure 12-6. OLB Window Detail

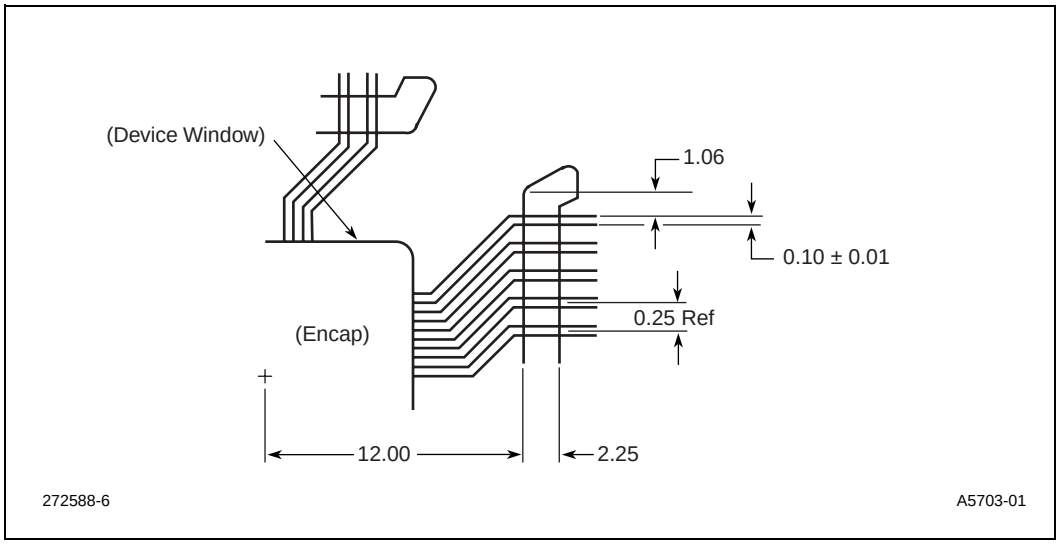


Table 12-2. TCP Key Dimensions

Symbol	Description	Dimension (mm)
A_2	Package Height	Varies by Product. See Product Data Sheet
b	Outer Lead Width	0.10 +/- 0.01
D_1, E_1	Package Body Size	24.0 +/- 0.1
DL, EL	Die/Encap Length	Varies by Product. See Product Data Sheet
DW, EL	Die/Encap Width	Varies by Product. See Product Data Sheet
e_1	Outer Lead Pitch	0.25 nom
L	Site Length	(43.94) ref.
N	Lead count	320 leads
W	Tape Width	48.18 +/- 0.12

12.2.3 Key Aspects of the Package Family

Table 12-3. Mounted TCP Package Dimensions

Symbol	Description	Dimension
A	Package Height	0.75 max.
D, E	Terminal Dimension	29.5 nom.
WT	Package Weight	0.5 g max.

NOTES:
1. Dimensions are in millimeters unless otherwise noted.
2. Dimensions in parentheses are for reference only.
3. Package terminal dimension (lead tip-to-lead tip) assumes the use of keeper bar.

12.2.3.1 Package Weight

The 320 lead 0.25 mm TCP component weighs a maximum of 0.5 grams for the 24 mm body size component. In comparison, a 296 lead multilayer PQFP package weighs 9.45 grams. This makes the TCP package family extremely attractive for weight constrained applications.

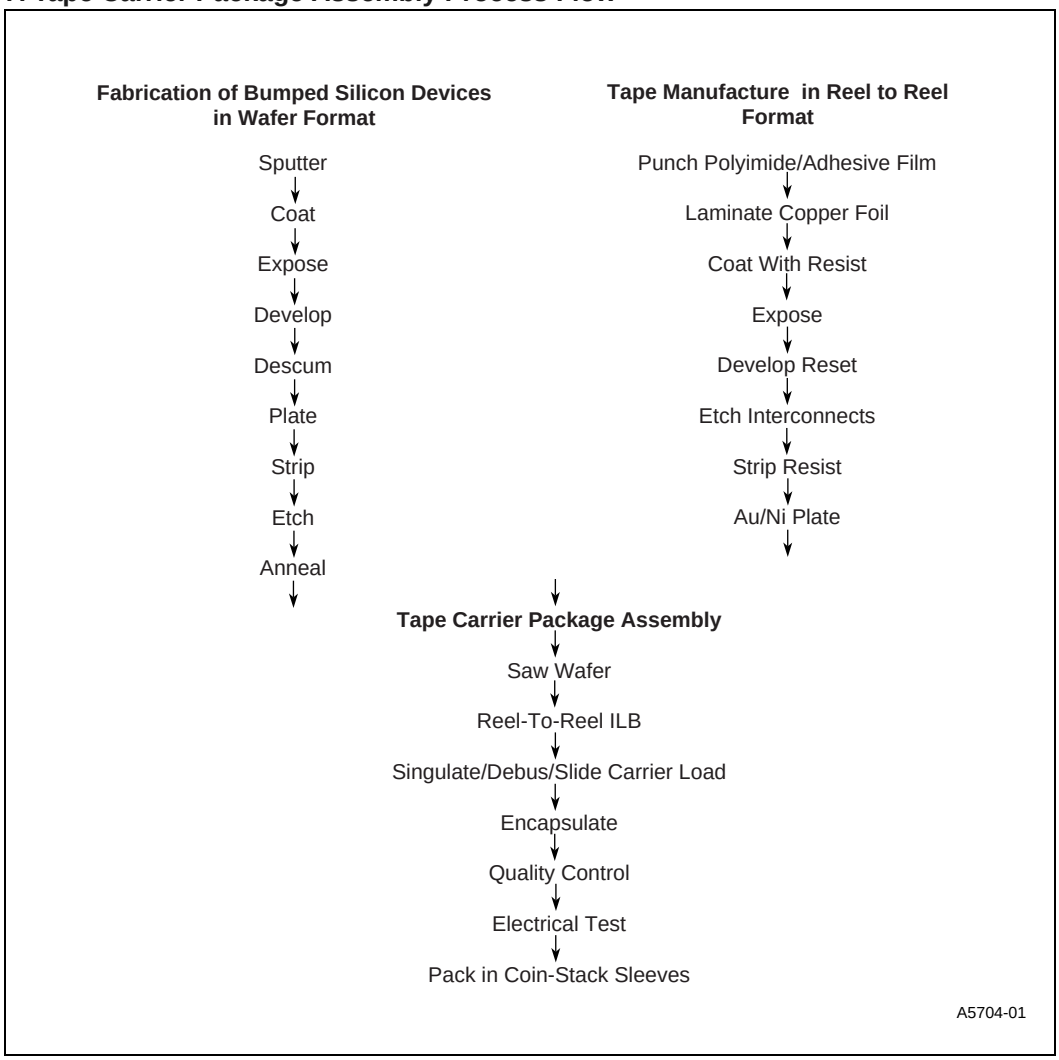
12.2.3.2 Use Applications

The TCP package is designed for use with applications where height, footprint, and weight are tightly controlled. Because of the tight pitch of the component, 0.25 mm, the recommended board assembly process for TCP is localized reflow, either by hot bar, hot gas, or laser. Mass reflow processes such as infrared, convection, or vapor phase reflow processes may be difficult to control at these pitches. Intel has developed a suggested process for localized reflow, specifically by hot bar thermode. Process envelope suggestions for hot gas reflow are available and have been determined through direct external development efforts between Intel and industry sources. Solder finish on the land pattern on the PCB can be used in lieu of screened or syringe dispensed solder paste.

12.2.3.3 TCP Component Assembly Process

The basic assembly flow used to form TCP packages is shown in Figure 12-7. There are several methods of forming TAB-based packaging technologies. To achieve the highest reliability joint between the silicon and the TAB tape, Intel creates gold “bumps” on the wafer surface at the I/O pads. This bumping process is a wafer fabrication process. Barrier metals are sputtered onto the active surface of the wafer. Photoresist is applied, patterned and exposed and then developed to open areas for plating up the “bump”. The resist is stripped from the surface, the excess sputter metal film is removed by etching and the gold bumps are annealed to optimize the metallurgical properties of the bump for subsequent bonding processes.

Figure 12-7. Tape Carrier Package Assembly Process Flow



In parallel with the bumping process, TAB tape sites are manufactured in reel-to-reel format. Polyimide carrier film with an adhesive in reel form, is punched to create the Inner Lead Bond (ILB) and Outer Lead Bond (OLB) windows and tooling holes for subsequent processing steps. Copper foil is laminated onto the polyimide and cured. Again, a photolithographic technique is used to create the specific pattern of metal leads and test pads. Once the tape metal pattern has been created, the exposed copper metal is plated with a Ni barrier metal and Au outer plating. Au outer plating is used for the entire tape interconnect path; both ILB and OLB lead areas are plated with gold. Intel has done extensive testing of the solder joint reliability of nickel-gold plated leads.

The silicon and the TAB tape are brought together at the TCP package process. After the wafers are sawn into individual devices, the TAB tape sites are matched to the device. During Inner Lead Bonding, the ILB area of the tape is aligned to the bumps on the device. They are brought into contact and a gold-to-gold weld is formed. This process establishes the silicon to PCB interconnection path. After ILB, the component sites are singulated from the reel, the tape plating bars are “debussed” from the tape, and the individual component sites are loaded into ESD protective slide carriers (see Figure 12-1 and Figure 12-2). Once in slide carriers, the devices are encapsulated in a high temperature polymer coating. The coating covers the top and sides of the silicon, the bumps, and the ILB area to the polyimide carrier ring. Complete coverage of the ILB area provides mechanical support to the ultra-fine pitch leads, protecting them from handling

damage and thermomechanical stress induced damage. The thermoset polymer is cured to ensure a high enough cross-link density to fully protect the device from environmental degradation. After quality control checks and electrical test, the components are ink marked, packed, and shipped. The components are shipped flat in slide carriers. This ensures that the outer lead area is undamaged at the time of board mount processing.

12.3 Shipping Media

The TCP components are shipped flat in slide carriers to protect the component leads. The tape sites are already debussed when in the slide carrier, therefore, the carrier is made of an intrinsically dissipative material for ESD protection. The carriers are molded of high temperature polymer and are suitable for hot and cold electrical test. The carriers meet JEDEC Outline CO-018 as shown in Figure 12-2. The carriers are shipped in polyethylene sleeves (also called coin stack tubes) which hold up to 50 carriers. The shipping tubes meet JEDEC outline CO-017 as shown in Figure 12-8. Figure 12-9 shows the detail of the tube in cross section.

For recycling information, contact Micro Plastics, Phoenix, Arizona.

Ship to: Micro Plastics 3420 West Whitton Ave. Phoenix, AZ 85017 Phone: (602) 278-4545 Fax: (602) 278-4477	Contact Micro Plastics for specific Intel shipping instructions for your area. **Bill Shipping Costs to:** Intel Corp. C/O NWTA PO Box 4567 Federal Way, WA 98063

Figure 12-8. Coin Stack Tube (Side & End Views)

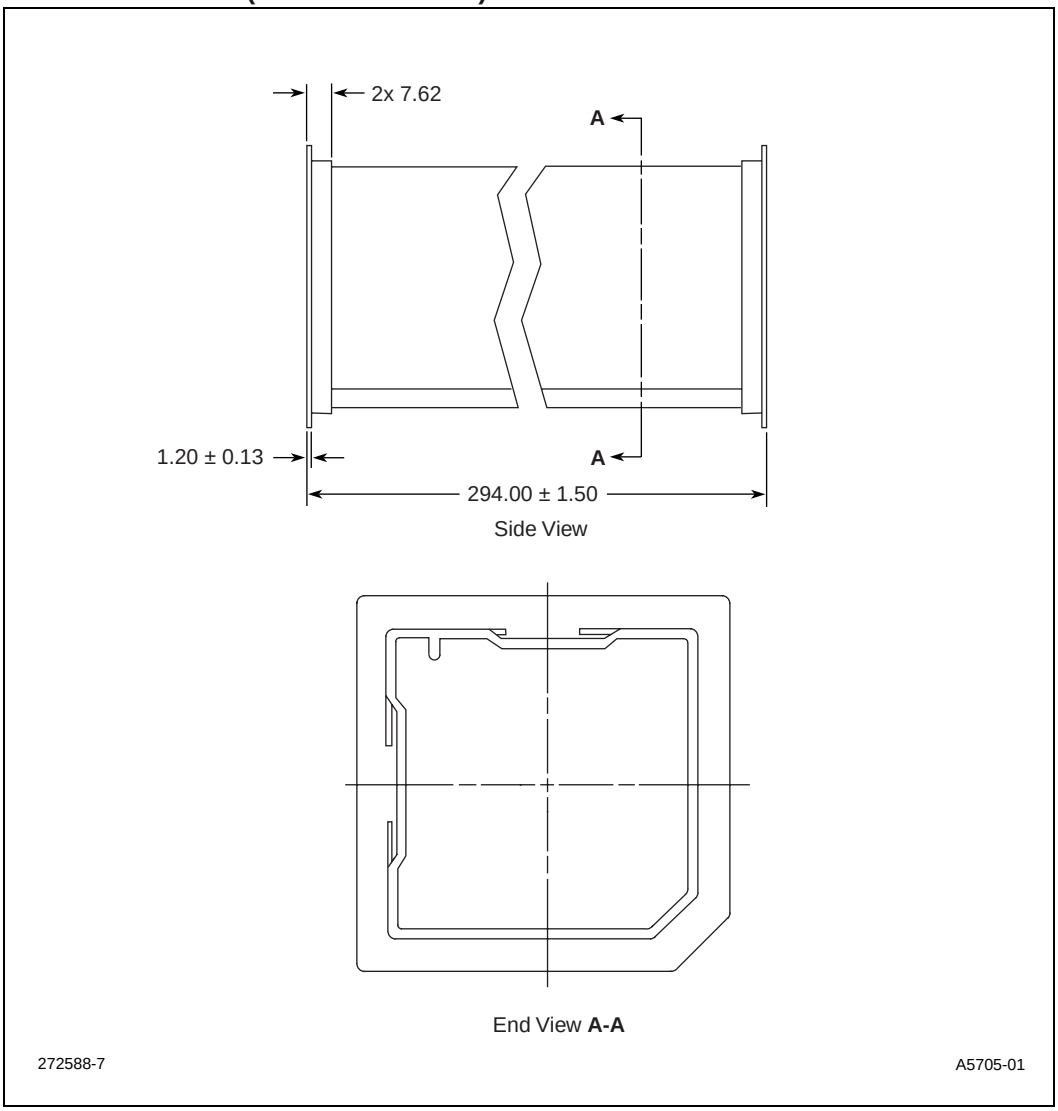
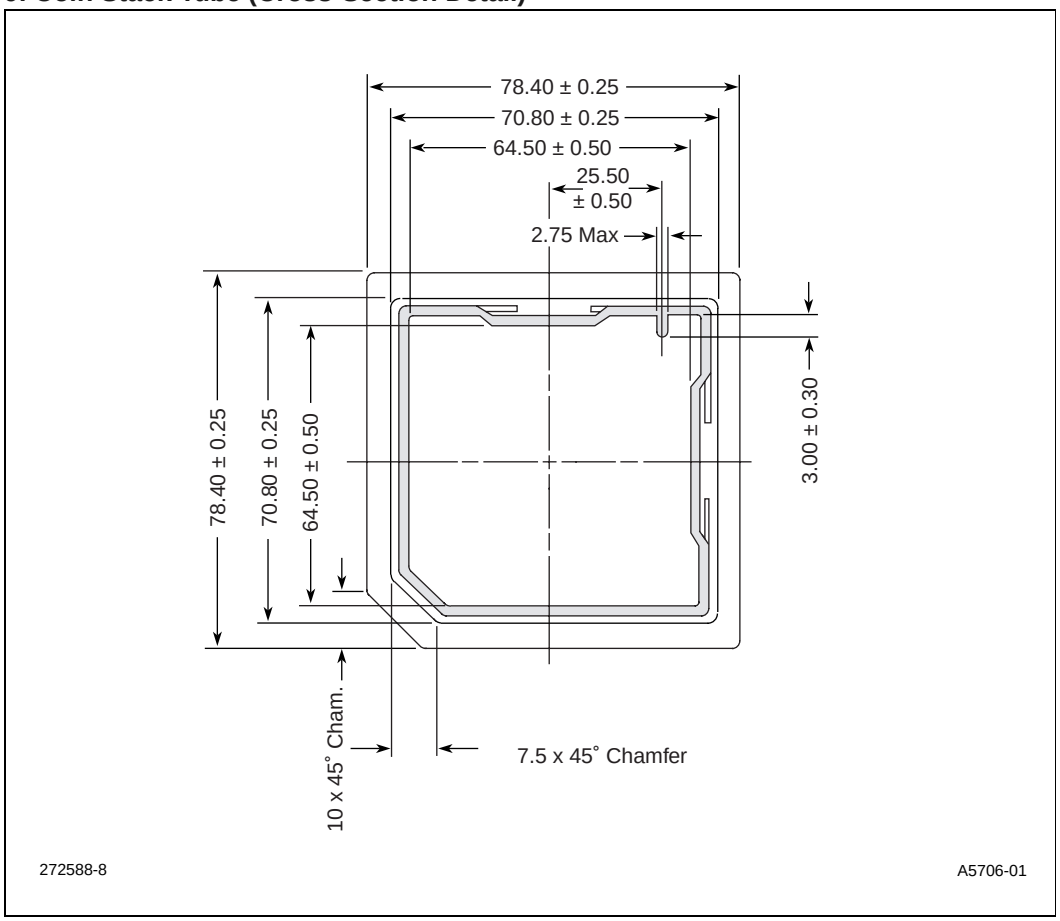


Figure 12-9. Coin Stack Tube (Cross-Section Detail)



12.4 Handling: Preconditioning and Moisture Sensitivity

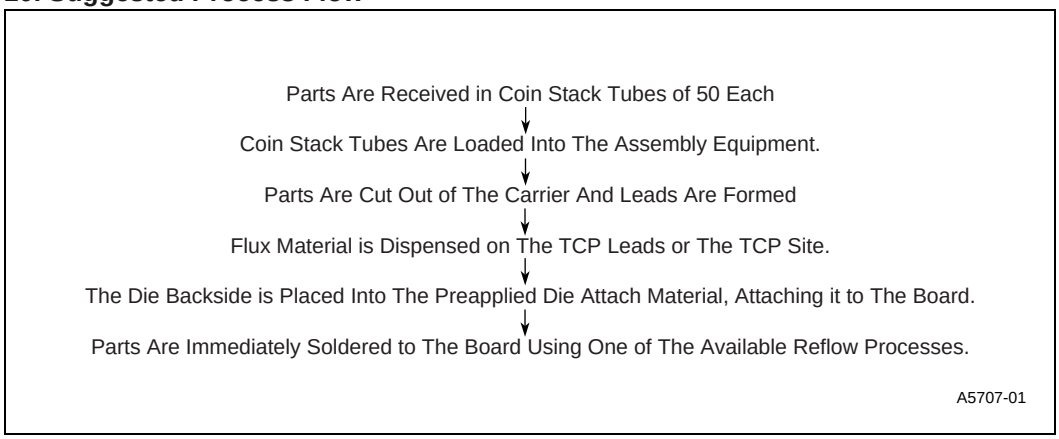
INTEL DOES NOT RECOMMEND SUBJECTING THE TCP PACKAGE TO ANY TYPE OF MASS REFLOW PROCESS. THE PACKAGE WAS NOT CHARACTERIZED FOR MASS REFLOW PROCESSES.

At this time Intel suggests hot bar and hot gas reflow processes that do not subject the component body to reflow temperatures. There is no jeopardy with moisture sensitivity when using these localized reflow processes. The TCP package has met all reliability requirements after exposure to the hot bar mounting process. Therefore, the TCP components are shipped without desiccant packing materials. There are no “out of bag” shelf life restrictions prior to component mount. For additional information contact your Intel representative.

12.4.1 Suggested Process Flow

It is suggested that the TCP component be mounted using either a hot bar, hot gas, or laser reflow process after all other board components have been completed, including cleaning. The TCP component mount can be accomplished in a number of different ways. The process that Intel has the most direct experience with is illustrated in Figure 12-10. Note that lead form and hot bar reflow soldering are mounting options.

Figure 12-10. Suggested Process Flow



12.4.2 Land Pattern Design

The TCP land pattern varies depending on specific process conditions and lead form dimensions. Some general guidelines and a land pattern developed for Intel's internal hot bar process follow. Note that the TCP is a metric package and that the land pattern should be dimensioned in metric. Converting dimensions to the English system can result in gross mis-match of the package to the lands.

12.4.3 Solder Lands

Figure 12-17 shows the suggested land pattern for a 0.25 mm Tape Carrier Package. All package dimensions are "as finished" and not necessarily the designed dimensions. For the 0.25 mm lead pitch component land pattern, the lands should be 0.125 mm $\pm$ 0.025 mm in width with a land length = 2.5mm. A minimum land length of 2.25mm is suggested to avoid potential solder joint reliability problems. A minimum spacing between land pads of 0.10 mm should be maintained, measured at the copper/laminate interface. See Figure 12-11.

The land length should be long enough to allow a solder fillet to form at the toe and heel of the lead. To prevent a starved joint or excess gold concentration in the solder joint it is suggested that the total solder volume of the land and the resultant solder joint be greater than 0.004 mm^3. The land pattern terminal dimension is defined as the distance from outer land edge to land edge as illustrated in a sample land pattern in Figure 12-13. This dimension is based on the lead toe location from center, the incremental land length allowed for solder fillet formation, and the tolerances. Generally, this is approximately 1.0 mm longer than the toe-to-toe dimension. Additionally, it is suggested that trace connection to lands be "necked down" by 0.013mm to help eliminate "solder thieving" during reflow.

Figure 12-11. Land Width Specification

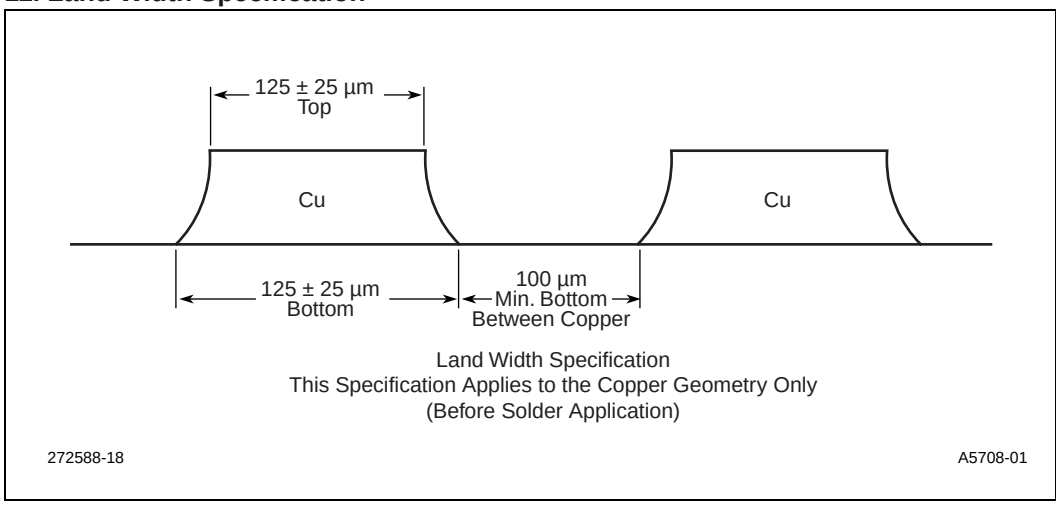


Figure 12-12. Solder Thickness Specification

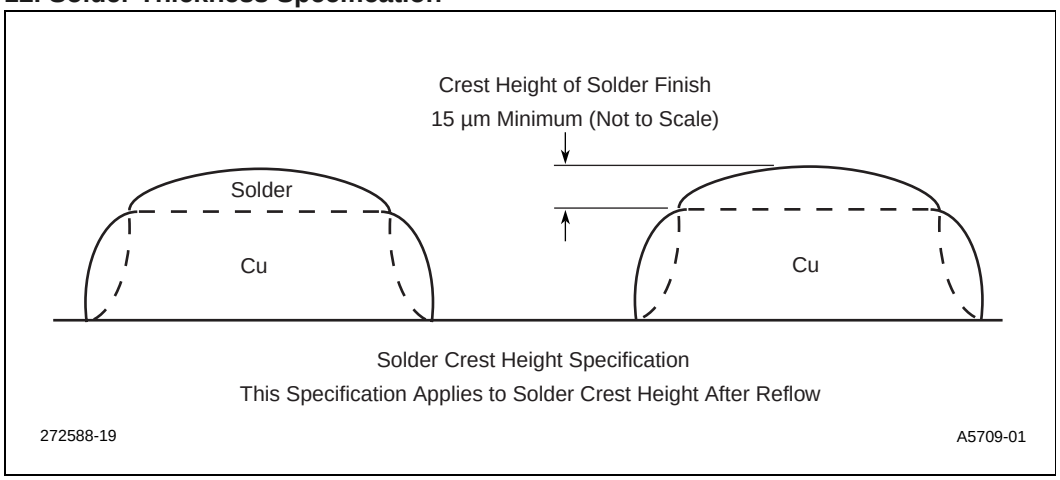
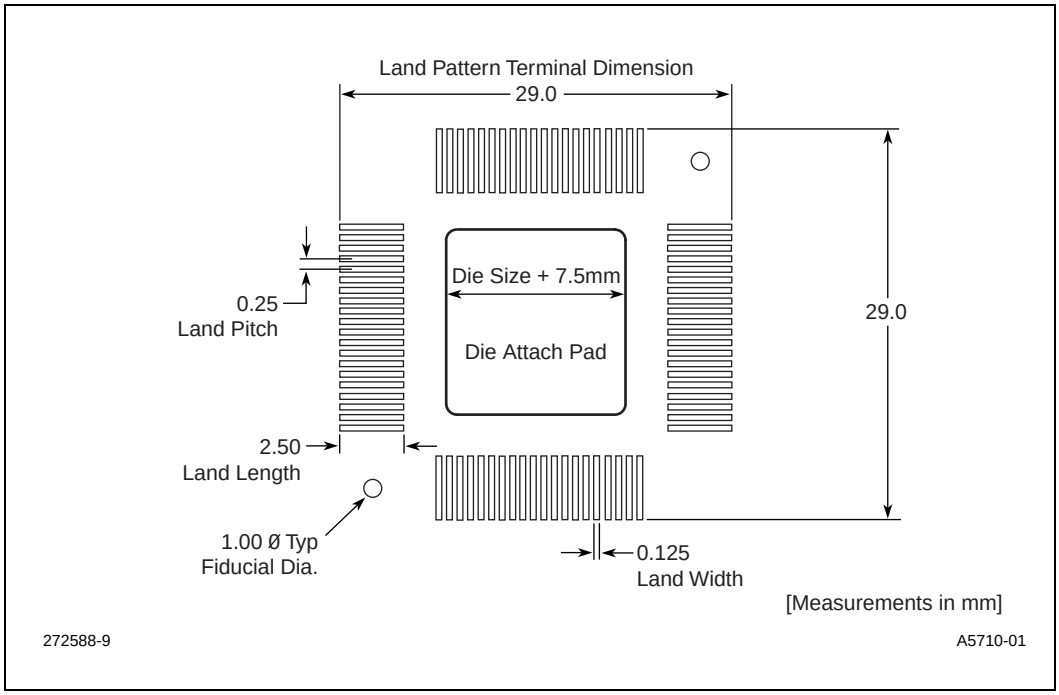


Figure 12-13. Sample Land Pattern for a TCP with 24 mm Body Size for Use with a Hot Bar Reflow Process



12.4.4 Land Pattern Solder Finish

The TCP component site should be finished with eutectic tin-lead solder (63/37) to a thickness sufficient to form acceptable fillets (reference IPC-SM-780). The thickness requirement may vary with reflow process, but in general the minimum solder thickness for reliable joint formation is 15 micrometers as measured at the crest of the reflowed land. Figure 12-12 shows the location of the crest height measurement. See Section 12-7 for a discussion of solder joint reliability as a function of component OLB metallurgy and solder finish on the land. See the section on Mechanical Behavior for a discussion of solder joint reliability as a function of component OLB metallurgy and solder finish on the land.

12.4.5 Die Attach Pad

Because Intel's TCP components require backside thermal contact, it is necessary to provide a die attach pad metallization area. The die attach pad should be 7.5 $\pm$ 0.025 mm larger than the device in both X and Y directions to allow for placement tolerance and the formation a die attach fillet. The Die Attach Pad area must be metallized to obtain optimal thermal contact; either SnPb or Au metallization is acceptable.

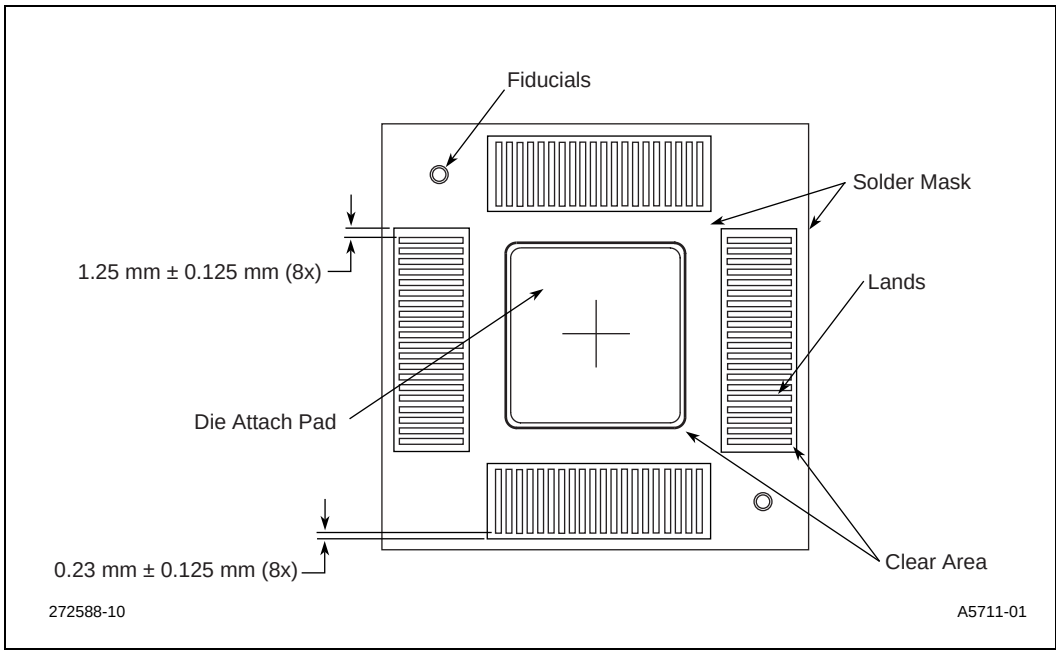
12.4.6 Solder Mask

If solder mask is used on the board, then there should be adequate pull-back around the lands so as not to restrict the movement of the thermode or hot gas head in the Z-direction when placing and reflowing the TCP component. In general, if the design permits (for example, if this area is not used for routing), then it is suggested that a square "donut" of solder mask clear area be left around the TCP lands and fiducials. A sample solder mask clear area is illustrated in Figure 12-14.

12.4.7 Fiducials

The ultra fine pitch of these components may require that pattern recognition systems be used to accurately locate the lead and the land. To facilitate the pattern recognition algorithms it is recommended that PCB lands have fiducials associated with each TCP site. Each equipment type will have specific requirements for fiducial configurations. For KME equipment, round fiducials of 0.3mm in diameter located on adjacent corners (same side of the site) are suggested. For Universal Instruments or Zevatech equipment, Surface Mount Equipment Manufacturers Association (SMEMA) Std. 3.1 compatible fiducials 1.0 mm (39 mil) in diameter should be placed at all 4 corners of the TCP site; at least 2 fiducials in opposite corners are required. Other equipment manufacturers may have other requirements. Please verify fiducial design requirements with the equipment supplier before finalizing board designs. A possible fiducial position is shown in Figure 12-13. They should be located within the terminal dimensions of the land pattern and equally spaced from the centroid of the site. The contrast of these fiducials is critical to providing adequate edge contrast. Therefore, the finish and finish morphology should not change during reflow processes. For example, Au or Sn are acceptable. Solder mask should be pulled back from the edge of the fiducial by 20 mils (SMEMA 3.1) to maximize Pattern Recognition System effectiveness. Figure 12-14 shows the solder mask pull back and the fiducials for a TCP land pattern site.

Figure 12-14. Solder Mask Clear Area



12.4.8 PCB Vias Design Rules

12.4.8.1 Interconnect Vias

Vias and connected pads placed too close to the TCP lands can sink heat away from the TCP component lands during localized reflow, resulting in longer process times. Additionally, if via pads or lands (connected or unconnected) are too close to the TCP lands, they can draw solder away from the TCP lead land resulting in a solder-poor joint. For this reason, it is suggested that vias be placed no closer than 0.65 mm (25 mils) from the edge of the lands.

12.4.8.2 Thermal Vias

Thermal vias in the die attach pad area can enhance heat transfer away from the die into and through the PCB where further heat spreading and transfer can be achieved. When designing the thermal via pattern, the tradeoffs between low thermal resistance and manufacturability (cost) must be considered. A full grid array provides the best heat transfer. Large, unfilled vias may cost less at the board fabrication level, but may also require special processing at board assembly to keep the die attach material from seeping through the holes. Either 100 percent open vias or 100 percent filled vias are best for manufacturability because they provide a consistent surface for the die attach medium. Thermal via design issues are discussed in the Package Performance section.

Traces can be routed on the signal layers between the thermal vias, however, this area of the board can get to near 100° C. This should be considered before routing critical traces through this area.

12.4.8.3 Lead Guard Hole Size

For those who want to protect the device after mounting, Intel has developed a light weight, low profile and low cost TCP cover called a Lead Guard. This device is attached with snap fit pins which can be inserted into holes in the PCB. Hole size and location are shown in Figure 12-15. See the description of a sample lead guard design in the Mechanical Behavior section.

12.4.9 Keep-out Areas

Since TCP component assembly is the last process in the board assembly flow, certain “keep out” areas-areas that must remain clear of other components-are defined to allow for placement of the TCP component. A clear area must be left on the side opposite the TCP site to allow for the board to be supported from the bottom side during the localized reflow (hot bar, hot gas) process. The specific pedestal (under-board support) design will dictate the exact dimensions of the keep out area, but in general, a square area directly site-opposite the TCP should remain clear to allow for TCP manufacturing and thermal enhancements. Additionally, sufficient clear area should remain around the TCP site to allow the reflow head to place the TCP component without interference in the Z-direction.

Figure 12-15. Hole Size and Location Illustration for a 24 mm Body Size TCP Lead Guard

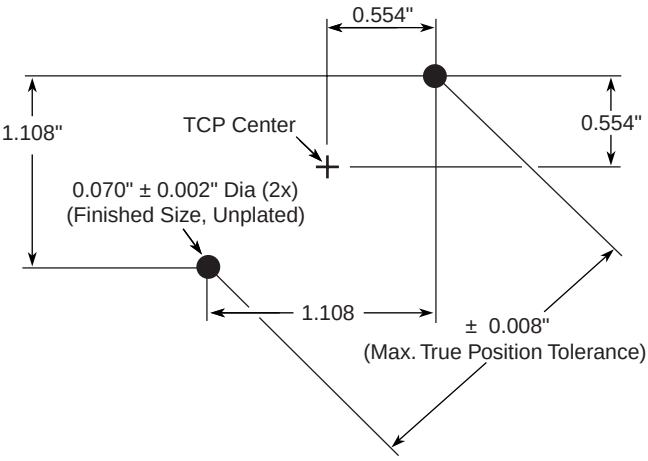


Table 12-4. Suggested Land Pattern Parameters

Land Pitch	0.25 mm
Land Width	0.125 (0.025 mm
Land Length	2.5 mm (2.25 mm minimum)
Land Pattern Solder Finish Solder Composition Solder Thickness	 63/37 SnPb 15 micrometers minimum, measured at the crest of the reflowed land
D/A Pad Size Via Diameter Via Location	 Die Size + 7.5 mm (75 mil free area around periphery for wet-out) 13.5mils Center of Vias should start 0.65 mm (25 mils) from the edge of the pad.
Fiducials Size (Diameter) Location	 1 mm (39 mils) for Universal and Zevatech. 0.3 mm for KME equipment. Minimum 2 cross-diagonal corners of the TCP site located within the terminal dimension of the land pattern for Universal and Zevatech equipment. Minimum of 2 adjacent side corners of the TCP site for KME equipment.
Solder Mask Clear area around entire Land Pattern and Fiducials.	 1.25 mm $\pm$ 0.125 mm pull back from the edges of the land pattern and 0.23 $\pm$ 0.125 mm from the ends of the lands.
Fiducials should be clear of Solder Mask.	

NOTE:
1. Land Patterns should be dimensioned in metric.

12.4.10 Package-to-Board Assembly

Intel has demonstrated mounting a Ultra Fine Pitch TCP package to a substrate with a hot bar gang bond process. The hot bar process is a combination of the following processes:

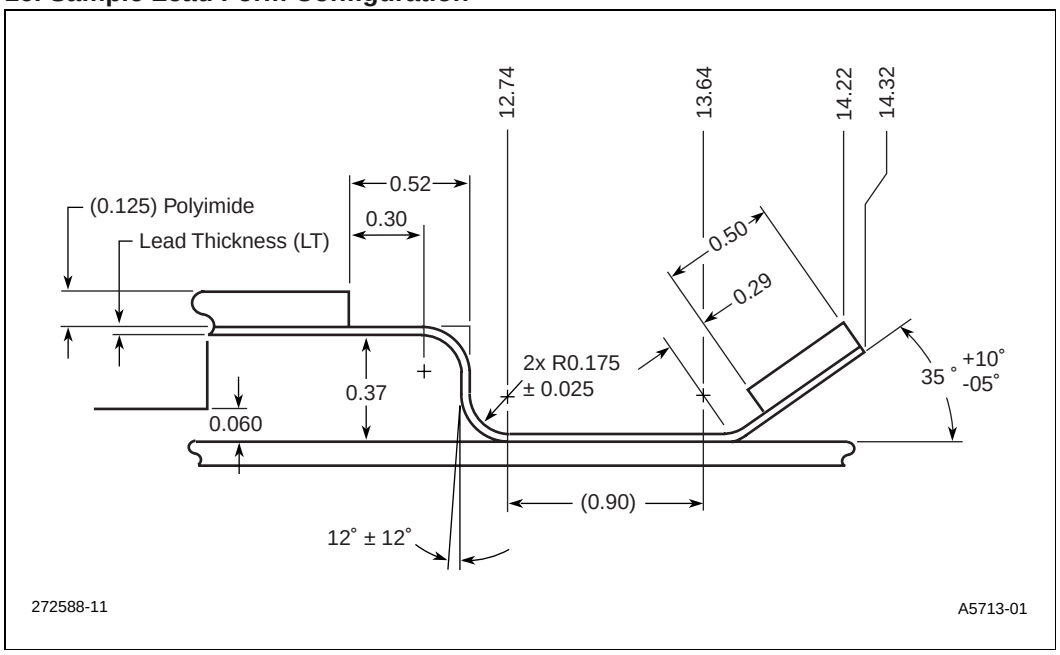
1. Excise and Form
2. Die Attach Dispense
3. Fluxing
4. Placement and Alignment
5. Solder Reflow

12.4.10.1 Excise And Lead Form

Intel has developed the following lead form process which can be used as a starting point for the customer's own development effort. The lead form dimensions may differ depending on the subcontractor or manufacturing site used. A no-form process has been demonstrated by some manufacturers in the industry, but Intel has neither experience with nor reliability data on this method and can make no suggestions for it at this time. Please note that the die attach material dispense pattern bond line thickness suggestions which follow were developed for the specific leadform profile shown in Figure 12-16.

TCP lead forming is a three step process which removes the component from the slide carrier and excess carrier film, cuts the leads from the support structure, and bends the lead to specified configuration and dimensional accuracy. Excise, or removal of the component from the excess tape occurs immediately prior to fluxing and component placement. The recommended tool set should cut the leads free of the tape and then bend them into a modified "gull-wing". Although not required, a "keeper bar" or strip of polyimide carrier ring can be used to maintain coplanarity and lead spacing during fluxing and placement. The keeper bar is a narrow strip of the carrier tape which is cut during the trim operation and remains in place on each row of leads after excise. The excise operation, itself, removes the device area and leaves the test pad and sprocket hole portion of the tape in the slide carrier. Figure 12-16 shows a recommended lead form configuration. Key items are tabulated in Table 12-5.

Figure 12-16. Sample Lead Form Configuration



It is necessary that sufficient distance between the bottom of the silicon device and the die attach pad be built into the leadform to allow for die attach material to attach the device to the board. A thermally conductive die attach medium is used to ensure optimum performance of the device. A suggested die attach material and processing flow are discussed in the next section.

Intel engineers have assessed several different lead form radii for shoulder, heel, and toe angles. To eliminate cracks in the outer plating of the lead which expose the copper base metal, a radius of at least 0.15 mm is suggested.

Table 12-5. Key Lead Form Dimensions

Controlled Dimension	Recommended Range
“Stand-Off” or “Set Back” of Die above Die Pad	0.035 mm to 0.085
Lead Foot Length Minimum	0.90 mm
Lead Foot Angle	0°
Keeper Bar Toe Angle	30° to 45°
Keeper Bar Width	0.5 mm
Toe Radius	0.15 mm (min.)
Heel Radius	0.15 mm (min.)
Lead Shoulder Length	0.3 mm
Lead Shoulder Radius	0.15 mm (min.)

12.4.10.2 Die Attach for Backside Bias and Thermal Dissipation

Intel has selected a thermally conductive die attach material specifically for use with TCP components for printed circuit board applications. This material, Ablebond* 8380, is a silver-filled thermoset polymer. Intel suggests a cure profile of 6 minutes above 130° C.

* Other brands and names are the property of their respective owners.

Electrically conductive, this material was selected for its thermal conductivity and mechanical performance characteristics.

Several die attach materials are available commercially for use as thermally conductive, electrically non-conductive adhesives. These materials may be adequate substitutes for a thermally and electrically conductive die attach material. For additional information on these materials contact your local Intel representative and request the applications note “Thermally Conductive Adhesives.”

Table 12-6. Baseline Material Properties for Thermoset Die Attach

Viscosity (5 RPM) Brookfield	10 ± 2 kcps
Thermal Conductivity	> 2.00 w/mk
Typical Material Composition	Silver-filled polymer
Rework Temperature	≤260°C
Cure Process Profile	130°C for 6 minutes

Alternate materials which meet these criteria may be available but have not been characterized by Intel.

12.4.10.2.1 Handling Ablebond* 8380

Ablestik’s Ablebond* 8380 die attach adhesive should be stored frozen at the Ablestik recommended temperature of -40° C. Prior to use, the material should be removed from cold storage and allowed to thaw to room temperature. The Ablestik recommended thaw times and temperatures for different adhesive containers is shown in Table 12-7.

Table 12-7. Recommended Thaw Times and Temperatures for Different Containers and Container Sizes of Ablebond* 8380 (Courtesy Ablestik)

Container Size	Container Type	Recommended Thaw Time (Hours)	Recommended Thaw Temp (°C)
≤10 cc	Syringe	1.5-2	23-27
≤1 lb	Jar	2-3	23-27

Containers of Ablebond* 8380 that appear to have separated should not be used. Separation is visually observable as a band of color (yellow or amber) along the length or top of the container.

To maintain high quality performance, adhesive dispensed from an unstirred reservoir (10 cc and smaller) must be completely used within a 24 hour period.

All pastes must be used in a 24 hour period from the time the syringe is opened. Any thawed adhesive not required for production should be returned to the freezer immediately. Any thawed adhesives not used (not opened in a 24 hour period) may be refrozen once. Contact Ablestik directly for maximum recommended time between dispense, placement and cure.

A typical 7-step preparation procedure is shown below.

1. Remove syringe from freezer.
2. Thaw syringe at room temperature (23° C-27° C) for 1.5-2 hours.
3. Remove plunger from syringe.
4. Stir or mix the material. Contact Ablestik directly for more information.
5. Attach needle to the syringe.

6. Insert syringe assembly into die attach subsystem.
7. Purge needle for 45-60 seconds.

Follow all manufacturer's suggestions for use.

12.4.10.2.2 Dispense Methods

One of several different dispense methods may be used including needle time/pressure dispense, stamp dispense, positive displacement pattern dispense, etc. Dispense method and pattern may vary depending on thermal via design, and should be developed by the customer to meet the following criteria for a reliable die attachment. The bondline defined in Table 12-8 was developed for the leadform described in Figure 12-16. The percentage of voiding in the bondline directly affects the thermal performance, therefore voiding should be minimized.

Table 12-8. Die Attach Acceptance Criteria

Post-Dry Bondline Thickness	0.025 mm to 0.095 mm
Device Tilt after Dry	≤0.05 mm

Reference material dispense parameters for Ablestik Ablebond* 8380 are listed in Table 12-9, and a reference pattern for a die size of 13.302mm x 12.235mm and a single needle time-pressure dispense system is illustrated in Figure 12-17 and Table 12-10. Further process development may be required to optimize the amount of material dispensed in order to minimize voids, control bond line thickness, and control fillet height. Dispense patterns should be verified for each thermal via pattern.

Figure 12-18 illustrates the low temperature cure profile used at Intel. This profile was set at 130° C maximum temperature as a compromise between snap cure and the need to keep the profile below the glass transition temperature of a majority of PCB materials.

Table 12-9. Intel Developed Time/Pressure Dispense Parameters

Needle Size	20 gauge
Syringe Pressure	6 psi
Line Speed	5.5 mm/sec
Dot Time	0.3 sec
Needle Standoff	0.55 mm
Withdraw Speed	1.0 mm/sec
Withdraw Height	10 mm
Pre-Movement Delay	0 sec
Pre-Stopping Delay	0.3 sec

Note: THE PARAMETERS IN TABLE 12-9 ARE EVALUATION SETTINGS ONLY. VALUES WILL CHANGE DEPENDING ON SEVERAL FACTORS INCLUDING DIE PAD VIA PATTERN, DIE PAD PLATING TYPE, EQUIPMENT SET AND EPOXY VISCOSITY.

Figure 12-17. Basic Dispense Pattern Locations for Die Attach Material

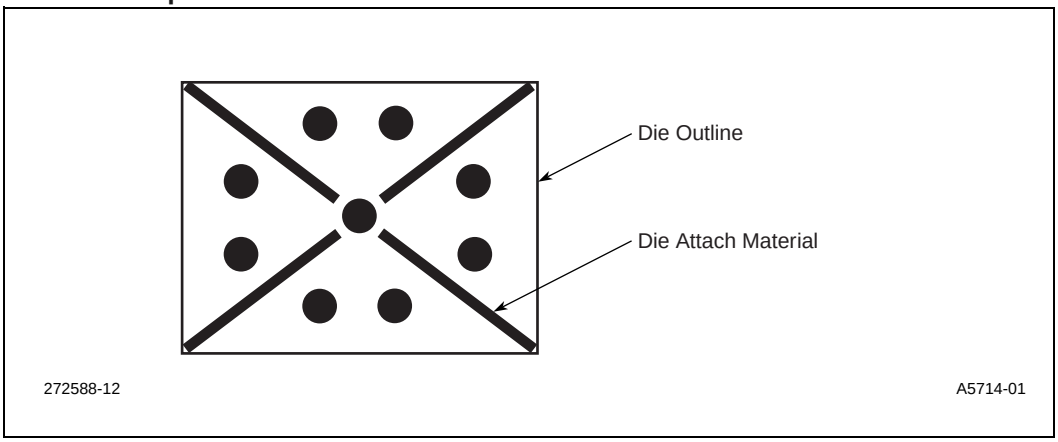
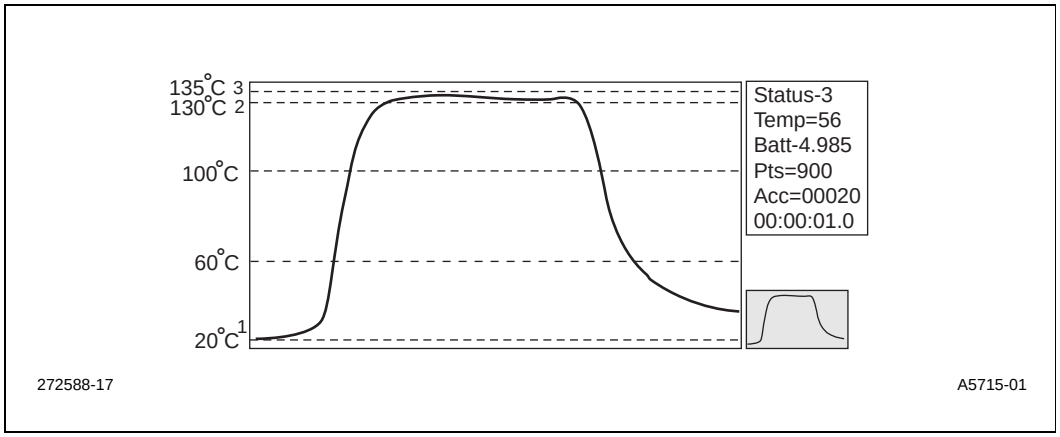


Table 12-10. Sample Die Attach Medium Dispense Pattern: 24 mm Body Size Component and 13.302 x 12.235 mm Die Size Component

STEP	TYPE	GEO[1]	[2]	[3]	[4]	AMOUNT/SPEED
1	DOT	0	0	0	0	0.2
2	LINE	-0.5	-0.5	-6.25	-6.75	5.5
3	DOT	-4. 5	-1.61	0	0	0.2
4	LINE	+0.5	-0.5	6.25	-6.75	5.5
5	DOT	4.5	1.61	0	0	0.2
6	LINE	0.5	0.5	6.25	6.75	5.5
7	DOT	-1.66	4.-5	0	0	0.2
8	LINE	-0.5	0.5	-6.25	6.75	5.5
9	DOT	1.61	-4.5	0	0	0.2
10	DOT	1.61	4.5	0	0	0.2
11	DOT	-4.5	1.66	0	0	0.2
12	DOT	-1.61	-4.5	0	0	0.2
13	DOT	4.5	-1.66	0	0	0.2

This pattern provides baseline information for process development. The pattern requires verification by the board level assembly site.

Figure 12-18. Low-Temperature, Cure Profile Used on a Convection Belt Oven to Cure Ablebond* 8380



12.4.10.2.3 Alternate Die Attach Material

The majority of Japanese OEM manufacturers use Toray-Dow* DA6523. Several contract board assembly manufacturers use Alpha Metals Staystik* 591. Intel has no information on reliability stress test results or manufacturability. Contact Toray-Dow or Alpha Metals for additional information.

12.4.10.3 Fluxing

A Rosin Mildly Activated (RMA), halide free, no residue flux is suggested. Multi-core no-clean X33-04 has been used successfully for the hot bar application for both SnPb and Au lead finish. Optimum results have been obtained by immersing the leads of the TCP component in the flux. Immersion should cover the entire surface of the foot, top and bottom up to the top of the heel radius. The specific gravity of the flux controls the amount of flux which remains on the leads after immersion and should be closely controlled at 0.80 to 0.81. The solids content of the flux should remain in the range 1%-3%. Because this is a no-clean material the surface insulation resistance should be monitored and kept at $>10^9\ \Omega$ minimum between adjacent leads. Extractable ions have been measured for this material at less than 100 ppm Cl-, Na+ and less than 50 ppm K+. The time between application of flux and solder reflow should be minimized.

12.4.10.4 Placement and Alignment

The pick and place accuracy should allow for better than 0.025 mm lead off land misalignment and 10° rotational alignment.

The alignment features of the TCP component include:

1. Sprocket holes in the tape to hold the tape in the carrier.
2. Four tooling holes at the periphery for alignment of the tape to the excise and form die set (see detail of tooling holes in Figure 12-5). Intel has used the tooling holes shown in the upper left and lower right of Figure 12-1 for alignment during processing at Intel. These should not be used during board assembly. The other two tooling holes have been left pristine for use during board assembly.
3. If desired, a polyimide keeper bar design to maintain TCP lead position.

* Other brands and names are the property of their respective owners.

4. A gold plated copper lead identifier flag on pin one corner of the component.

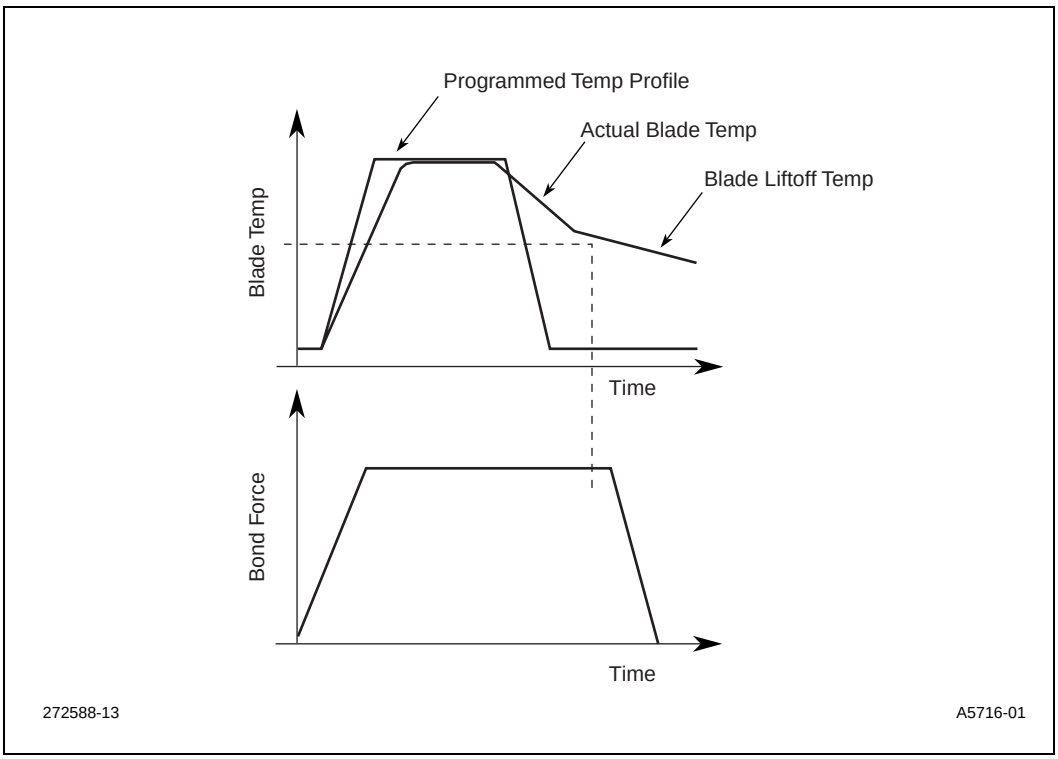
12.4.10.5 Solder Reflow

12.4.10.5.1 Reflow Process Suggestions: Hot Bar

Reflow process parameters can vary significantly depending on board design, support pedestal design, and equipment. Some general guidelines for the hot bar process follow, which can be used by the customer as a starting point for their specific process development.

Intel engineers have done extensive process development of hot bar reflow for 0.25 mm TCP components. The reflow thermal and force profiles are shown in Figure 12-19. Blade design is crucial for effective hot bar reflow. Blades should maintain flatness across the active surface of the blade. Temperature variations across the blade should be less than 10° C. Four independent ceramic blades with tungsten resistors are suggested. Each blade is used to reflow one side of a TCP component. Mean blade-to-blade temperature differentials should be kept less than 5° C. The blade width should be such that the contacted area of the TCP foot is less than the length of the flat of the foot. A baseline thermal profile is shown below. This profile has been shown to yield acceptable solder fillets. Different temperature/time profiles may be required for different thermal densities.

Figure 12-19.



12.4.10.5.2 Suggested Template For Hot Bar Reflow Profile

Blade Temperature.....280 +/- 10° C

Temperature Variation Across Blade.....≤ 10° C

Blade-to-Blade Variation Between Mean Temperature.....5° C

Blade Force.....approximately 12 lbs total (3 lbs./blade for 4 blades)

Dwell Time.....25 sec.

Heel fillets should extend 1/3 to 1/2 the height of the heel radius. The solder wetting angle should be positive. Reliability stress test data has shown that toe fillets are not required for acceptable joint reliability after 1000 cycles of -55° C to 125° C. However, the presence of toe fillets may be a quality indicator for the reflow process.

The pick-up head design can contribute to component alignment control and bond line thickness of the die attach medium. Pick-up contact on the polyimide carrier ring area has been found to provide a wide process window for alignment in some equipment. Pick-up tooling design should be verified with your equipment supplier.

12.4.10.5.3 Removal Process Suggestions After Hot Bar Mount And Cure

Intel has developed the following removal process which can be used as a starting point for the customer's own development effort. The actual times and temperatures may differ depending on the rework machine and equipment utilized. Please note that this process was developed on a 0.062 thick FR-4 PCB with Au die attach pad, using Intel's suggested die attach material Ablebond* 8380. Other PCB assemblies with varying thickness, material and die attach, may require different removal profiles.

TCP removal is a thermally profiled, stepped process, which removes the device from the PCB assembly after die attach cure. This process is centered around breaking the bond between the die attach material and the PCB and/or die, by using the coefficients of thermal expansion variations associated with the die and PCB material. This characteristic of the removal process is based on the thermoset properties associated with Intel's suggested die attach material Ablebond* 8380.

The stepped process is derived from the underboard heating of the removal site, prior to top surface heating. This process allows for the PCB to expand for a longer period of time than the die, creating the forces necessary to break the thermoset die attach bond. Intel has developed the removal process with Air-Vac's* DRS 26 Semi-Automated Soldering and Desoldering Machine. The removal time profile is approximately 135 seconds with the equipment settings as shown in Table 12-11. These actual settings and time may differ depending on the actual configuration of the PCB assembly the TCP is being removed from. The time profile may even be reduced by using higher wattage heating elements.

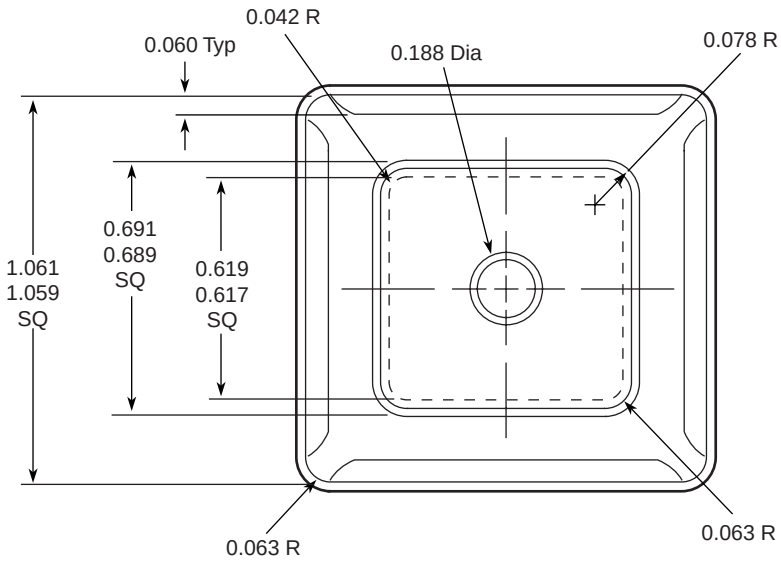
Table 12-11. DRS-26 Settings

Air Pressure	85psi
Underboard Heater	250° C
Wattage	300 W
Airflow	60%
Nozzle Heater	260° C
Wattage	900 W
Airflow	80%
Mode	Manual

Even though this process is centered around a manual method, the DRS-26 allows the user programming capabilities to semi-automate the process to improve throughput and efficiency.

The nozzle assembly that Intel used during the development of this process is a center vacuum ported design with the air flow directed to the outer perimeter of the nozzle. This allows for peripheral heating from the top side of the TCP, which is an advantage when trying to break the thermoset bond created during the curing process. This nozzle was equipped with a high temperature O-ring to seal the vacuum for TCP pick up, around the inner tape perimeter. See Figure 12-20 for the nozzle design.

Figure 12-20. Nozzle Design for Rework Process



The following outline for TCP removal is for a manual operation under the DRS-26 operating environment.

1. Turn on the power and initialize the DRS-26 system.
2. A preheat stage for the underboard and nozzle heating elements should be used for cold system start-up. A 2 minute preheat cycle was utilized with the settings shown in Table 12-11.
3. Place the PCB assembly into the guide rails while positioning the TCP directly over the underboard heating element. The heating element should be positioned approximately 0.25” below the underside of the PCB assembly.
4. Use the vision alignment system to center the removal nozzle to the TCP component to be removed.
5. The nozzle working height should be set to approximately 0.40” above the top surface of the PCB. The system should now be set for the stepped, timed profile for removal.
6. Flux the leads of the TCP prior to starting the heating elements.
7. Turn on the underboard heating element for approximately 30 seconds prior to turning on the nozzle heating element. Once the nozzle heating element has been turned on, run both elements for approximately 1 minute 45 seconds.
8. With approximately 40 seconds left, lower the nozzle assembly to the top of the surface.
9. With approximately 10 seconds left, turn on the system vacuum and slowly raise the nozzle assembly. If the component does not lift, then lower the nozzle assembly with continued heating and try again. Repeat this procedure until the device is removed cleanly.

Follow all manufacturer’s suggestions for use.

12.5 Package Performance

12.5.1 Thermal Performance

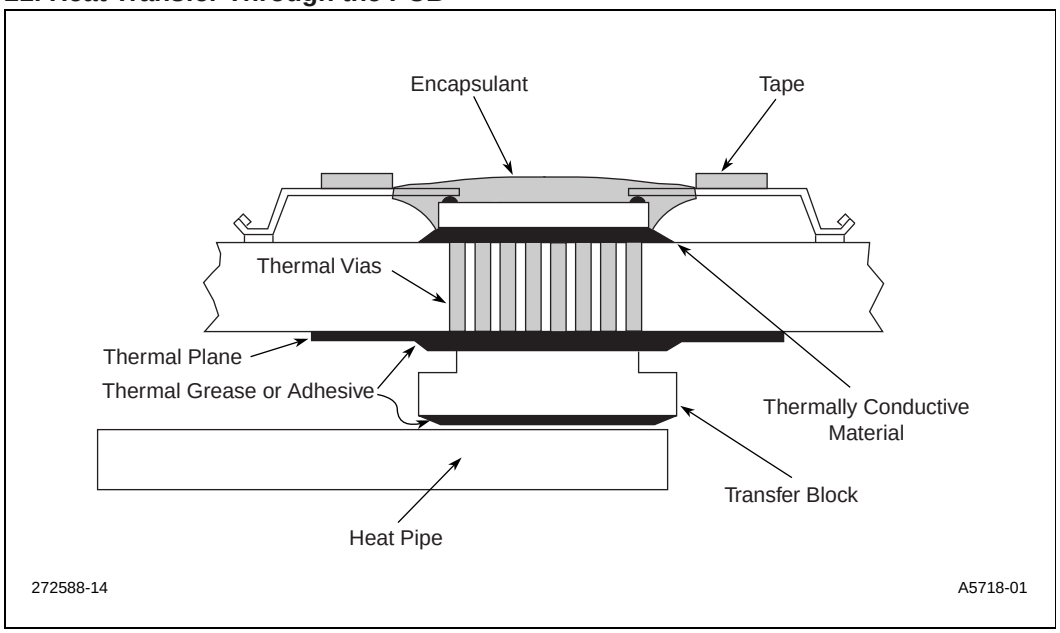
The thermal resistance of a TCP package, or theta-jc, is 0.8°C/W to 2°C/W depending on the product and the thermal design. Simple PCB enhancements such as the addition of thermal vias, alone or with the use of low profile heatsinks, bring the thermal performance in line with requirements for mobile computing platforms which do not have forced convection cooling options available. Key PCB design parameters which influence the thermal behavior of TCP packages mounted on printed circuit boards include the number of board layers, the number of internal power and ground planes, thermal vias and spreading area on the back side of the board. The addition of heat pipe and spreader plate reduces thermal resistance further, up to 50% improvement over the unenhanced performance. This allows the system designer significant flexibility in box design for trade-offs in inter-card spacing, heat pipe design and location, and weight.

Thermal vias in the die attach pad allow the heat from the die to be transferred and spread into the board. Heat is also transferred through the board to the opposite side where it can be further spread and transferred. Figure 12-21 shows thermal vias connecting to a heat spreading plane on the opposite side of the board. A heat pipe is shown for illustration purposes. In the illustration, a transfer block made from copper or aluminum is used to clear the component height on the backside of the board. The other end of the heat pipe is connected to a heat spreading area such as the keyboard plate or the bottom chassis.

Thermal vias can be arranged in several configurations within the die attach pad. It is suggested that a full grid of 0.34 mm (13.5 mil) as-drilled thermal vias be placed on 1.27 mm (50 mil) minimum centers across the die attach pad. Decreasing pitch (increasing via count under the die) will further improve heat transfer into the board. The thermal vias should be connected without thermal relief to the ground planes(s). A ground plane that mirrors the die attach pad should be placed on the opposite side of the board from the TCP site to enhance system heat spreading solutions.

Additional use of heat pipes on the opposite side of the board further enhances thermal performance. Figure 12-21 illustrates a possible mounting. The advantages of mounting the heat pipe to the board rather than the device include: coupling to the major thermal path for this device, the ability to select the adhesive or mechanical attachment method, mechanical isolation of TCP leads from the load of the heatsink especially in vibration, and the ability to utilize potential open real estate on the back side of the board to increase the thermally active area.

Figure 12-21. Heat Transfer Through the PCB



For detailed information on system thermal design solutions please contact your local Intel sales office.

12.6 Electrical Performance

Intel has developed a methodology to characterize the electrical performance of Intel TCP components. All information is generated on a product specific basis.

The construction of TCP components is unique compared to traditional CPU packages such as PGAs and PQFPs. Both the PGA and the PQFP use wire bond technology that connects the die to the package. The package leads then provide the final connection to the printed circuit board. The TCP package uses TAB (tape automated bonding) interconnect which provides a direct connection from the die to the outside world. The result is a low inductance path from the die to the board when compared to traditional PGA or PQFP packages.

Originally, the mobile processor required a thermally and electrically conductive path between the board and the device. Additional tests have revealed that an electrically conductive path between the board and the device is not required.

For more detail about the electrical performance of a specific product in the TCP package consult the datasheet or call your local Intel sales office.

12.7 Mechanical Performance

12.7.1 Lead Strength

Lead fragility testing has shown that the TCP component, mounted to a PCB without D/A material, can withstand up to 11X its own weight under random vibration testing up to a frequency of 1000 Hz. No solder joint degradation was seen.

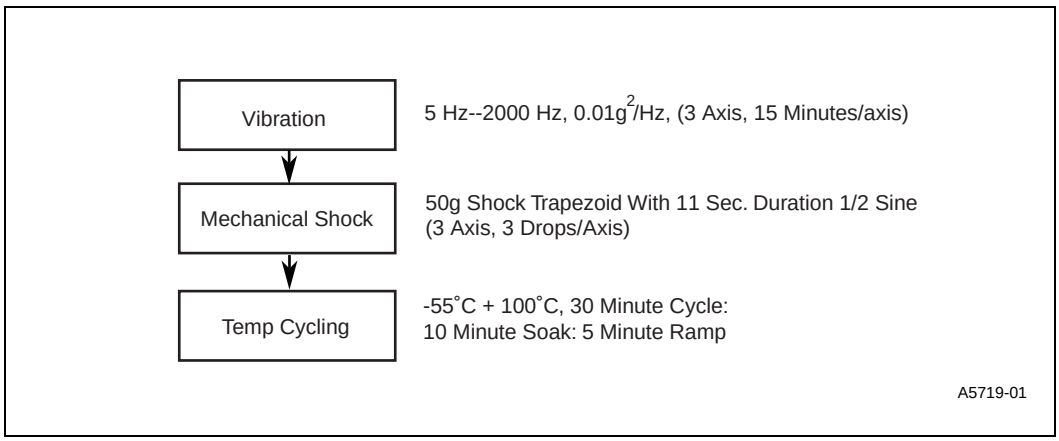
12.7.2 Solder Joint Reliability

Concern over the integrity of gold leadfinish in direct contact with tin-lead (Sn-Pb) solder has led to much study. The major cause of concern is the formation of Au-Sn intermetallic compounds in the joint which segregate at grain boundaries and metal layer interfaces. These compounds are in themselves brittle and can cause embrittlement of the joint as a whole. Such embrittlement can cause mechanical and electrical failure over time in high vibration environments or under situations with much thermal cycling induced fatigue. The TCP component was put through multiple tests to ensure mechanical integrity.

The TCP package lead has a nickel underplate and gold final plate in the outer lead bond area of the package. The nickel acts as a barrier between the copper lead and gold surface, ensuring a solderable lead at the customer site.

Intel has done extensive testing on the reliability of solder joints. Packages with Ni/Au were assembled onto boards with various plating thicknesses which bracket Intel's recommended lead finish thickness. No failures were detected after the boards were subjected to vibration stress, mechanical shock, and thermal cycling stresses performed in Figure 12-22.

Figure 12-22. Series of Stresses Performed

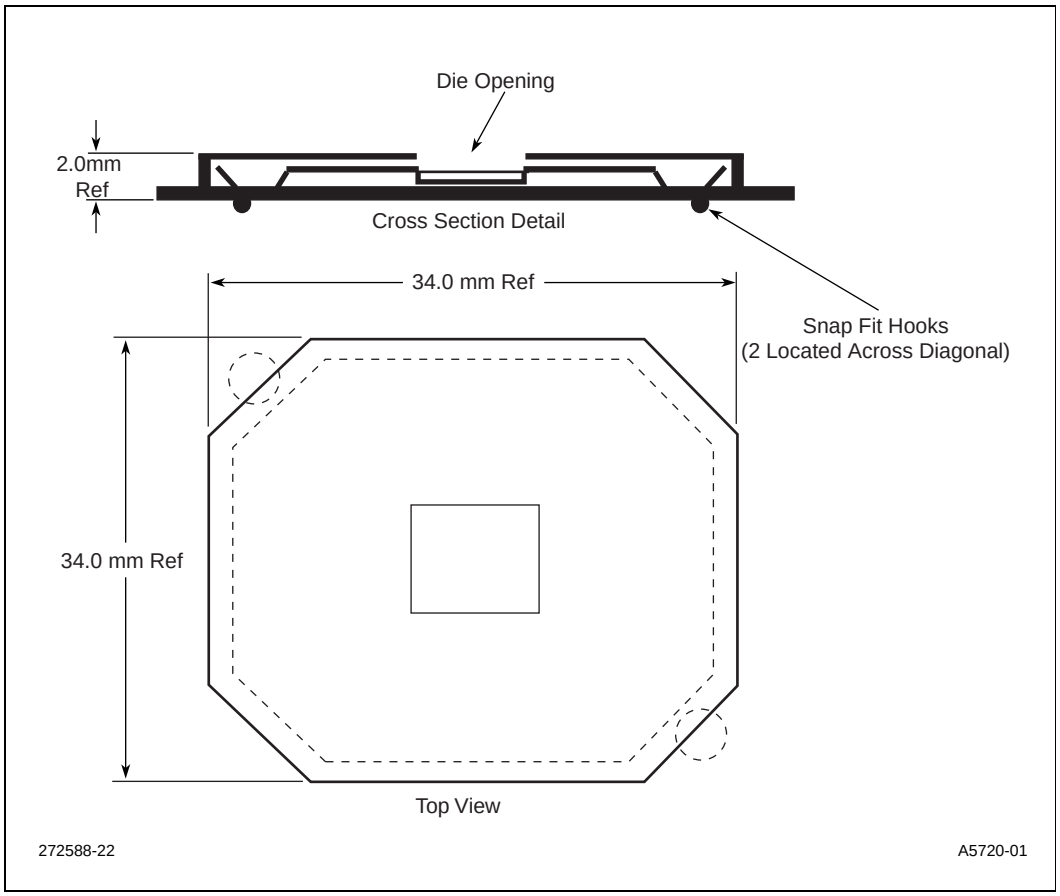


12.7.3 Lead Guard

Because the Intel TCP has thinner leads and a thin tape body compared with other plastic surface mount devices, it can be relatively more susceptible to handling damage once on the printed circuit board. A cover or "lead guard", can be used to protect the device after mounting. A drawing of an Intel TCP lead guard is shown in Figure 12-23. The lead guard can be used to protect the TCP after it is mounted to the PCB for protection through the factory processes, as a shipping protective cover, and/or before and after final assembly into the computer box.

Intel has developed a light weight, low profile and low cost TCP lead guard. For additional information on this design, please request a copy of the *TCP Lead Guard Application Note* from your Intel representative.

Figure 12-23. TCP Lead Guard



12.8 Selected Readings in TCP and Ultra-fine Pitch Hot Bar Reflow

12.8.1 Outer Lead Metallurgy References

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12.8.3 Thermal Performance References

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12.9 Revision History

- General review of the chapter