FUJITSU SEMICONDUCTOR

MB91F464AA preliminary datasheet

MB91460 series

European MCU Design Centre (EMDC)
Fujitsu Microelectronics Europe GmbH
Pittlerstrasse 47
63225 Langen, Germany
Version 1.10

Revision History

Version	Date	Remark
0.10	2005-09-20	Initial draft
0.11	2005-10-11	Updated pinout + resource mix + RAM sizes
0.30	2005-11-19	Updated pinout + resource mix + RAM sizes (design spec.rev.3.0)
0.31	2006-01-09	Absolute max. ratings corrected
0.32	2006-01-19	Package type changed (LQFP)
0.33	2006-01-23	Added: Relationship of supply voltages
1.00	2006-02-14	Added IO-Map as Appendix 1
1.01	2006-02-22	Corrected section 4.2. (AVCC5/AVSS pin comment)
1.02	2006-05-02	Flash memory access timing settings added
1.03	2006-05-12	ADC operating conditions updated, ICC run mode updated
1.04	2006-05-23	IO-Map added with new formatting
1.05	2006-06-19	ROMS setting corrected in memory map
1.06	2006-06-19	Special notes: Flash write only with 16bit
1.10	2006-10-12	First public release
1.10		Latest revision

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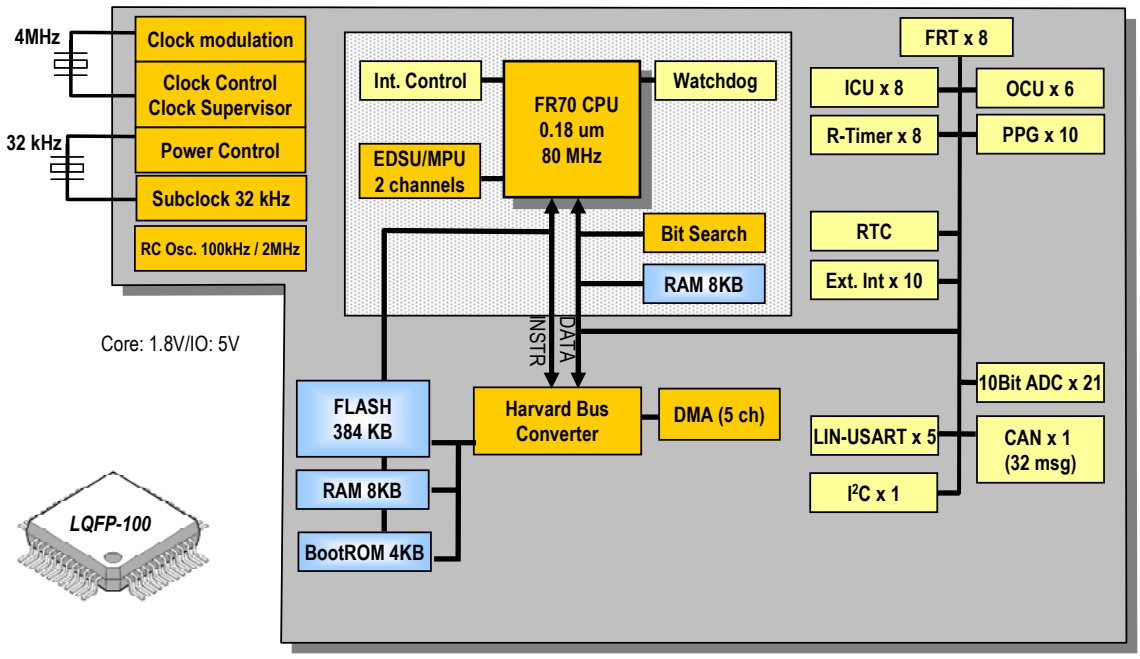
1 Overview

The MB91F464AA is the 100-pin body control flash MCU of the M91460 family.
The corresponding evaluation device is the MB91V460.

1.1 Block Diagram



2 Feature List

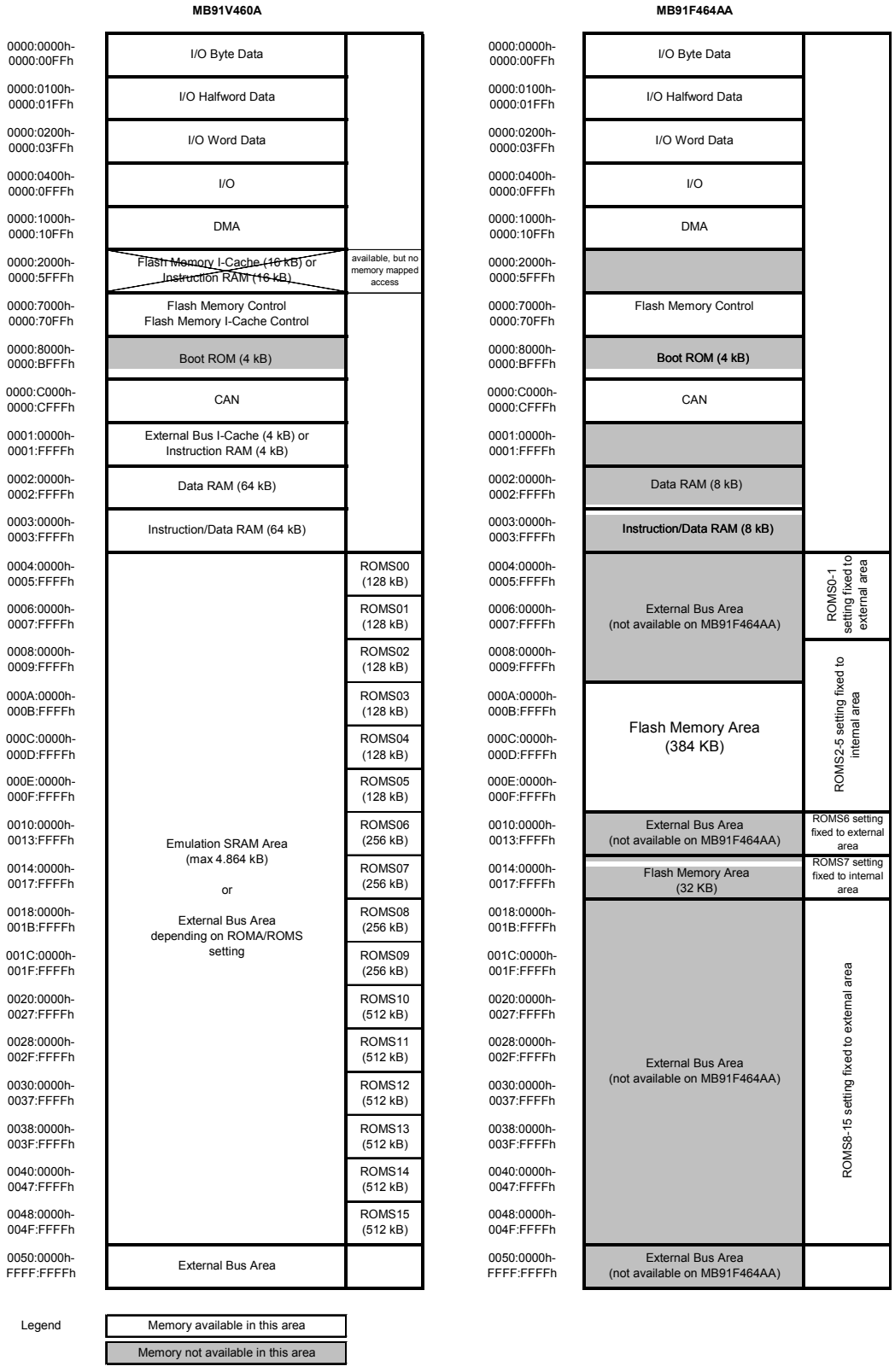
2.1 Overview Table

Feature	MB91V460	MB91F464AA	MB91F465KA
Core frequency	80 MHz	80 MHz	80 MHz
Resource frequency	40 MHz	40 MHz	40 MHz
Watchdog	yes	yes	yes
Bit Search	yes	yes	yes
Reset Input	yes	yes	yes
Clock Modulator	(yes)	yes	yes
DMA	5 ch	5 ch	5 ch
MPU/EDSU	16 ch	2 ch	2 ch
Flash	external	384 KB + 32 KB	512 KB + 32 KB
Satellite Flash	external	-	-
Flash Protection	n.a.	yes	yes
D-bus RAM	64 KB	8 KB	8 KB
GP RAM	64 KB	8 KB	8 KB
Direct mapped cache	16 KB	-	4 KB
Boot-ROM	4 kB	4 KB	4 KB
RTC	1 ch	1 ch	1 ch
Free Running Timer	8 ch	8 ch	8 ch
ICU	8 ch	8 ch	8 ch
OCU	8 ch	6 ch	8 ch
Reload Timer	8 ch	8 ch	8 ch
PPG	16 ch	10 ch	12 ch
PFM	1 ch	-	-
Sound Generator	1 ch	-	-
UpDown Counter	4 ch	-	-
C_CAN	6 ch (128 msg buffer)	1 ch (32 msg.)	1 ch (32 msg.)
LIN-USART	16 ch (4 ch FIFO)	5 ch (1 ch FIFO)	5 ch (1 ch FIFO)
I2C	4 ch	1 ch	1 ch

Feature	MB91V460	MB91F464AA	MB91F465KA
FR external bus	32-bit address / 32-bit data / 8 chip select	-	-
External Interrupts	16 ch	10 ch	10 ch
NMI	1 ch	-	-
SMC (Quad Option)	6 ch	-	-
LCD	1 ch 40x4	-	-
ADC (10-bit)	32 ch	21 ch	26 ch
Alarm Comparator	2 ch	-	-
General Purpose Port I/O	14	-	7
Low voltage detection	yes	yes	yes
Clock Supervisor	yes	yes	yes
Package	BGA 666	LQFP-100	LQFP-120

2.2 Core Functionality

2.2.1 Memory Map



2.2.2 FR70 CPU Core

- 32-bit RISC, load/store architecture, pipeline 5 stages
- Maximum operating frequency: Core clock = 64 MHz to 100 MHz (device dependent)
  (Source oscillation= 4 MHz, multiplied by 16 to 25 (PLL clock multiplier method))
- General-purpose registers: 16 x 32 bits
- 16-bit fixed-length instruction (Base instruction)
- 32-bit linear address space: 4 Gbytes
- Instructions suitable for embedded application
  - Transfer command between memories
  - Bit-processing instruction
  - Barrel-shift instructions
- Instructions supporting C-language
- Function's enter command /exit command
- Multi-load/store command of register contents
- Assembler statement is also easily available
  Register's interlock function
- Multiplier's embedded application/command level support
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS are saved): 6 cycles (16 priority level)
- Harvard architecture enables simultaneous execution of program access and data access
- Memory protection function
- Embedded debug support
- Commands compatible with FR family

2.2.3 Instruction Cache

- I-Cache is not available on MB91F464AA.

2.2.4 Interrupt Controller

- A total of 10 external interrupt lines (8 normal interrupt pins, 2 interrupt pins shared with peripheral inputs for Wake Up from STOP mode (CAN RX and I^2C SDA)
- Interrupts from internal peripherals (128 interrupt vectors)
- Priority levels programmable for normal interrupt lines excluding the nonmaskable one (16 levels)

- Capable of using the normal interrupt pins for Wake Up from STOP mode

2.2.5 External Bus Interface

- An External Bus Interface is not available on MB91F464AA.

2.2.6 DMA Controller

- Four transfer modes supported: single/block, burst, continuous transfer, and fly-by
- 5 channels
- 3 types of transfer sources (external pins/internal peripherals/and software)
- Up to 128 selectable internal transfer sources
- Addressing mode: Specifying up to 32-bit addresses (Increment/decrement/fixed)
- Transfer mode (Demand transfer/burst transfer/step transfer/block transfer)
- Transferred data size selectable from among 8, 16, and 32 bits

2.2.7 Internal Data RAM

- 8 KBytes integrated
- Zero wait state for read/write access

2.2.8 Internal Program/Data RAM

- 8 kBytes integrated
- Zero wait state for read/write access of instructions
- One wait state for read/write access of data

2.3 Embedded Program/Data Memory

2.3.1 Flash Features

- 384+32 KByte Flash
- Power: Single +3.0-5.5V supply
- Programmable wait states for read/write access;
- Read 16/32bit width, write 16 bit width
- Flash security with security vector at 0x0014:8000 – 0x0014:800F[1]
- Operation modes:
- (1) 32-bit CPU mode:
  - CPU reads and executes programs in word (32-bit) length units.
  - Flash writing is not possible.
  - Actual Flash Memory access is performed in word (32-bit) length units.
- (2) 16-bit CPU mode:
  - CPU reads and writes in half-word (16-bit) length units.
  - Program execution from the Flash is not possible.
  - Actual Flash Memory access is performed in word (16-bit) length units.
- (3) Flash memory mode (external access to Flash memory enabled)
- Features (Through combination of Flash memory macro and FR-CPU interface circuit):
  - Functions as CPU program/data storage memory.
  - Enables access to 32-bit bus width.
  - Enables read/write/erase by CPU (auto program algorithm*).
  - Functions equivalent to MBM29LV400TC stand-alone Flash-memory product.
  - Enables read/write/erase by parallel Flash programmer (auto program algorithm*).

    *: Auto program algorithm = Embedded Algorithm TM

[1] See MB91460 hardware manual for further details.

2.3.2 CPU Mode

2.3.2.1 Flash configuration in CPU mode

Flash memory map in CPU mode (MD[2:0] = 00x)

addr									
0014:FFFFh 0014:C000h	SA6 (8kB)				SA7 (8kB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8kB)				SA5 (8kB)				
0014:7FFFh 0014:4000h	SA2 (8kB)				SA3 (8kB)				
0014:3FFFh 0014:0000h	SA0 (8kB)				SA1 (8kB)				
0013:FFFFh 0012:0000h	SA22 (64kB)				SA23 (64kB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64kB)				SA21 (64kB)				
000F:FFFFh 000E:0000h	SA18 (64kB)				SA19 (64kB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64kB)				SA17 (64kB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64kB)				SA15 (64kB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64kB)				SA13 (64kB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64kB)				SA11 (64kB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64kB)				SA9 (64kB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				

Legend	
	Memory available in this area
	Memory not available in this area

2.3.2.2 Flash access timing settings in CPU mode

The flash access timing is described in MB91460 Hardware Manual chapter 11. The following tables list all settings for a given Core Frequency for Flash read and write access.

Flash read timing settings for MB91F464AA

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Comment
to 20 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 56 MHz	1	1	2	-	3	
to 80 MHz	1	1	3	-	4	

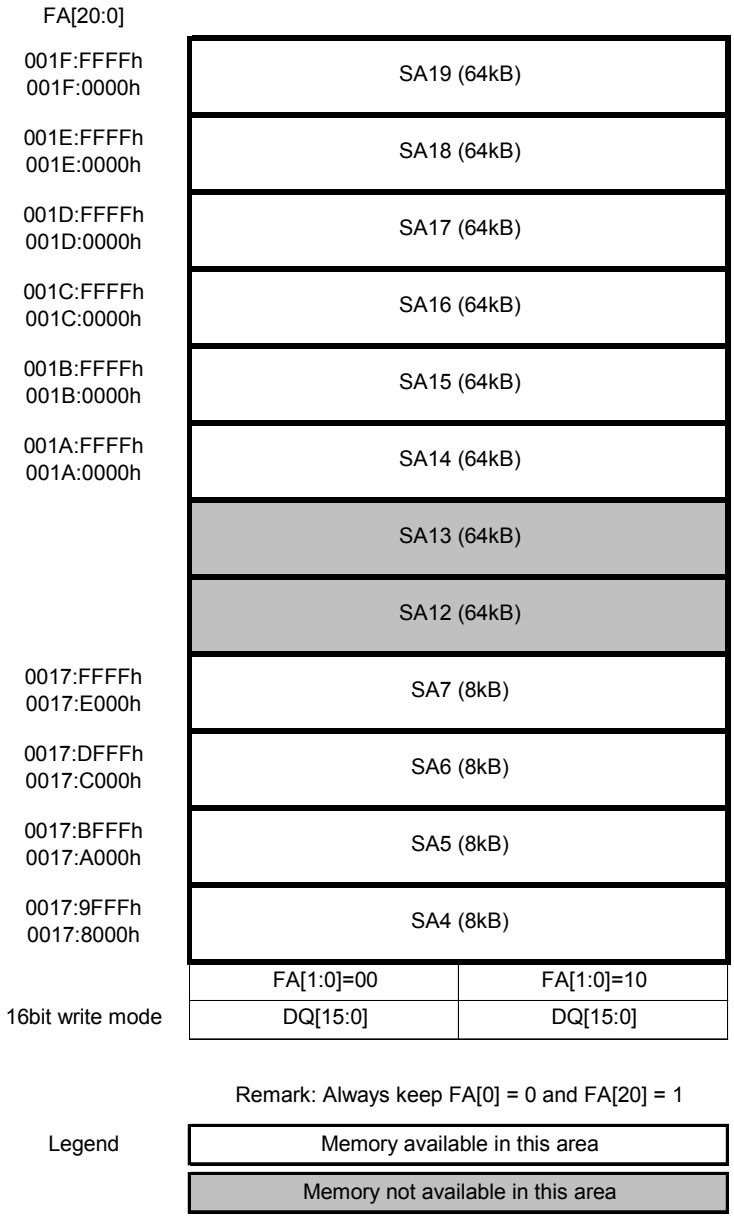
Flash write timing settings for MB91F464AA (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Comment
2 MHz	0	-	-	0	1	
to 20 MHz	0	-	-	0	3	
to 32 MHz	1	-	-	0	4	
to 56 MHz	1	-	-	0	5	
to 76 MHz	1	-	-	0	6	
to 80 MHz	1	-	-	0	7	

2.3.3 Parallel flash programming mode

2.3.3.1 Flash configuration in parallel flash programming mode

Parallel Flash programming mode (MD[2:0] = 111)



Remark: Always keep FA[0] = 0 and FA[20] = 1

Legend	
	Memory available in this area
	Memory not available in this area

2.3.3.2 Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 16.5 Mbit Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	MB91F464AA external pins			Comment
		Flash memory mode	Normal function	Pin number	
-	INITX	-	INITX	52	
RESET	-	FRSTX	GP16_7	53	
-	-	MD2	MD2	99	Set to ‘1’
-	-	MD1	MD1	98	Set to ‘1’
-	-	MD0	MD0	92	Set to ‘1’
RY/BY	FMCS:RDY bit	RY/BYX	GP24_0	74	
BYTE	Internally fixed to ‘H’	BYTEX	GP24_2	78	
WE	Internal control signal + control via interface circuit	WEX	GP28_3	29	
OE		OEX	GP28_2	28	
CE		CEX	GP28_1	27	
-		ATDIN	GP22_1	73	Set to ‘0’
-		EQIN	GP22_0	72	Set to ‘0’
-		TESTX	GP24_3	79	Set to ‘1’
-		RDYI	GP24_1	77	Set to ‘0’
A0	Internal address bus	FA0	GP19_2	47	Set to ‘0’
A1 to A8		FA1 to FA8	GP27_0 to GP27_7	16 to 23	
A9 to A16		FA9 to FA16	GP15_0 to GP15_5, GP21_0, GP21_1	68 to 71, 10, 11, 57, 58	
A17 to A19		FA17 to FA19	GP21_2, GP21_4, GP21_5	59, 60, 61	
A20 to A21		FA20, FA21	GP21_6, GP28_0	62, 24	Set to ‘1’
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	GP17_0 to GP17_7	48, 49, 54, 55, 56, 65, 66, 67	
DQ8 to DQ15		DQ8 to DQ15	GP14_0 to GP14_7	2 to 9	

2.3.4 Flash Security

2.3.4.1 Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the flash security module:

FSV1: 0x14:8000 **BSV1: 0x14:8004**

FSV2: 0x14:8008 **BSV2: 0x14:800C**

2.3.4.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 kByte sectors.

■ **FSV1 (bits 31 to 16)**

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1[31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to '0'	set to '0'	set to '0'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '0'	set to '1'	set to '0'	Write Protection (all device modes, without exception)
set all to '0'	set to '0'	set to '1'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000") and Write Protection (all device modes)
set all to '0'	set to '1'	set to '0'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '1'	set to '1'	set to '0'	Write Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '1'	set to '1'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000") and Write Protection (all device modes except INTVEC mode MD[2:0]="000")

■ **FSV1 (bits 15 to 0)**

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 kByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1[15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	-	set to '0'	set to '1'	not available
FSV1[1]	-	set to '0'	set to '1'	not available
FSV1[2]	-	set to '0'	set to '1'	not available
FSV1[3]	-	set to '0'	set to '1'	not available
FSV1[4]	SA4	set to '0'	-	**Write protection is mandatory!**
FSV1[5]	SA5	set to '0'	set to '1'	
FSV1[6]	SA6	set to '0'	set to '1'	
FSV1[7]	SA7	set to '0'	set to '1'	
FSV1[8]	-	set to '0'	set to '1'	not available
FSV1[9]	-	set to '0'	set to '1'	not available
FSV1[10]	-	set to '0'	set to '1'	not available
FSV1[11]	-	set to '0'	set to '1'	not available
FSV1[12]	-	set to '0'	set to '1'	not available
FSV1[13]	-	set to '0'	set to '1'	not available
FSV1[14]	-	set to '0'	set to '1'	not available
FSV1[15]	-	set to '0'	set to '1'	not available

Remark: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the flash content or manipulate data by writing.

2.3.4.3 Security Vector FSV2

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 kByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	-	set to '0'	set to '1'	not available
FSV2[1]	-	set to '0'	set to '1'	not available
FSV2[2]	-	set to '0'	set to '1'	not available
FSV2[3]	-	set to '0'	set to '1'	not available
FSV2[4]	-	set to '0'	set to '1'	not available
FSV2[5]	-	set to '0'	set to '1'	not available
FSV2[6]	SA14	set to '0'	set to '1'	
FSV2[7]	SA15	set to '0'	set to '1'	
FSV2[8]	SA16	set to '0'	set to '1'	
FSV2[9]	SA17	set to '0'	set to '1'	
FSV2[10]	SA18	set to '0'	set to '1'	
FSV2[11]	SA19	set to '0'	set to '1'	
FSV2[12-32]	-	-	-'	not available

2.3.4.4 Register description for Flash Security

For a description of Flash Security registers please refer to Hardware Manual chapter 55.

2.4 Peripheral Function

- General-purpose port : All functional pins can be used as general-purpose ports, if the corresponding function is not needed.
    - N channel open drain port out of above: 2 (for I^2C)

- A/D converter : 21 channels (1 unit)
    - Series-parallel type
    - Resolution: 10 bits
    - Minimum conversion time: 3µs
    - Single conversion mode
    - Continuous conversion mode
    - Stop conversion mode
    - Activation by software or external trigger can be selected
    - Reload timer 7 and A/D Converter co-operate

- External interrupt input : 8 + 2 channels
    - Can be programmed to be edge sensitive or level sensitive
    - Interrupt mask and request pending bits per channel
    - 1 channel combined with CAN RX for wakeup
    - 1 channel combined with I^2C SDA for wakeup

- Bit search module (using REALOS)
    - Function to search the first bit position of “1”, “0”, “Changed” from MSB (most significant bit) within 1 word

- Reload timer : 16 bits x 8 channels
    - 16-bit reload counter
    - Includes clock prescaler ($f_{RES}/2^1$, $f_{RES}/2^3$, $f_{RES}/2^5$, $f_{RES}/2^6$, $f_{RES}/2^7$)

- Free-run timer : 16 bits x 8 channels
    - 16-bit free running counter, signals an interrupt when overflow or match with compare register
    - Includes prescaler ($f_{RES}/2^2$, $f_{RES}/2^4$, $f_{RES}/2^5$, $f_{RES}/2^6$)
    - Timer data register has R/W access

- PPG : 16 bit x 10 channels
  - 16 bit down counter, cycle and duty setting registers
  - Interrupt at triggering, cycle or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows $f_{RES}/2^0$, $f_{RES}/2^2$, $f_{RES}/2^4$, $f_{RES}/2^6$ as counter clock
  - Can be triggered by software, reload timer or external trigger event
  - Reload timer 0/1 available as trigger for PPG 0/1/2/3
  - Reload timer 2/3 available as trigger for PPG 4/5/6/7
  - Reload timer 4/5 available as trigger for PPG 8/9

- Input capture : 16 bits x 8 channels
  - Rising edge, falling edge or rising & falling edge sensitive
  - Free-run timer 0 and input capture 0/1 co-operate
  - Free-run timer 1 and input capture 2/3 co-operate
  - Free-run timer 4 and input capture 4/5 co-operate
  - Free-run timer 5 and input capture 6/7 co-operate

- Output compare : 16 bits x 6 channels
  - Signals an interrupt when a match with of 16-bit IO timer occurs
  - An output signal can be generated
  - Free-run timer 2 and output compare 0/1 co-operate
  - Free-run timer 3 and output compare 2/3 co-operate
  - Free-run timer 6 and output compare 4/5 co-operate

- LIN-USART (LIN=Local Interconnect Network) : 5 channels
  - Full-duplex double buffer system
  - With parity/without parity selectable
  - 1 or 2 stop bits selectable
  - 7 or 8 bits data length selectable
  - NRZ type transfer format
  - Asynchronous /synchronous communications selectable
  - Master-slave communication function (multiprocessor mode)
  - Dedicated baud rate prescaler is embedded in each channel
  - External clock is able to use as transfer clock
  - Parity error, frame error, and overrun error detecting functions

- SPI compatible
- LIN master and slave
- LIN-USART 0 and ICU 0 co-operate (for LIN sync field in slave mode)
- LIN-USART 1 and ICU 1 co-operate (for LIN sync field in slave mode)
- LIN-USART 2 and ICU 2 co-operate (for LIN sync field in slave mode)
- LIN USART 3 and ICU 3 co-operate (for LIN sync field in slave mode)
- LIN USART 4 and ICU 4 co-operate (for LIN sync field in slave mode)

- CAN : 1 channel
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1 Mbit/s
  - 32 message objects
  - Each message object has its own identifier mask
  - Programmable FIFO mode (cocatenation of message objects)
  - Maskable interrupt
  - Disabled Automatic Retransmission mode for Time Triggered CAN applications
  - Programmable loop-back mode for self-test operation

- I^2C (400k fast mode) : 1 channel
  - Master or slave transmission
  - Arbitration function
  - Clock synchronization function
  - Slave address and general call address detect function
  - Transfer direction detect function
  - Start condition repeat generation and detection function
  - Bus error detect function
  - Compatible to I2C standard and fast mode specification (operation up to 400 kHz, 10 bit addressing)
  - Includes clock divider functionality
  - SCL and SDA lines include optional noise filter. The noise filter allows the suppression of spikes in the range of 1 to 1.5 cycles of the Peripheral Clock.

- Stepper Motor Controller : 0 channels
  - There are no Stepper Motor Controllers on MB91F464AA.

- Timebase/watchdog timer (26 bits)
  - Adjustable watchdog timer interval (between 2^{20} and 2^{26} system clock cycles)

- Real-time clock (counts during stop mode)
  - RTC module can be clocked either from 32 kHz quartz, 4 MHz quartz or from the RC Oscillator
  - Facility to correct oscillation deviation (subclock calibration)
  - Read/write accessible second/minute/ hour registers
  - Can signal interrupts every halfsecond/second/ minute/hour/day
  - Internal clock divider and prescaler provide exact 1s clock based on a 4 MHz or a 32 kHz clock input
  - Prescaler value for 4 MHz is $1E847F_H$
  - Prescaler value for 32 kHz is $003FFF_H$

- Clock supervisor
  - Monitors external 32kHz and 4MHz for fails (e.g. crystal breaks)
  - Switches in case of fail to an available recovery clock (other oscillator, or RC oscillator)

- Clock modulator (reduction of EME)

- Subclock calibration
  - Calibration of the RTC timer in 32 kHz or RC oscillator operation, based on the more accurate 4 MHz quartz is possible

- Main oscillation stabilisation timer
  - 23 bit counter for main oscillation stabilisation wait when running in sub clock mode
  - Generates an interrupt when stabilisation time has elapsed

- Sub oscillation stabilisation timer
  - 15 bit counter for sub oscillation stabilisation wait when running in main clock mode
  - Generates an interrupt when stabilisation time has elapsed

3 Recommended Settings

3.1 PLL and Clockgear settings

Please note that for MB91F464AA core base clock frequencies above 80MHz are not allowed

Recommended PLL divider and clockgear settings

PLL Input (CK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core base Clock [MHz]
	DIVM	DIVN	DIVG	MULG		
4	2	20	16	20	160	80
4	2	19	16	20	152	76
4	2	18	16	20	144	72
4	2	17	16	16	136	68
4	2	16	16	16	128	64
4	2	15	16	16	120	60
4	2	14	16	16	112	56
4	2	13	16	12	104	52
4	2	12	16	12	96	48
4	2	11	16	12	88	44
4	4	10	16	24	160	40
4	4	9	16	24	144	36
4	4	8	16	24	128	32
4	4	7	16	24	112	28
4	6	6	16	24	144	24
4	8	5	16	28	160	20
4	10	4	16	32	160	16
4	12	3	16	32	144	12

3.2 Flash interface settings

Please refer to section 2.3.2.2 ‘Flash access timing settings in CPU mode’ for the recommended Flash interface settings.

3.3 Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 80MHz.

Please note that Fmax must not exceed 80MHz.

The flash access time settings (see section 2.3.2.2) need to be adjusted according to Fmax while the PLL and clockgear settings (see section 3.1) should be set according to base clock frequency.

Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	3	026F	72	65.5	79.9
1	3	026F	68	62	75.3
1	3	026F	64	58.5	70.7
1	5	02AE	64	55.3	75.9
2	3	046E	64	55.3	75.9
1	3	026F	60	54.9	66.1
1	5	02AE	60	51.9	71
1	7	02ED	60	49.3	76.7
3	3	066D	60	49.3	76.7
1	3	026F	56	51.4	61.6
1	5	02AE	56	48.6	66.1
1	7	02ED	56	46.1	71.4
1	9	032C	56	43.8	77.6
2	3	046E	56	48.6	66.1
2	5	04AC	56	43.8	77.6
3	3	066D	56	46.1	71.4
4	3	086C	56	43.8	77.6
1	3	026F	52	47.8	57
1	5	02AE	52	45.2	61.2
1	7	02ED	52	42.9	66.1
1	9	032C	52	40.8	71.8
1	11	036B	52	38.8	78.6
2	3	046E	52	45.2	61.2
2	5	04AC	52	40.8	71.8
3	3	066D	52	42.9	66.1
4	3	086C	52	40.8	71.8
5	3	0A6B	52	38.8	78.6
1	3	026F	48	44.2	52.5
1	5	02AE	48	41.8	56.4
1	7	02ED	48	39.6	60.9
1	9	032C	48	37.7	66.1
1	11	036B	48	35.9	72.3
1	13	03AA	48	34.3	79.9
2	3	046E	48	41.8	56.4
2	5	04AC	48	37.7	66.1
2	7	04EA	48	34.3	79.9
3	3	066D	48	39.6	60.9

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
3	5	06AA	48	34.3	79.9
4	3	086C	48	37.7	66.1
5	3	0A6B	48	35.9	72.3
6	3	0C6A	48	34.3	79.9
1	3	026F	44	40.6	48.1
1	5	02AE	44	38.4	51.6
1	7	02ED	44	36.4	55.7
1	9	032C	44	34.6	60.4
1	11	036B	44	33	66.1
1	13	03AA	44	31.5	73
2	3	046E	44	38.4	51.6
2	5	04AC	44	34.6	60.4
2	7	04EA	44	31.5	73
3	3	066D	44	36.4	55.7
3	5	06AA	44	31.5	73
4	3	086C	44	34.6	60.4
5	3	0A6B	44	33	66.1
6	3	0C6A	44	31.5	73
1	3	026F	40	37	43.6
1	5	02AE	40	34.9	46.8
1	7	02ED	40	33.1	50.5
1	9	032C	40	31.5	54.8
1	11	036B	40	30	59.9
1	13	03AA	40	28.7	66.1
1	15	03E9	40	27.4	73.7
2	3	046E	40	34.9	46.8
2	5	04AC	40	31.5	54.8
2	7	04EA	40	28.7	66.1
3	3	066D	40	33.1	50.5
3	5	06AA	40	28.7	66.1
4	3	086C	40	31.5	54.8
5	3	0A6B	40	30	59.9
6	3	0C6A	40	28.7	66.1
7	3	0E69	40	27.4	73.7
1	3	026F	36	33.3	39.2
1	5	02AE	36	31.5	42
1	7	02ED	36	29.9	45.3
1	9	032C	36	28.4	49.2
1	11	036B	36	27.1	53.8
1	13	03AA	36	25.8	59.3
1	15	03E9	36	24.7	66.1
2	3	046E	36	31.5	42
2	5	04AC	36	28.4	49.2
2	7	04EA	36	25.8	59.3
2	9	0528	36	23.7	74.7
3	3	066D	36	29.9	45.3
3	5	06AA	36	25.8	59.3
4	3	086C	36	28.4	49.2
4	5	08A8	36	23.7	74.7
5	3	0A6B	36	27.1	53.8
6	3	0C6A	36	25.8	59.3
7	3	0E69	36	24.7	66.1
8	3	1068	36	23.7	74.7
1	3	026F	32	29.7	34.7
1	5	02AE	32	28	37.3
1	7	02ED	32	26.6	40.2
1	9	032C	32	25.3	43.6
1	11	036B	32	24.1	47.7
1	13	03AA	32	23	52.5
1	15	03E9	32	22	58.6
2	3	046E	32	28	37.3
2	5	04AC	32	25.3	43.6
2	7	04EA	32	23	52.5
2	9	0528	32	21.1	66.1

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
3	3	066D	32	26.6	40.2
3	5	06AA	32	23	52.5
3	7	06E7	32	20.3	75.9
4	3	086C	32	25.3	43.6
4	5	08A8	32	21.1	66.1
5	3	0A6B	32	24.1	47.7
6	3	0C6A	32	23	52.5
7	3	0E69	32	22	58.6
8	3	1068	32	21.1	66.1
9	3	1267	32	20.3	75.9

4 Interrupt Vector Table

This section shows the allocation of interrupt and interrupt vector/interrupt register.

Interrupt	Interrupt number		Interrupt level[*1]		Interrupt vector[*2]		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
Reset	0	00	-	-	0x3FC	0x000FFFFC	
Mode vector	1	01	-	-	0x3F8	0x000FFFF8	
System reserved	2	02	-	-	0x3F4	0x000FFFF4	
System reserved	3	03	-	-	0x3F0	0x000FFFF0	
System reserved	4	04	-	-	0x3EC	0x000FFFEC	
CPU supervisor mode (INT #5 instruction) [*6]	5	05	-	-	0x3E8	0x000FFFE8	
Memory Protection exception [*6]	6	06	-	-	0x3E4	0x000FFFE4	
Co-processor fault trap [*5]	7	07	-	-	0x3E0	0x000FFFE0	
Co-processor error trap [*5]	8	08	-	-	0x3DC	0x000FFFDC	
INTE instruction [*5]	9	09	-	-	0x3D8	0x000FFFD8	
Instruction break exception [*5]	10	0A	-	-	0x3D4	0x000FFFD4	

Interrupt	Interrupt number		Interrupt level[*1]		Interrupt vector[*2]		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
Operand break trap [*5]	11	0B	-	-	0x3D0	0x000FFFD0	
Step trace trap [*5]	12	0C	-	-	0x3CC	0x000FFFCC	
NMI interrupt (tool)[*5]	13	0D	-	-	0x3C8	0x000FFFC8	
Undefined instruction exception	14	0E	-	-	0x3C4	0x000FFFC4	
NMI request	15	0F	F_H fixed		0x3C0	0x000FFFC0	
External Interrupt 0	16	10	ICR00	0x440	0x3BC	0x000FFFBC	0, 16
External Interrupt 1	17	11			0x3B8	0x000FFFB8	1, 17
External Interrupt 2	18	12	ICR01	0x441	0x3B4	0x000FFFB4	2, 18
External Interrupt 3	19	13			0x3B0	0x000FFFB0	3, 19
External Interrupt 4	20	14	ICR02	0x442	0x3AC	0x000FFFAC	20
External Interrupt 5	21	15			0x3A8	0x000FFFA8	21
External Interrupt 6	22	16	ICR03	0x443	0x3A4	0x000FFFA4	22
External Interrupt 7	23	17			0x3A0	0x000FFFA0	23
reserved	24	18	ICR04	0x444	0x39C	0x000FFF9C	
reserved	25	19			0x398	0x000FFF98	
reserved	26	1A	ICR05	0x445	0x394	0x000FFF94	
reserved	27	1B			0x390	0x000FFF90	

Interrupt	Interrupt number		Interrupt level[*1]		Interrupt vector[*2]		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
External Interrupt 12	28	1C	ICR06	0x446	0x38C	0x000FFF8C	
reserved	29	1D			0x388	0x000FFF88	
External Interrupt 14	30	1E	ICR07	0x447	0x384	0x000FFF84	
reserved	31	1F			0x380	0x000FFF80	
Reload Timer 0	32	20	ICR08	0x448	0x37C	0x000FFF7C	4, 32
Reload Timer 1	33	21			0x378	0x000FFF78	5, 33
Reload Timer2	34	22	ICR09	0x449	0x374	0x000FFF74	34
Reload Timer 3	35	23			0x370	0x000FFF70	35
Reload Timer 4	36	24	ICR10	0x44A	0x36C	0x000FFF6C	36
Reload Timer 5	37	25			0x368	0x000FFF68	37
Reload Timer 6	38	26	ICR11	0x44B	0x364	0x000FFF64	38
Reload Timer 7	39	27			0x360	0x000FFF60	39
Free Run Timer 0	40	28	ICR12	0x44C	0x35C	0x000FFF5C	40
Free Run Timer 1	41	29			0x358	0x000FFF58	41
Free Run Timer 2	42	2A	ICR13	0x44D	0x354	0x000FFF54	42
Free Run Timer 3	43	2B			0x350	0x000FFF50	43
Free Run Timer 4	44	2C	ICR14	0x44E	0x34C	0x000FFF4C	44
Free Run Timer 5	45	2D			0x348	0x000FFF48	45

Interrupt	Interrupt number		Interrupt level[*1]		Interrupt vector[*2]		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
Free Run Timer 6	46	2E	ICR15	0x44F	0x344	0x000FFF44	46
Free Run Timer 7	47	2F			0x340	0x000FFF40	47
reserved	48	30	ICR16	0x450	0x33C	0x000FFF3C	
reserved	49	31			0x338	0x000FFF38	
reserved	50	32	ICR17	0x451	0x334	0x000FFF34	
reserved	51	33			0x330	0x000FFF30	
CAN 4	52	34	ICR18	0x452	0x32C	0x000FFF2C	
reserved	53	35			0x328	0x000FFF28	
USART (LIN) 0 RX	54	36	ICR19	0x453	0x324	0x000FFF24	6, 48
USART (LIN) 0 TX	55	37			0x320	0x000FFF20	7, 49
USART (LIN) 1 RX	56	38	ICR20	0x454	0x31C	0x000FFF1C	8, 50
USART (LIN) 1 TX	57	39			0x318	0x000FFF18	9, 51
USART (LIN) 2 RX	58	3A	ICR21	0x455	0x314	0x000FFF14	52
USART (LIN) 2 TX	59	3B			0x310	0x000FFF10	53
USART (LIN) 3 RX	60	3C	ICR22	0x456	0x30C	0x000FFF0C	54
USART (LIN) 3 TX	61	3D			0x308	0x000FFF08	55
System reserved	62	3E	ICR23 [*4]	0x457	0x304	0x000FFF04	
Delayed Interrupt	63	3F			0x300	0x000FFF00	

Interrupt	Interrupt number		Interrupt level[*1]		Interrupt vector[*2]		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
System reserved [*3]	64	40	(ICR24)	(0x458)	0x2FC	0x000FFEFC	
System reserved [*3]	65	41			0x2F8	0x000FFEF8	
USART (LIN FIFO) 4 RX	66	42	ICR25	0x459	0x2F4	0x000FFEF4	10, 56
USART (LIN FIFO) 4 TX	67	43			0x2F0	0x000FFEF0	11, 57
reserved	68	44	ICR26	0x45A	0x2EC	0x000FFEEC	12, 58
reserved	69	45			0x2E8	0x000FFEE8	13, 59
reserved	70	46	ICR27	0x45B	0x2E4	0x000FFEE4	60
reserved	71	47			0x2E0	0x000FFEE0	61
reserved	72	48	ICR28	0x45C	0x2DC	0x000FFEDC	62
reserved	73	49			0x2D8	0x000FFED8	63
I2C 0	74	4A	ICR29	0x45D	0x2D4	0x000FFED4	
reserved	75	4B			0x2D0	0x000FFED0	
reserved	76	4C	ICR30	0x45E	0x2CC	0x000FFECC	64
reserved	77	4D			0x2C8	0x000FFEC8	65
reserved	78	4E	ICR31	0x45F	0x2C4	0x000FFEC4	66
reserved	79	4F			0x2C0	0x000FFEC0	67
reserved	80	50	ICR32	0x460	0x2BC	0x000FFEBC	68

Interrupt	Interrupt number		Interrupt level[*1]		Interrupt vector[*2]		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
reserved	81	51			0x2B8	0x000FFEB8	69
reserved	82	52	ICR33	0x461	0x2B4	0x000FFEB4	70
reserved	83	53			0x2B0	0x000FFEB0	71
reserved	84	54	ICR34	0x462	0x2AC	0x000FFEAC	72
reserved	85	55			0x2A8	0x000FFEA8	73
reserved	86	56	ICR35	0x463	0x2A4	0x000FFEA4	74
reserved	87	57			0x2A0	0x000FFEA0	75
reserved	88	58	ICR36	0x464	0x29C	0x000FFE9C	76
reserved	89	59			0x298	0x000FFE98	77
reserved	90	5A	ICR37	0x465	0x294	0x000FFE94	78
reserved	91	5B			0x290	0x000FFE90	79
Input Capture 0	92	5C	ICR38	0x466	0x28C	0x000FFE8C	80
Input Capture 1	93	5D			0x288	0x000FFE88	81
Input Capture 2	94	5E	ICR39	0x467	0x284	0x000FFE84	82
Input Capture 3	95	5F			0x280	0x000FFE80	83
Input Capture 4	96	60	ICR40	0x468	0x27C	0x000FFE7C	84
Input Capture 5	97	61			0x278	0x000FFE78	85
Input Capture 6	98	62	ICR41	0x469	0x274	0x000FFE74	86

Interrupt	Interrupt number		Interrupt level[*1]		Interrupt vector[*2]		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
Input Capture 7	99	63			0x270	0x000FFE70	87
Output Compare 0	100	64	ICR42	0x46A	0x26C	0x000FFE6C	88
Output Compare 1	101	65			0x268	0x000FFE68	89
Output Compare 2	102	66	ICR43	0x46B	0x264	0x000FFE64	90
Output Compare 3	103	67			0x260	0x000FFE60	91
Output Compare 4	104	68	ICR44	0x46C	0x25C	0x000FFE5C	92
Output Compare 5	105	69			0x258	0x000FFE58	93
reserved	106	6A	ICR45	0x46D	0x254	0x000FFE54	94
reserved	107	6B			0x250	0x000FFE50	95
reserved	108	6C	ICR46	0x46E	0x24C	0x000FFE4C	
reserved	109	6D			0x248	0x000FFE48	
System reserved	110	6E	ICR47 [*4]	0x46F	0x244	0x000FFE44	
System reserved	111	6F			0x240	0x000FFE40	
Prog. Pulse Gen. 0	112	70	ICR48	0x470	0x23C	0x000FFE3C	15, 96
Prog. Pulse Gen. 1	113	71			0x238	0x000FFE38	97
Prog. Pulse Gen. 2	114	72	ICR49	0x471	0x234	0x000FFE34	98
Prog. Pulse Gen. 3	115	73			0x230	0x000FFE30	99
Prog. Pulse Gen. 4	116	74	ICR50	0x472	0x22C	0x000FFE2C	100

Interrupt	Interrupt number		Interrupt level[*1]		Interrupt vector[*2]		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
Prog. Pulse Gen. 5	117	75			0x228	0x000FFE28	101
Prog. Pulse Gen. 6	118	76	ICR51	0x473	0x224	0x000FFE24	102
Prog. Pulse Gen. 7	119	77			0x220	0x000FFE20	103
Prog. Pulse Gen. 8	120	78	ICR52	0x474	0x21C	0x000FFE1C	104
Prog. Pulse Gen. 9	121	79			0x218	0x000FFE18	105
reserved	122	7A	ICR53	0x475	0x214	0x000FFE14	106
reserved	123	7B			0x210	0x000FFE10	107
reserved	124	7C	ICR54	0x476	0x20C	0x000FFE0C	108
reserved	125	7D			0x208	0x000FFE08	109
reserved	126	7E	ICR55	0x477	0x204	0x000FFE04	110
reserved	127	7F			0x200	0x000FFE00	111
reserved	128	80	ICR56	0x478	0x1FC	0x000FFDFC	
reserved	129	81			0x1F8	0x000FFDF8	
reserved	130	82	ICR57	0x479	0x1F4	0x000FFDF4	
reserved	131	83			0x1F0	0x000FFDF0	
Real Time Clock	132	84	ICR58	0x47A	0x1EC	0x000FFDEC	

Interrupt	Interrupt number		Interrupt level[*1]		Interrupt vector[*2]		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
Calibration Unit	133	85			0x1E8	0x000FFDE8	
A/D Converter 0	134	86	ICR59	0x47B	0x1E4	0x000FFDE4	14, 112
reserved	135	87			0x1E0	0x000FFDE0	
	136	88	ICR60	0x47C	0x1DC	0x000FFDDC	
reserved	137	89			0x1D8	0x000FFDD8	
Low Voltage Detection	138	8A	ICR61	0x47D	0x1D4	0x000FFDD4	
reserved	139	8B			0x1D0	0x000FFDD0	
Timebase Overflow	140	8C	ICR62	0x47E	0x1CC	0x000FFDCC	
PLL Clock Gear	141	8D			0x1C8	0x000FFDC8	
DMA Controller	142	8E	ICR63	0x47F	0x1C4	0x000FFDC4	
Main/Sub OSC stability wait	143	8F			0x1C0	0x000FFDC0	
Security vector	144	90	-	-	0x1BC	0x000FFDBC	
Used by the INT instruction.	145 to 255	91 to FF	-	-	0x1B8 to 0x000	0x000FFDB8 to 0x000FFC00	

Notes:

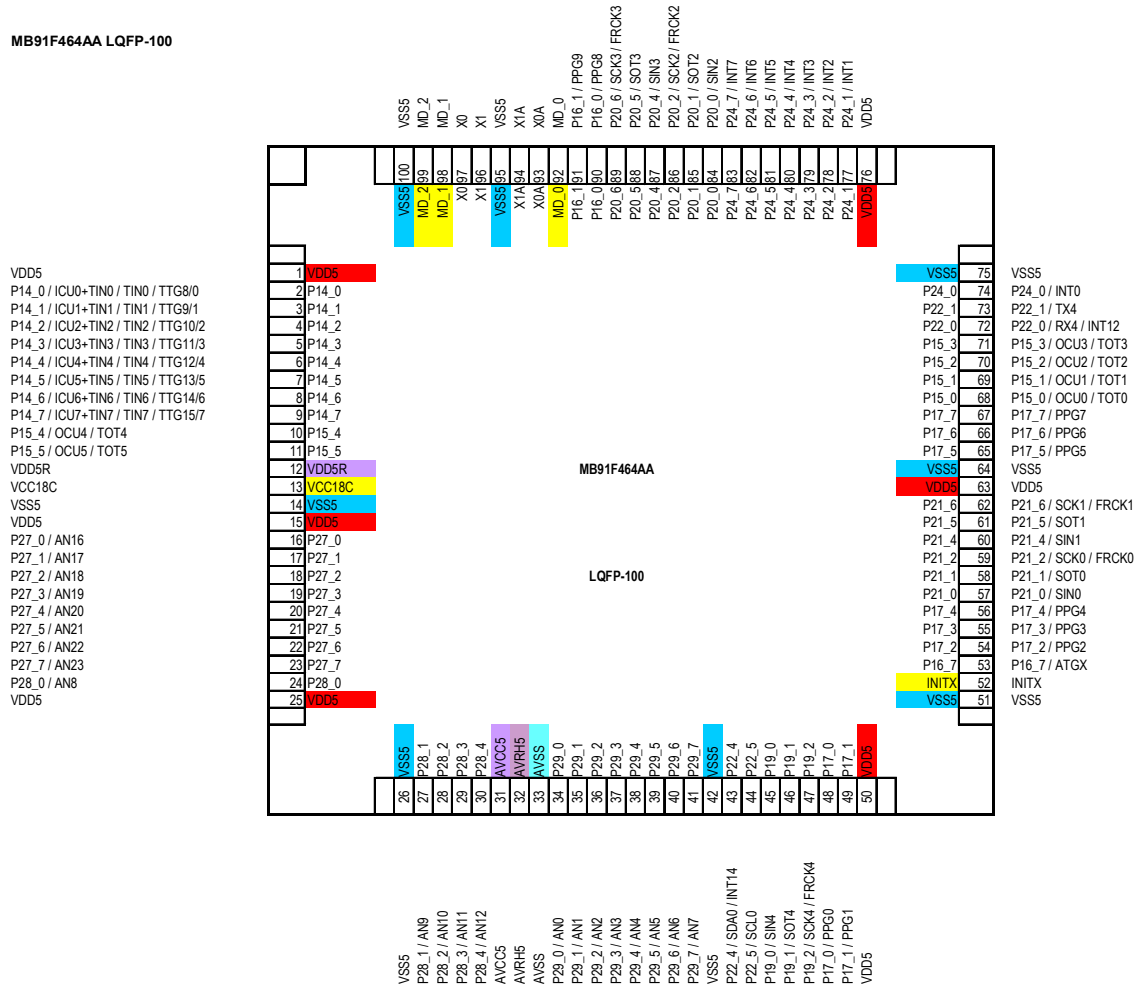
[*1] The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00). The TBR is initialized to this value by a reset. After execution of the internal boot ROM TBR is set to 0x000FFC00.
*3 Used by REALOS
*4 ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0x0C03 : IOS[0])
*5 System reserved
*6 Memory Protection Unit (MPU) support

5 Package and Pin Assignment

5.1 Package

A LQFP-100 package will be used for MB91F464AA. The package code is FPT-100P-M20 (100-pin plastic QFP, lead pitch: 0.50 mm, size 14 mm x 14 mm, Theta-ja = 30 degr. C / W)



5.2 I/O Pins and Their Functions

Pin Number	Name	PFR=1	EPFR=1	Special	Pad Type	Description
96	X1	-	-	-	TO00_1	4 MHz Quarz Oscillator
97	X0	-	-	-	TO00_0	
94	X1A	-	-	-	TO01_1	32 kHz Quarz Oscillator
93	X0A	-	-	-	TO01_0	
9	P14_7	ICU7+TIN7	TIN7	TTG15/7	TP04_0	
8	P14_6	ICU6+TIN6	TIN6	TTG14/6	TP04_0	General Purpose Port 14
7	P14_5	ICU5+TIN5	TIN5	TTG13/5	TP04_0	
6	P14_4	ICU4+TIN4	TIN4	TTG12/4	TP04_0	ICU: Input Capture Unit event input
5	P14_3	ICU3+TIN3	TIN3	TTG11/3	TP04_0	TIN: Reload Timer external trigger input
4	P14_2	ICU2+TIN2	TIN2	TTG10/2	TP04_0	TTG: PPG external trigger input
3	P14_1	ICU1+TIN1	TIN1	TTG9/1	TP04_0	
2	P14_0	ICU0+TIN0	TIN0	TTG8/0	TP04_0	
11	P15_5	OCU5	TOT5	-	TP04_0	
10	P15_4	OCU4	TOT4	-	TP04_0	General Purpose Port 15
71	P15_3	OCU3	TOT3	-	TP04_0	OCU: Output Compare waveform output
70	P15_2	OCU2	TOT2	-	TP04_0	TOT: Reload Timer output
69	P15_1	OCU1	TOT1	-	TP04_0	
68	P15_0	OCU0	TOT0	-	TP04_0	
53	P16_7	--	ATGX	-	TP04_0	General Purpose Port 16
91	P16_1	PPG9	--	-	TP04_0	ATGX: ADC external trigger
90	P16_0	PPG8	--	-	TP04_0	PPG: PPG waveform output
67	P17_7	PPG7	-	-	TP04_0	
66	P17_6	PPG6	-	-	TP04_0	
65	P17_5	PPG5	-	-	TP04_0	General Purpose Port 17
56	P17_4	PPG4	-	-	TP04_0	
55	P17_3	PPG3	-	-	TP04_0	PPG: PPG waveform output
54	P17_2	PPG2	-	-	TP04_0	
49	P17_1	PPG1	-	-	TP04_0	
48	P17_0	PPG0	-	-	TP04_0	
47	P19_2	SCK4	FRCK4	-	TP04_0	General Purpose Port 19
46	P19_1	SOT4	--	-	TP04_0	SCK, SOT, SIN, FRCK see below
45	P19_0	SIN4	--	-	TP04_0	
89	P20_6	SCK3	FRCK3	-	TP04_0	
88	P20_5	SOT3	--	-	TP04_0	General Purpose Port 20
87	P20_4	SIN3	--	-	TP04_0	FRCK: Free Run Timer external clock input
86	P20_2	SCK2	FRCK2	-	TP04_0	SCK: LIN-USART serial clock in/out
85	P20_1	SOT2	--	-	TP04_0	SOT: LIN-USART serial data output
84	P20_0	SIN2	--	-	TP04_0	SIN: LIN-USART serial data input

62	P21_6	SCK1	FRCK1	-	TP04_0	
61	P21_5	SOT1	--	-	TP04_0	General Purpose Port 21
60	P21_4	SIN1	--	-	TP04_0	FRCK: Free Run Timer external clock input
59	P21_2	SCK0	FRCK0	-	TP04_0	SCK: LIN-USART serial clock in/out
58	P21_1	SOT0	--	-	TP04_0	SOT: LIN-USART serial data output
57	P21_0	SIN0	--	-	TP04_0	SIN: LIN-USART serial data input
44	P22_5	SCL0	-	-	TP02_0	General Purpose Port 22
43	P22_4	SDA0	-	INT14	TP02_0	SCL, SDA: I2C Clock/Data in/out (open drain)
73	P22_1	TX4	-	-	TP04_0	TX, RX: CAN Transmit / Receive out/in
72	P22_0	RX4	-	INT12	TP04_0	INT: External Interrupt (I2C/CAN-Wakeup)
83	P24_7	INT7	-	--	TP04_0	
82	P24_6	INT6	-	--	TP04_0	
81	P24_5	INT5	-	--	TP04_0	
80	P24_4	INT4	-	--	TP04_0	General Purpose Port 24
79	P24_3	INT3	-	-	TP04_0	INT: External Interrupt input
78	P24_2	INT2	-	-	TP04_0	
77	P24_1	INT1	-	-	TP04_0	
74	P24_0	INT0	-	-	TP04_0	
23	P27_7	-	AN23	-	TP03_0	
22	P27_6	-	AN22	-	TP03_0	
21	P27_5	-	AN21	-	TP03_0	
20	P27_4	-	AN20	-	TP03_0	General Purpose Port 27
19	P27_3	-	AN19	-	TP03_0	AN: ADC Analog input
18	P27_2	-	AN18	-	TP03_0	
17	P27_1	-	AN17	-	TP03_0	
16	P27_0	-	AN16	-	TP03_0	
30	P28_4	AN12	-	-	TP03_0	
29	P28_3	AN11	-	-	TP03_0	
28	P28_2	AN10	-	-	TP03_0	General Purpose Port 28
27	P28_1	AN9	-	-	TP03_0	AN: ADC Analog input
24	P28_0	AN8	-	-	TP03_0	
41	P29_7	AN7	-	-	TP03_0	
40	P29_6	AN6	-	-	TP03_0	
39	P29_5	AN5	-	-	TP03_0	
38	P29_4	AN4	-	-	TP03_0	General Purpose Port 29
37	P29_3	AN3	-	-	TP03_0	AN: ADC Analog input
36	P29_2	AN2	-	-	TP03_0	
35	P29_1	AN1	-	-	TP03_0	
34	P29_0	AN0	-	-	TP03_0	
52	INITX	-	-	-	TC02_0	Initialization input (low active)
99	MD_2	-	-	-	TC01_0	
98	MD_1	-	-	-	TC01_0	Device Mode inputs
92	MD_0	-	-	-	TC01_0	
1	VDD5	-	-	-	TS02_0	Power Supply 5 Volt

15	VDD5	-	-	-	TS02_0	
25	VDD5	-	-	-	TS02_0	
50	VDD5	-	-	-	TS02_0	
63	VDD5	-	-	-	TS02_0	
76	VDD5	-	-	-	TS02_0	
14	VSS5	-	-	-	TS00_0	Ground Supply
26	VSS5	-	-	-	TS00_0	
42	VSS5	-	-	-	TS00_0	
51	VSS5	-	-	-	TS00_0	
64	VSS5	-	-	-	TS00_0	
75	VSS5	-	-	-	TS00_0	
95	VSS5	-	-	-	TS00_0	
100	VSS5	-	-	-	TS00_0	
31	AVCC5	-	-	-	TA03_0	Analog Power Supply 5 Volt
32	AVRH5	-	-	-	TA01_0	Analog High Reference, up to 5 Volt
33	AVSS	-	-	-	TA00_0	Analog Ground Supply
12	VDD5R	-	-	-	TA00_0	Voltage Regulator Supply 5 Volt
13	VCC18C	-	-	-	TA10_0	Voltage Regulator Capacitance pin

5.3 I/O Pin Types

Pin Type	Pull Up/ Down	Input Type	STOP control	Output Driver	Comment
TP02_0	U/D control	CH / A / TTL / CH2	Stop	3 mA	I2C Pin (open drain if PFR=1)
TP03_0	U/D control	CH / A / TTL / CH2	Stop	2/5 mA	General Purpose I/O with 1 analog input line
TP04_0	U/D control	CH / A / TTL / CH2	Stop	2/5 mA	General Purpose I/O
TP05_0	U/D control	CH / A / TTL / CH2	Stop	2/5/30 mA	General Purpose I/O, 30mA SMC, 2 analog lines
TP05_1	U/D control	CH / A / TTL / CH2	Stop	2/5/30 mA	General Purpose I/O, 30mA SMC, 1 analog line
TC01_0	-	C2	no	-	Mode Pin
TC02_0	Up	C2	no	-	INITX
TC10_0	-	-	no	5 mA	Output port 5mA for MONCLK

Notes:

- The pull-up / pull-down resistors are typical 50 kOhm. The controlled pull-up/down's can be enabled by register setting.
- Input Types: CH CMOS Schmitt trigger
  CH2 CMOS Schmitt trigger 2
  A CMOS Automotive Schmitt trigger
  TTL TTL
  (for input high/low voltages, please see section Operating Conditions)
- Stop control: Switch to HiZ in STOP mode by register setting, and disable input lines in STOP if the port is not configuerd to be external interrupt input.
- Default output driver strength is 3 mA (I2C pins) and 5 mA (all other pins).

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter	Symbol	min.	max.	Unit	Condition
Digital supply voltage	VDD-VSS	-0.3	6.0	V	
Storage temperature	T_{ST}	-55	125	°C	
Power consumption	P_{TOT}		1000	mW	T_A = 25°C
Digital input voltage	V_{IDIG}	VSS-0.3 *	VDD+0.3	V	
Analog input voltage	V_{IA}	AVSS-0.3 *	AVCC+0.3	V	AVCC=AVRH
Analog supply voltage	AVCC-AVSS	-0.3	5.8	V	
Analog reference voltage	AVRH-AVSS	-0.3	5.8	V	
Static DC current into digital I/O	$I_{I/ODC}$	-2	2	mA	$\Sigma I_{I/ODC} < I_{SRUN}$
Relationship of the supply voltages	AVCC	VDD - 0.3 VSS - 0.3	VDD + 0.3 VDD + 0.3	V V	At least one pin of the ports 26 - 29 (AN*) is used as digital input or output All pins of the ports 26 - 29 (AN*) follow the condition of V_{IA}

***** Making full use of the allowed static DC current into digital I/Os will lead to lower values here.

6.2 Operating Conditions

Parameter	**Symbol**	**min.**	**typ.**	**max.**	**Unit**	**Condition**
Operating temperature	T_{OP}	-40		105	°C	
Supply voltage - Digital supply	VDD5-VSS	3.0		5.5	V	Internal voltage reg. VDD_{CORE} =1.8V
- Analog supply	AVCC-AVSS	3.0		5.5	V	AVSS=0V

Current consumption						
-Run mode, flash unused	I_{srun}		80		mA	f = 80 MHz (1.0 mA/MHz)
-Run mode, flash accessed	I_{srun}		110		mA	f = 80 MHz (1.3 mA/MHz +5 mA)
- Sleep mode	I_{sSLEEP}		40		mA	f = 80 MHz (0.5 mA/MHz)
-RTC mode	I_{sRTC}		100		µA	f = 4MHz, T_A =25 ºC
			40		µA	f ≤ 100kHz, T_A =25 ºC
			500		µA	f = 4MHz, T_A =105 ºC
			250		µA	f ≤ 100kHz, T_A =105 ºC
-Stop mode	I_{sstop}		30		µA	T_A =25 ºC
			200		µA	T_A =105 ºC
Digital Inputs [1)]						
CMOS Schmitt-Trigger:						
- High voltage range	V_{IH}	0.7*VDD		VDD	V	all voltage ranges valid at
- Low voltage range	V_{IL}	VSS		0.3*VDD	V	4.5V ≤ VDD ≤ 5.5V
CMOS Schmitt-Trigger 2:						
- High voltage range	V_{IH}	0.8*VDD		VDD	V	
- Low Voltage range	V_{IL}	VSS		0.2*VDD	V	
CMOS Automotive Schmitt-Trigger:						
- High voltage range	V_{IH}	0.8*VDD		VDD	V	
- Low voltage range	V_{IL}	VSS		0.5*VDD	V	
- hysteresis voltage		0.2		0.5	V	
TTL:						
- High voltage range	V_{IH}	2.0		VDD	V	
- Low voltage range	V_{IL}	VSS		0.8	V	
all inputs:						
- Input capacitance	C_{IN}			tbd	pF	
- Input leakage current	I_{IL}	-1		1	µA	T_A =25 ºC
- Pull up resistor	R_{up}		50		kΩ	
- Pull down resistor	R_{down}		50		kΩ	
Digital outputs						4.5V ≤ VDD ≤ 5.5V
- Output "H" voltage	V_{OH}	VDD-0.5		VDD	V	I_{load} = ±2mA / ±5mA
- Output "L" voltage	V_{OL}	VSS		VSS+0.4	V	3.0V ≤ VDD ≤ 4.5V I_{load} = ±1.6mA/ ±3mA
Digital outputs I^2C Port						4.5V ≤ VDD ≤ 5.5V
- Output "H" voltage	V_{OH}	VDD-0.5		VDD	V	I_{load} = ±3 mA
- Output "L" voltage	V_{OL}	VSS		VSS+0.4	V	3.0V ≤ VDD ≤ 4.5V I_{load} = ±2mA

ADC inputs [2]						
- Reference voltage input	AVRH AVRL	AVCC*0.75 AVSS		AVCC AVCC*0.25	V V	
- Input voltage range	V_{imax} V_{imin}	 AVRL		AVRH	V V	
- Input resistance	R_I			2.6 12.1	kΩ kΩ	4.5V < AVCC < 5.5V 3.0V < AVCC < 4.5V
- Input capacitance	C_I			8.5	pF	
- Impedance of external output driving the ADC input				100	kΩ	
- Input leakage current	I_{IL}	-1		1	µA	T_A =25 ºC
I²C Bus Interface						
- Output voltage	V_{OH} V_{OL}	- VSS		VDD VSS+0.4	V V	Open Drain Output I_{load} = 3mA
- Output current	I_{out}	3			mA	
Lock-up time PLL1 (4MHz->16…100MHz)			0.1	0.2	ms	
ESD Protection (Human body model)	V_{surge}	2			kV	$R_{discharge}$=1.5kΩ $C_{discharge}$= 100pF
RC Oscillator	$f_{RC100KHz}$ f_{RC2MHz}	50 1	100 2	200 4	kHz MHz	VDD_{CORE} ≥1.65V

[1] valid for bidirectional tristate I/O PAD cell

[2] The protection diodes at the analog inputs are connected to the digital supply voltage

6.3 Converter Characteristics

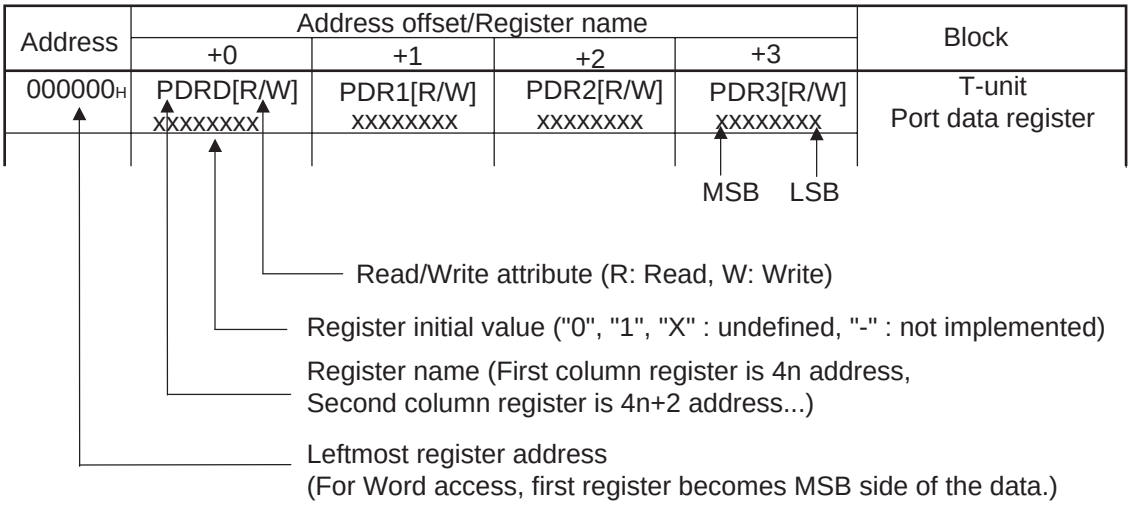
- A/D Converter

Parameter	Symbol	Rating			Unit	Remark
		Minimum	Typical	Maximum		
Resolution				10	Bit	
Conversion error				+/- 3.0	LSB	Overall error
Non-linearity				+/-2.5	LSB	
Differential Non-linearity				+/-1.9	LSB	
Zero Reading voltage	V_{0T}	AVRL -1.5	AVRL+0.5	AVRL+2.5	LSB	
Full scale reading voltage	V_{FST}	AVRH-3.5	AVRH-1.5	AVRH+0.5	LSB	
Input current	IA @ AVCC		2.4	4.7	mA	
Reference voltage current	IR		0.65	1.0	mA	

7 I/O Map

This section shows the association between memory space and each register of peripheral resources.

• Table convention:



Note: Bit value of register shows initial values as follows.

- "1": Initial value is "1".
- "0": Initial value is "0".
- "X": Initial value is indeterminate.
- "-": No physical register exists in the position.

Do not use other data access attributes to access data.

Table 6-1 I/O Map

Address	Register				Block
	+0	+1	+2	+3	
000000_H - 000008H	reserved				
$00000C_H$	res.	res.	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] - - XXXXXX	R-bus Port Data Register
000010_H	PDR16 [R/W] X - - - - - XX	PDR17 [R/W] XXXXXXXX	res.	PDR19 [R/W] - - - - - XXX	
000014_H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] - XXX - XXX	PDR22 [R/W] - - XX - - XX	res.	
000018_H	PDR24 [R/W] XXXXXXXX	res.	res.	PDR27 [R/W] XXXXXXXX	
$00001C_H$	PDR28 [R/W] - - - XXXXX	PDR29 [R/W] XXXXXXXX	res.	res.	
000020_H - $00002C_H$	reserved				
000030_H	EIRR0 [R/W] 00000000	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		Ext. INT 0-7 NMI
000034_H	EIRR1 [R/W] 00000000	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		Ext. INT 8-15
000038_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	RBSYNC *1		DLYI/I-unit
$00003C_H$	reserved				
000040_H	SCR00 [R/W,W] 00000000	SMR00 [R/W,W] 00000000	SSR00 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	USART (LIN) 0
000044_H	ESCR00 [R/W] 00000X00	ECCR00 [R/W,R,W] -00000XX	res.		
000048_H	SCR01 [R/W,W] 00000000	SMR01 [R/W,W] 00000000	SSR01 [R/W,R] 00001000	RDR01/TDR01 [R/W] 00000000	USART (LIN) 1

Address	Register				Block
	+0	+1	+2	+3	
$00004C_H$	ESCR01 [R/W] 00000X00	ECCR01 [R/W,R,W] -00000XX	res.		USART (LIN) 1
000050_H	SCR02 [R/W,W] 00000000	SMR02 [R/W,W] 00000000	SSR02 [R/W,R] 00001000	RDR02/TDR02 [R/W] 00000000	USART (LIN) 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W,R,W] -00000XX	res.		
000058_H	SCR03 [R/W,W] 00000000	SMR03 [R/W,W] 00000000	SSR03 [R/W,R] 00001000	RDR03/TDR03 [R/W] 00000000	USART (LIN) 3
$00005C_H$	ESCR03 [R/W] 00000X00	ECCR03 [R/W,R,W] -00000XX	res.		
000060_H	SCR04 [R/W,W] 00000000	SMR04 [R/W,W] 00000000	SSR04 [R/W,R] 00001000	RDR04/TDR04 [R/W] 00000000	USART (LIN) 4 with FIFO
000064_H	ESCR04 [R/W] 00000X00	ECCR04 [R/W,R,W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068_H - $00007C_H$	reserved				
000080_H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	BGR101 [R/W] 00000000	BGR001 [R/W] 00000000	Baudrate Generator USART (LIN) 0-7
000084_H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088_H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	res.	res.	
$00008C_H$ - $0000CC_H$	reserved				
$0000D0_H$	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I2C 0
$0000D4_H$	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
$0000D8_H$	res.	IDAR0 [R/W] 00000000	ICCR0 [R/W] - 0011111	res.	

Address	Register				Block
	+0	+1	+2	+3	
$0000DC_H$ - $0000FC_H$	reserved				
000100_H	GCN10 [R/W] 00110010 00010000		res.	GCN20 [R/W] - - - - 0000	PPG Control 0-3
000104_H	GCN11 [R/W] 00110010 00010000		res.	GCN21 [R/W] - - - - 0000	PPG Control 4-7
000108_H	GCN12 [R/W] 00110010 00010000		res.	GCN22 [R/W] - - - - 0000	PPG Control 8-11
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160_H - $00017C_H$	reserved				
000180_H	res.	ICS01 [R/W] 00000000	res.	ICS23 [R/W] 00000000	Input Capture 0-3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0-3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H - $00019C_H$	reserved				

Address	Register				Block
	+0	+1	+2	+3	
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	reserved				
$0001B0_H$	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
$0001B4_H$	res.		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
$0001B8_H$	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
$0001BC_H$	res.		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	
$0001C0_H$	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4-5)
$0001C4_H$	res.		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	
$0001C8_H$	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6-7)
$0001CC_H$	res.		TMCSRH3 [R/W] - - - 00000	TMCSRL3 [R/W] 0 - 000000	
$0001D0_H$	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8-9)
$0001D4_H$	res.		TMCSRH4 [R/W] - - - 00000	TMCSRL4 [R/W] 0 - 000000	

Address	Register				Block
	+0	+1	+2	+3	
$0001D8_H$	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10-11)
$0001DC_H$	res.		TMCSRH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
$0001E0_H$	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12-13)
$0001E4_H$	res.		TMCSRH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
$0001E8_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14-15) (ADC)
$0001EC_H$	res.		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
$0001F0_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0-1)
$0001F4_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2-3)
$0001F8_H$	TCDT2 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0-1)
$0001FC_H$	TCDT3 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2-3)

Address	Register				Block
	+0	+1	+2	+3	
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H - $00023C_H$	reserved				
000240_H	DMACR [R/W] 00 - - 0000	reserved			
000244_H - $00024C_H$	reserved				
000250_H	reserved				
000254_H	reserved				
000258_H - $0002CC_H$	reserved				

Address	Register				Block
	+0	+1	+2	+3	
$0002D0_H$	res.	ICS045 [R/W] 00000000	res.	ICS67 [R/W] 00000000	Input Capture 4-7
$0002D4_H$	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
$0002D8_H$	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
$0002DC_H$	OCS45 [R/W] - - - 0 - - 00 0000 - - 00		reserved		Output Compare 4-5
$0002E0_H$	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
$0002E4_H$ - $0002EC_H$	reserved				
$0002F0_H$	TCDT4 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4-5)
$0002F4_H$	TCDT5 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6-7)
$0002F8_H$	TCDT6 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS6 [R/W] 00000000	Free Running Timer 6
$0002FC_H$	TCDT7 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS7 [R/W] 00000000	Free Running Timer 7
000300_H - $00038C_H$	reserved				
000390_H	ROMS [R] 11111111 01000011		res.		ROM Select Register
000394_H - $0003EC_H$	reserved				

Address	Register				Block
	+0	+1	+2	+3	
$0003F0_H$	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
$0003F4_H$	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400_H - $00043C_H$	reserved				
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control Unit
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
$00044C_H$	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450_H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454_H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
$00045C_H$	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460_H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464_H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468_H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	

Address	Register				Block
	+0	+1	+2	+3	
00046C$_H$	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470$_H$	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474$_H$	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478$_H$	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
00047C$_H$	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	
000480$_H$	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] X0000X00	CTBR [W] XXXXXXXX	Clock Control Unit
000484$_H$	CLKR [R/W] 00000000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488$_H$	res.	res.	res.	res.	
00048C$_H$	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [W] 00000000	PLL Clock Gear Unit
000490$_H$	PLLCTRL [R/W] - - - - 0000	res.	res.	res.	
000494$_H$	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control
000498$_H$	PORTEN [R/W] - - - - - - 00	res.	res.	res.	Port Input Enable Control
0004A0$_H$	res.	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
0004A4$_H$	res.	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
0004A8$_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	res.	
0004AC$_H$	CSVTR [R/W] - - - 00010	CSVCR [R/W] 00011100	CSCFG [R/W] 0X000000	res.	Clock-Supervisor / Selector

Address	Register				Block
	+0	+1	+2	+3	
$0004B0_H$	CUCR [R/W] - - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration Unit of Sub Oscillation
$0004B4_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
$0004B8_H$	CMPR [R/W] - - 000010 11111101		res.	CMCR [R/W] - 001 - - 00	Clock Modulation
$0004BC_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
$0004C0_H$	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - - 0 - - - -	res.	res.	CAN Clock Control
$0004C4_H$	LVSEL [R/W] 00000111	LVDET [R/W] 00000-00	HWWDE [R/W] - - - - - - 00	HWWD [R/W,W] 00011000	LV Detection / Hardware-Watchdog
$0004C8_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 00 - - - 000	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilisation Timer
$0004CC_H$	OSCCR [R/W] - - - - - - - 0	res.	REGSEL [R/W] - - 000110	REGCTR [R/W] - - - 0 - - 00	Main-Oscillation Standby Control / Main/Sub Regulator Control
$0004D0_H$ - $000BFC_H$	reserved				
$000C00_H$	res.	res.	res.	res.	
$000C04_H$ - $000D08_H$	reserved				

Address	Register				Block
	+0	+1	+2	+3	
$000D0C_H$	res.	res.	PDRD14 [R] XXXXXXXX	PDRD15 [R] - - XXXXXX	R-bus Port Data Direct Read Register
000D10	PDRD16 [R] X - - - - - XX	PDRD17 [R] XXXXXXXX	res.	PDRD19 [R] - - - - - XXX	
$000D14_H$	PDRD20 [R] -XXX - XXX	PDRD21 [R] - XXX - XXX	PDRD22 [R] - - XX - - XX	res.	
$000D18_H$	PDRD24 [R] XXXXXXXX	res.	res.	PDRD27 [R] XXXXXXXX	
$000D1C_H$	PDRD28 [R] - - - XXXXX	PDRD29 [R] XXXXXXXX	res.	res.	
$000D20_H$ - $000D48_H$	reserved				
$000D4C_H$	res.	res.	DDR14 [R/W] 00000000	DDR15 [R/W] - - 000000	R-bus Port Direction Register
$000D50_H$	DDR16 [R/W] 0 - - - - - 00	DDR17 [R/W] 00000000	res.	DDR19 [R/W] - - - - - 000	
$000D54_H$	DDR20 [R/W] -000 - 000	DDR21 [R/W] - 000 - 000	DDR22 [R/W] - - 00 - - 00	res.	
$000D58_H$	DDR24 [R/W] 00000000	res.	res.	DDR27 [R/W] 00000000	
$000D5C_H$	DDR28 [R/W] - - - 00000	DDR29 [R/W] 00000000	res.	res.	
$000D60_H$ - $000D88_H$	reserved				
$000D8C_H$	res.	res.	PFR14 [R/W] 00000000	PFR15 [R/W] - - 000000	R-bus Port Function Register
$000D90_H$	PFR16 [R/W] 0 - - - - - 00	PFR17 [R/W] 00000000	res.	PFR19 [R/W] - - - - - 000	
$000D94_H$	PFR20 [R/W] - 000 - 000	PFR21 [R/W] - 000 - 000	PFR22 [R/W] - - 00 - - 00	res.	
$000D98_H$	PFR24 [R/W] 00000000	res.	res.	PFR27 [R/W] 00000000	
$000D9C_H$	PFR28 [R/W] - - - 00000	PFR29 [R/W] 00000000	res.	res.	

Address	Register				Block
	+0	+1	+2	+3	
$000DA0_H$ - $000DC8_H$	reserved				
$000DCC_H$	res.	res.	EPFR14 [R/W] 00000000	EPFR15 [R/W] - - 000000	R-bus Port Extra Function Register
$000DD0_H$	EPFR16 [R/W] 0 - - - - - - -	EPFR17 [R/W] - - - - - - - -	res.	EPFR19 [R/W] - - - - - 0 - -	
$000DD4_H$	EPFR20 [R/W] - 0 - - - 0 - -	EPFR21 [R/W] - 0 - - - 0 - -	EPFR22 [R/W] - - - - - - - -	res.	
$000DD8_H$	EPFR24 [R/W] - - - - - - - -	res.	res.	EPFR27 [R/W] 00000000	
$000DDC_H$	res.	EPFR29 [R/W] - - - - - - - -	res.	res.	
$000DE0_H$ - $000E08_H$	reserved				
$000E0C_H$	res.	res.	PODR14 [R/W] 00000000	PODR15 [R/W] - - 000000	R-bus Port Output Drive Select Register
$000E10_H$	PODR16 [R/W] 0 - - - - - 00	PODR17 [R/W] 00000000	res.	PODR19 [R/W] - - - - - 000	
$000E14_H$	PODR20 [R/W] - 000 - 000	PODR21 [R/W] - 000 - 000	PODR22 [R/W] - - 00 - - 00	res.	
$000E18_H$	PODR24 [R/W] 00000000	res.	res.	PODR27 [R/W] 00000000	
$000E1C_H$	PODR28 [R/W] - - - 00000	PODR29 [R/W] 00000000	res.	res.	
$000E20_H$ - $000E48_H$	reserved				
$000E4C_H$	res.	res.	PILR14 [R/W] 00000000	PILR15 [R/W] - - 000000	R-bus Port Input Level Select Register
$000E50_H$	PILR16 [R/W] 0 - - - - - 00	PILR17 [R/W] 00000000	res.	PILR19 [R/W] - - - - - 000	
$000E54_H$	PILR20 [R/W] - 000 - 000	PILR21 [R/W] - 000 - 000	PILR22 [R/W] - - 00 - - 00	res.	

Address	Register				Block
	+0	+1	+2	+3	
$000E58_H$	PILR24 [R/W] 00000000	res.	res.	PILR27 [R/W] 00000000	
$000E5C_H$	PILR28 [R/W] - - - 00000	PILR29 [R/W] 00000000	res.	res.	
$000E60_H$ - $000E88_H$	reserved				
$000E8C_H$	res.	res.	EPILR14 [R/W] 00000000	EPILR15 [R/W] - - 000000	R-bus Port Extra Input Level Select Register
$000E90_H$	EPILR16 [R/W] 0 - - - - - 00	EPILR17 [R/W] 00000000	res.	EPILR19 [R/W] - - - - - 000	
$000E94_H$	EPILR20 [R/W] - 000 - 000	EPILR21 [R/W] - 000 - 000	EPILR22 [R/W] - - 00 - - 00	res.	
$000E98_H$	EPILR24 [R/W] 00000000	res.	res.	EPILR27 [R/W] 00000000	
$000E9C_H$	EPILR28 [R/W] - - - 00000	EPILR29 [R/W] 00000000	res.	res.	
$000EA0_H$ - $000EC8_H$	reserved				
$000ECC_H$	res.	res.	PPER14 [R/W] 00000000	PPER15 [R/W] - - 000000	R-bus Port Pull-Up/Down Enable Register
$000ED0_H$	PPER16 [R/W] 0 - - - - - 00	PPER17 [R/W] 00000000	res.	PPER19 [R/W] - - - - - 000	
$000ED4_H$	PPER20 [R/W] - 000 - 000	PPER21 [R/W] - 000 - 000	PPER22 [R/W] - - 00 - - 00	res.	
$000ED8_H$	PPER24 [R/W] 00000000	res.	res.	PPER27 [R/W] 0000000	
$000EDC_H$	PPER28 [R/W] - - - 00000	PPER29 [R/W] 00000000	res.	res.	
$000EE0_H$ - $000F08_H$	reserved				

Address	Register				Block
	+0	+1	+2	+3	
$000F0C_H$	res.	res.	PPCR14 [R/W] 11111111	PPCR15 [R/W] - - 111111	R-bus Port Pull-Up/Down Control Register
$000F10_H$	PPCR16 [R/W] 1 - - - - - 11	PPCR17 [R/W] 11111111	res.	PPCR19 [R/W] - 1 - - - 111	
$000F14_H$	PPCR20 [R/W] - 111 - 111	PPCR21 [R/W] - 111 - 111	PPCR22 [R/W] - - 11 - - 11	res.	
$000F18_H$	PPCR24 [R/W] 11111111	res.	res.	PPCR27 [R/W] 11111111	
$000F1C_H$	PPCR28 [R/W] - - - 11111	PPCR29 [R/W] 11111111	res.	res.	
$000F20_H$ - $000F3C_H$	reserved				
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
001028_H - $006FFC_H$	reserved				
007000_H	FMCS [R/W] 01101000	FMCR [R] - - - 00000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ I-Cache Control Register
007004_H	FMWT [R/W] 11111111 11111111		FMWT2 [R] - 001 - - - -	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$ - $007FFC_H$	reserved				
008000_H - $00BFFC_H$	MB91F464AA Boot-ROM size is 4kB : $00B000_H$ - $00BFFC_H$ (instruction access is 1 waitcycle, data access is 1 waitcycle)				Boot ROM 16 kB
00C0000 - $00C3FC_H$	reserved				
$00C400_H$	CTRLR4 [R/W] 00000000 00000001		STATR4 [R/W] 00000000 00000000		CAN 4 Control Register
$00C404_H$	ERRCNT4 [R] 00000000 00000000		BTR4 [R/W] 00100011 00000001		
$00C408_H$	INTR4 [R] 00000000 00000000		TESTR4 [R/W] 00000000 X0000000		
$00C40C_H$	BRPE4 [R/W] 00000000 00000000		CBSYNC4 *2		

Address	Register				Block
	+0	+1	+2	+3	
$00C410_H$	IF1CREQ4 [R/W] 00000000 00000001		IF1CMSK4 [R/W] 00000000 00000000		CAN 4 IF 1 Register
$00C414_H$	IF1MSK24 [R/W] 11111111 11111111		IF1MSK14 [R/W] 11111111 11111111		
$00C418_H$	IF1ARB24 [R/W] 00000000 00000000		IF1ARB14 [R/W] 00000000 00000000		
$00C41C_H$	IF1MCTR4 [R/W] 00000000 00000000		res.		
$00C420_H$	IF1DTA14 [R/W] 00000000 00000000		IF1DTA24 [R/W] 00000000 00000000		
$00C424_H$	IF1DTB14 [R/W] 00000000 00000000		IF1DTB24 [R/W] 00000000 00000000		
$00C428_H$ - $00C42C_H$	reserved				
$00C430_H$	*IF1DTA24 [R/W] 00000000 00000000*		*IF1DTA14 [R/W] 00000000 00000000*		
$00C434_H$	*IF1DTB24 [R/W] 00000000 00000000*		*IF1DTB14 [R/W] 00000000 00000000*		
$00C438_H$ - $00C43C_H$	reserved				
$00C440_H$	IF2CREQ4 [R/W] 00000000 00000001		IF2CMSK4 [R/W] 00000000 00000000		CAN 4 IF 2 Register
$00C444_H$	IF2MSK24 [R/W] 11111111 11111111		IF2MSK14 [R/W] 11111111 11111111		
$00C448_H$	IF2ARB24 [R/W] 00000000 00000000		IF2ARB14 [R/W] 00000000 00000000		
$00C44C_H$	IF2MCTR4 [R/W] 00000000 00000000		res.		
$00C450_H$	IF2DTA14 [R/W] 00000000 00000000		IF2DTA24 [R/W] 00000000 00000000		
$00C454_H$	IF2DTB14 [R/W] 00000000 00000000		IF2DTB24 [R/W] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
$00C458_H$ - $00C45C_H$	reserved				
$00C460_H$	*IF2DTA24 [R/W]* *00000000 00000000*		*IF2DTA14 [R/W]* *00000000 00000000*		
$00C464_H$	*IF2DTB24 [R/W]* *00000000 00000000*		*IF2DTB14 [R/W]* *00000000 00000000*		
$00C468_H$ - $00C47C_H$	reserved				
$00C480_H$	TREQR24 [R] 00000000 00000000		TREQR14 [R] 00000000 00000000		CAN 4 Status Flags
$00C484_H$ - $00C48C_H$	reserved				
$00C490_H$	NEWDT24 [R] 00000000 00000000		NEWDT14 [R] 00000000 00000000		
$00C494_H$ - $00C49C_H$	reserved				
$00C4A0_H$	INTPND24 [R] 00000000 00000000		INTPND14 [R] 00000000 00000000		
$00C4A4_H$ - $00C4AC_H$	reserved				
$00C4B0_H$	MSGVAL24 [R] 00000000 00000000		MSGVAL14 [R] 00000000 00000000		
$00C4B4_H$ - $00EFFC_H$	reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--0000				
$00F008_H$	BIAC [R] -------- -------- -------- 00000000				
$00F00C_H$	BOAC [R] -------- -------- -------- 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- -------- 00000000				
$00F014_H$ - $00F01C_H$	reserved				
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$ - $00F07C_H$	reserved				
$00F080_H$	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
$00F084_H$	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F088_H$	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F08C_H$	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F090_H$	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F094_H$	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F098_H$	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F09C_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
$00F0A0_H$ - $027FFC_H$	reserved				
028000_H - $02FFFC_H$	MB91F464AA D-RAM size is 8kB : $02E000_H$ - $02FFFC_H$ (data access is 0 waitcycles)				D-RAM 32 kB
030000_H - $037FFC_H$	MB91F464AA I-/D-RAM size is 8kB : 030000_H - $031FFC_H$ (instruction access is 0 waitcycles, data access is 1 waitcycle)				I-/D-RAM 32 kB
038000_H - $09FFFC_H$	reserved				
$0A0000_H$ - $0BFFFC_H$	ROMS03 area (128kB)				
$0C0000_H$ - $0DFFFC_H$	ROMS04 area (128kB)				
$0E0000_H$ - $0FFFF4_H$	ROMS05 area (128kB)				
$0FFFF8_H$	FMV [R] $06\ 00\ 00\ 00_H$				Fixed Reset/Mode Vector
$0FFFFC_H$	FRV [R] $00\ 00\ BF\ F8_H$				
100000_H - $137FFC_H$	reserved				
148000_H - $14FFFC_H$	ROMS07 area (32kB)				
150000_H - $4FFFFC_H$	reserved				
Write operations to address $0FFFF8_H$ and $0FFFFC_H$ are not possible. When reading these addresses, the values shown above will be read.					