Freescale Semiconductor

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MPC5554 Microcontroller Data Sheet

32-bit Embedded Controller Division

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5554 microcontroller device. For functional characteristics, refer to the *MPC5553/MPC5554 Microcontroller Reference Manual* (MPC5553/MPC5554RM).

Table of Contents

1 Overview

The MPC5554 microcontroller (MCU) is one of the first members of the MPC5500 family of next generation powertrain microcontrollers based on the PowerPC Book E architecture. The MPC5500 family contains a PowerPC™ processor core. This family of parts contains many new features coupled with high performance CMOS technology to provide significant performance improvement over the MPC565.

The e200z6 CPU of the MPC5500 family complies with the PowerPC Book E architecture. It is 100% user mode compatible (with floating point library) with the classic PowerPC instruction set. The Book E architecture has enhancements that improve the PowerPC architecture's fit in embedded applications. This core also has

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additional instructions, including digital signal processing (DSP) instructions, beyond the classic PowerPC instruction set.

The MPC5554 of the MPC5500 family has two levels of memory hierarchy. The fastest accesses are to the 32-kilobyte unified cache. The next level in the hierarchy contains the 64-kilobyte on-chip internal SRAM and 2 Mbyte internal Flash memory. Both the internal SRAM and the Flash memory can hold instructions and data. The external bus interface has been designed to support most of the standard memories used with the MPC5xx family.

The complex I/O timer functions of the MPC5500 family are performed by two enhanced time processor unit engines (eTPU). Each eTPU engine controls 32 hardware channels. The eTPU has been enhanced over the TPU by providing 24-bit timers, double action hardware channels, variable number of parameters per channel, angle clock hardware, and additional control and arithmetic instructions. The eTPU can be programmed using a high-level programming language.

The less complex timer functions of the MPC5500 family are performed by the enhanced modular input/output system (eMIOS). The eMIOS' 24 hardware channels are capable of single action, double action, pulse width modulation (PWM) and modulus counter operation. Motor control capabilities include edge-aligned and center-aligned PWM.

Off-chip communication is performed by a suite of serial protocols including controller area networks — three FlexCANs, four enhanced deserial/serial peripheral interfaces (DSPI), and enhanced serial communications interfaces (eSCIs). The DSPIs support pin reduction through hardware serialization and deserialization of timer channels and general-purpose input/output (GPIO) signals.

The MCU of the MPC5554 has an on-chip 40-channel enhanced queued dual analog-to-digital converter (eQADC).

The system integration unit (SIU) performs several chip-wide configuration functions. Pad configuration and general-purpose input and output (GPIO) are controlled from the SIU. External interrupts and reset control are also found in the SIU. The internal multiplexer submodule (SIU_DISR) provides multiplexing of eQADC trigger sources, daisy chaining the DSPIs and external interrupt signal multiplexing.

2 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5554 MCU.

2.1 Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Num	Characteristic	Symbol	Min	Max[2]	Unit
1	1.5V Core Supply Voltage [3]	V_{DD}	- 0.3	1.7	V
2	Flash Program/Erase Voltage	V_{PP}	- 0.3	6.5	V
3	Flash Core Voltage [4]	V_{DDF}	- 0.3	1.7	V
4	Flash Read Voltage	V_{FLASH}	- 0.3	4.6	V
5	SRAM Standby Voltage	V_{STBY}	- 0.3	1.7	V
6	Clock Synthesizer Voltage	V_{DDSYN}	- 0.3	4.6	V
7	3.3V I/O Buffer Voltage	V_{DD33}	-0.3	4.6	V
8	Voltage Regulator Control Input Voltage	V_{RC33}	-0.3	4.6	V
9	Analog Supply Voltage (reference to V_{SSA})	V_{DDA}	- 0.3	5.5	V
10	I/O Supply Voltage (Fast I/O Pads) [5]	V_{DDE}	- 0.3	4.6	V
11	I/O Supply Voltage (Slow/Medium I/O Pads)	V_{DDEH}	- 0.3	6.5	V
12	DC Input Voltage (VDDEH powered I/O Pads)[6] (VDDE powered I/O Pads)[7]	V_{IN}	 -0.3 -0.3	 6.5 4.6	V
13	Analog Reference High Voltage (reference to VRL)	V_{RH}	- 0.3	5.5	V
14	VSS Differential Voltage	V_{SS} - V_{SSA}	- 0.1	0.1	V
15	VDD Differential Voltage	V_{DD} - V_{DDA}	- V_{DDA}	V_{DD}	V
16	V_{REF} Differential Voltage	V_{RH} - V_{RL}	- 0.3	5.5	V
17	V_{RH} to VDDA Differential Voltage	V_{RH} - V_{DDA}	- 5.5	5.5	V
18	V_{RL} to VSSA Differential Voltage	V_{RL} - V_{SSA}	- 0.3	0.3	V
19	V_{DDEH} to V_{DDA} Differential Voltage	V_{DDEH} - V_{DDA}	-V_{DDA}	V_{DDEH}	V
20	V_{DDF} to V_{DD} Differential Voltage	V_{DDF} - V_{DD}	-0.3	0.3	V
21	VRC33 to VDDSYN Differential Voltage	V_{RC33} - V_{DDSYN}	-0.1	0.1[8]	V
22	VSSSYN to VSS Differential Voltage	V_{SSSYN} - V_{SS}	-0.1	0.1	V
23	V_{RCVSS} to V_{SS} Differential Voltage	V_{RCVSS} - V_{SS}	-0.1	0.1	V

Table 1. Absolute Maximum Ratings[1] (continued)

Num	Characteristic	Symbol	Min	Max[2]	Unit
24	Maximum Instantaneous Digital Input Current [9] (per pin, applies to all digital pins)	I_{MAXD}	-1	1	mA
25	Maximum Instantaneous Analog Input Current [10] (per pin, applies to all analog pins)	I_{MAXA}	-3	3	mA
26	Maximum Operating Temperature Range [11] - Die Junction Temperature	T_J	-40.0	150.0	°C
27	Storage Temperature Range	T_{STG}	- 55.0	150.0	°C
28	Maximum Solder Temperature [12]	T_{SDR}	-	260.0	°C
29	Moisture Sensitivity Level [13]	MSL	-	3	

NOTES:

[1]Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

[2]Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.

[3]1.5V +/- 10% for proper operation. This parameter is specified at a maximum junction temperature of 140C.

[4]The VDDF supply is connected to VDD in the package substrate. This specification applies to non-packaged devices only.

[5]All functional non-supply I/O pins are clamped to VSS and VDDE or VDDEH.

[6]Internal structures hold the input voltage below this maximum voltage on all of these pins powered by VDDEHx supplies, if the maximum injection current specification is met (1 mA for all pins) and VDDEH is within Operating Voltage specifications.

[7]Internal structures limit the input voltage below 1.1 volts above the VDDEx power supply on all pins powered by VDDEHx supplies, if the maximum injection current specification is met (1 mA for all pins) and if VDDEx is less than 3.5 volts. External structures may be required if the VDDEx supply can go up to 3.6 volts.

[8]Up to 0.6 volts during power up and power down.

[9]Total injection current for all pins (including both digital and analog) must not exceed 25mA.

[10]Total injection current for all analog input pins must not exceed 15mA.

[11]Lifetime operation at these specification limits is not guaranteed.

[12]Solder profile per CDF-AEC-Q100.

[13]Moisture sensitivity per JEDEC test method A112.

2.2 Thermal Characteristics

Table 2. Thermal Characteristics

Num	Characteristic	Symbol	Value	Unit
1	Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\theta JA}$	24	°C/W
2	Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\theta JMA}$	18	°C/W
3	Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JA}$	19	°C/W
4	Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	15	°C/W
5	Junction to Board [4] (Four layer board 2s2p)	$R_{\theta JB}$	9	°C/W
6	Junction to Case [5]	$R_{\theta JC}$	5	°C/W
7	Junction to Package Top [6] Natural Convection	Ψ_{JT}	2	°C/W

NOTES:
[1]Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[2]Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

[3]Per JEDEC JESD51-6 with the board horizontal.

[4]Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[5]Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

[6]Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

2.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D)$$

where:

T_A= ambient temperature for the package (^oC)

$R_{\theta JA}$= junction to ambient thermal resistance ($^oC/W$)

P_D= power dissipation in the package (W)

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single layer (1s) board and on the four layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of the component is not a constant. It will depend on the construction of the application board (number of planes), the effective size of the board which cools the component, and how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

The recommendation is to connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes will reduce the thermal performance. Thinner planes will also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm^2.

The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package will be approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D)$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction to board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$= junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$= case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around

the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate "two resistor" thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} * P_D)$$

where:

T_T= thermocouple temperature on top of the package (^oC)

Ψ_{JT}= thermal characterization parameter ($^oC/W$)

P_D= power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

- 1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- 2. G. Kromann, S. Shidore, and S. Addison, "Thermal Modeling of a PBGA for Air-Cooled Applications," Electronic Packaging and Production, pp. 53-58, March 1998.
- 3. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

2.3 MPC5554 Package

The MPC5554 is available in packaged form. The package is a 416-ball PBGA with a 1.0 mm ball pitch and Freescale case outline 1494-01. Refer to Section 3, "Mechanicals" for more information.

2.4 EMI (Electromagnetic Interference) Characteristics

Table 3. EMI Testing Specifications[1]

Num	Characteristic	Min. Value	Typ. Value	Max. Value	Unit
1	Scan Range	0.15		1000	MHz
2	Operating Frequency	-		132	MHz
3	V_{DD} Operating Voltages	-	1.5	-	V
4	V_{DDSYN}, V_{RC33}, V_{DD33}, V_{FLASH}, V_{DDE} Operating Voltages	-	3.3	-	V
5	VPP, VDDEH, VDDA Operating Voltages	-	5.0	-	V
6	Maximum Amplitude	-		14[2] 32[3]	dBuV
7	Operating Temperature	-		25	°C

NOTES:
[1]EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03.
[2]As measured with "single-chip" EMI program.
[3]As measured with "expanded" EMI program.

2.5 ESD Characteristics

Table 4. ESD Ratings[1, 2]

Characteristic	Symbol	Value	Unit
ESD for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ohm
	C	100	pF
ESD for Field Induced Charge Model (FDCM)		500 (all pins)	V
		750 (corner pins)	
Number of Pulses per pin: Positive Pulses (HBM) Negative Pulses (HBM)	 - -	 1 1	 - -
Interval of Pulses	-	1	second

NOTES:
[1]All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

[2]A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

2.6 VRC/POR Electrical Specifications

Table 5. VRC/POR Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Units
1	1.5V (VDD) POR Negated (Ramp Up) 1.5V (VDD) POR Asserted (Ramp Down)	V_POR15	1.1 1.1	1.35 1.35	V
2	3.3V (VDDSYN) POR Negated (Ramp Up) 3.3V (VDDSYN) POR Asserted (Ramp Down)	V_POR33	2.0 2.0	2.85 2.85	V
3	RESET Pin Supply (VDDEH6) POR Negated (Ramp Up) RESET Pin Supply (VDDEH6) POR Asserted (Ramp Down)	V_POR5	2.0 2.0	2.85 2.85	V
4	VRC33 voltage before regulator controller allows the pass transistor to start turning on	V_TRANS_START	1.0	2.0	V
5	VRC33 voltage when regulator controller allows the pass transistor to completely turn on[1, 2]	V_TRANS_ON	2.0	2.85	V
6	VRC33 voltage above which the regulator controller will keep the 1.5V supply in regulation[3, 6]	V_VRC33REG	3.0	—	V
7	Current which can be sourced by VRCCTL	I_VRCCTL[4]	6.8	—	mA
8	Voltage differential during power up that VDD33 can lag VDDSYN or $\overline{\text{VDDEH6}}$ before VDDSYN and $\overline{\text{VDDEH6}}$ reach V_POR33 and V_POR5 minimums respectively	VDD33_LAG	—	1.0	V
9	|Slew rate| on power supply pins		—	50	V/ms
10	Requested Gain: Idd / I_VRCCTL (@vdd = 1.35v, f_{sys} = 133MHz)[5, 6] -40C 25C 150C (Tj)	BETA		 50 60 70	

NOTES:
[1]User must be able to supply full operating current for the 1.5V supply when the 3.3V supply reaches this range.
[2]Current limit may be reached during ramp up and should not be treated as short circuit current.
[3]At peak current for device.
[4]I_VRCCTL measured at the following conditions: VDD=1.35V, VRC33=3.0V, V_VRCCTL=2.2V.
[5]Values are based on IDD from typical applications as explained in the IDD Electrical Specification. Beta value for high use IDD numbers would be 75 (-40C), 90 (+25C), 105 (+150C)@ 133MHz.
[6]Assumes transistor and board design conform to Freescale recommendations as described in Application note **TBA**.

2.7 Power Up/Down Sequencing

Power sequencing between the 1.5V power supply and VDDSYN or the RESET power supplies is required if the user provides an external 1.5V power supply and ties VRC33 to ground. To avoid this power sequencing requirement, the user should power up VRC33 within the specified operating range, even if not using the on chip Voltage Regulator Controller. Refer to Section 2.7.1, "Power Up Sequence (If VRC33 Grounded)" and Section 2.7.2, "Power Down Sequence (If VRC33 Grounded)."

Another power sequencing requirement is that VDD33 must be of sufficient voltage before POR negates so that the values on certain pins are treated as 1s when POR does negate. Refer to Section 2.7.3, "Input Value of Pins During POR Dependent on VDD33."

Although there is no power sequencing required between VRC33 and VDDSYN during power up, in order for the VRC stage turn-on to operate within specification, VRC33 must not lead VDDSYN by more than 600mV or lag by more than 100mV. Higher spikes in the emitter current of the pass transistor will occur if VRC33 leads or lags VDDSYN by more than these amounts. The value of that higher spike in current depends on the board power supply circuitry and the amount of board level capacitance.

Furthermore, when all of the PORs negate, the system clock will start to toggle, adding another large increase of the current consumption from VRC33. If VRC33 lags VDDSYN by more than 100 mV, this increased current consumption can drop VDD low enough to assert the 1.5V POR again. Oscillations are even possible because when the 1.5V POR asserts, the system clock will stop, causing the voltage on VDD to rise until the 1.5V POR negates again. Any oscillations will stop when VRC33 is powered sufficiently.

When powering down, VRC33 and VDDSYN do not have a delta requirement to each other because the bypass capacitors internal and external to the SoC already are charged.

When not powering up or down, VRC33 and VDDSYN do not have a delta requirement to each other for the VRC to operate within specification.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies depending on power. Table 6 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type), and Table 7 for all pins with pad type pad_mh (medium type) and pad_sh (slow type) .

Table 6. Power Sequence Pin States (fast pads)

V_{DDE}	V_{DD33}	V_{DD}	pad_fc (fast) Output Driver state	Comment
LOW	X	X	LOW	Functional I/O pins are clamped to VSS and VDDE
VDDE	LOW	X	HIGH	
VDDE	VDD33	LOW	HIGH IMPEDANCE	POR asserted.
VDDE	VDD33	VDD	FUNCTIONAL	No POR asserted

Table 7. Power Sequence Pin States (medium and slow pads)

V_{DDEH}	V_{DD}	pad_mh/pad_sh (medium and slow) Output Driver	Comment
LOW	X	LOW	Functional I/O pins are clamped to VSS and VDDEH
VDDEH	LOW	HIGH IMPEDANCE	POR asserted
VDDEH	VDD	FUNCTIONAL	No POR asserted

2.7.1 Power Up Sequence (If VRC33 Grounded)

In this case, the 1.5V VDD supply must rise to 1.35V before the 3.3V VDDSYN and the RESET power supplies rises above 2.0V. This is to insure that digital logic in the PLL on the 1.5V supply will not begin to operate below the specified operation range lower limit of 1.35V. Since the internal 1.5V POR is disabled, the internal 3.3V POR or the RESET power POR must be depended on to hold the device in reset. Since they may negate as low as 2.0V, it is necessary for VDD to be within spec before the 3.3V POR and the RESET POR negate.

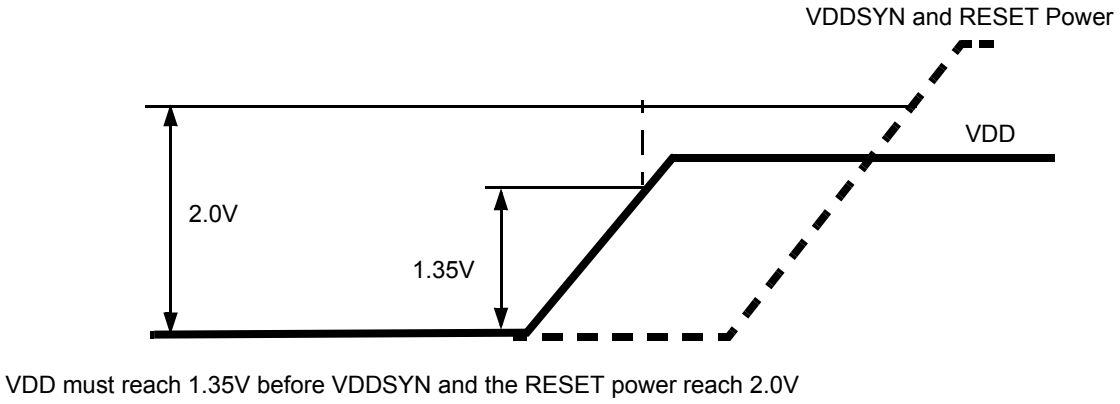

Figure 1. Power Up Sequence if VRC33 Grounded

2.7.2 Power Down Sequence (If VRC33 Grounded)

In this case, the only requirement is that if VDD falls below its operating range, VDDSYN or the RESET power must fall below 2.0V before VDD is allowed to rise back into its operating range. This is to insure that digital 1.5V logic that is only reset by ORed_POR, which may have been affected by the 1.5V supply falling below spec, will be reset properly.

2.7.3 Input Value of Pins During POR Dependent on VDD33

In order to avoid accidentally selecting the bypass clock because PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ were not treated as 1s when POR negates, VDD33 must not lag VDDSYN and the RESET pin power (VDDEH6)

when powering the device by more than the VDD33 lag specification in Table 5. VDD33 individually can lag either VDDSYN or the RESET pin power (VDDEH6) by more than the VDD33 lag specification. VDD33 can lag one of the VDDSYN or VDDEH6 supplies, but cannot lag both by more than the VDD33 lag specification. This VDD33 lag specification only applies during power up. VDD33 has no lead or lag requirements when powering down.

2.8 DC Electrical Specifications

Table 8. DC Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit
1	Core Supply Voltage	V_{DD}	1.35	1.65	V
2	I/O Supply Voltage (Fast I/O)	V_{DDE}	1.62	3.6	V
3	I/O Supply Voltage (Slow/Medium I/O)	V_{DDEH}	3.0	5.25	V
4	3.3V I/O Buffer Voltage	V_{DD33}	3.0	3.6	V
5	Voltage Regulator Control Input Voltage	V_{RC33}	3.0	3.6	V
6	Analog Supply Voltage[1]	V_{DDA}	4.5	5.25	V
7	Flash Operating Voltage [2]	VDDF	1.35	1.65	V
8	Flash Programming Voltage[3]	VPP	4.5	5.25	V
9	Flash Read Voltage	VFLASH	3.0	3.6	V
10	SRAM Standby Voltage[4]	VSTBY	0.8	1.2	V
11	Clock Synthesizer Operating Voltage	VDDSYN	3.0	3.6	V
12	Fast I/O Input High Voltage	V_{IH_F}	0.65 * V_{DDE}	V_{DDE} + 0.3	V
13	Fast I/O Input Low Voltage	V_{IL_F}	V_{SS} - 0.3	0.35 * V_{DDE}	V
14	Slow I/O Input High Voltage	V_{IH_S}	0.65 * V_{DDEH}	V_{DDE_H} + 0.3	V
15	Slow I/O Input Low Voltage	V_{IL_S}	V_{SS} - 0.3	0.35 * V_{DDEH}	V
16	Fast I/O Input Hysteresis	V_{HYS_F}	0.1 * V_{DDE}		V
17	Slow I/O Input Hysteresis	V_{HYS_S}	0.1 * V_{DDEH}		V
18	Analog Input Voltage	V_{INDC}	VSSA - 0.3	VDDA + 0.3	V
19	Fast I/O Output High Voltage (I_{OH_F} = -2.0mA)	V_{OH_F}	0.8 * VDDE	-	V
20	Slow/Medium I/O Output High Voltage (I_{OH_S} = -2.0mA)	V_{OH_S}	0.8 * VDDEH	-	V
21	Fast I/O Output Low Voltage (I_{OL_F} = 2.0mA)	V_{OL_F}	-	0.2 * VDDE	V
22	Slow/Medium I/O Output Low Voltage (I_{OL_S} = 2.0mA)	V_{OL_S}	-	0.2 * VDDEH	V
23	Load Capacitance (Fast I/O)[5] DSC(PCR[8:9]) = 0b00 DSC(PCR[8:9]) = 0b01 DSC(PCR[8:9]) = 0b10 DSC(PCR[8:9]) = 0b11	C_L	 - - -	 10 20 30 50	 pF pF pF pF

Table 8. DC Electrical Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
24	Input Capacitance (Digital Pins)	C_{IN}	-	7	pF
25	Input Capacitance (Analog Pins)	C_{IN_A}	-	10	pF
26	Input Capacitance (Digital and Analog Pins[6])	C_{IN_M}	-	12	pF
27	Operating Current 1.5V Supplies @ 132MHz: VDD (including VDDF max current)[7, 8] @1.65V Typical Use VDD (including VDDF max current)[7, 8] @1.35V Typical Use VDD (including VDDF max current)[8, 9] @1.65V High Use VDD (including VDDF max current)[8, 9] @1.35V High Use Operating Current 1.5V Supplies @ 114MHz: VDD (including VDDF max current)[7, 8] @1.65V Typical Use VDD (including VDDF max current)[7, 8] @1.35V Typical Use VDD (including VDDF max current)[8, 9] @1.65V High Use VDD (including VDDF max current)[8, 9] @1.35V High Use Operating Current 1.5V Supplies @ 82MHz: VDD (including VDDF max current)[7, 8] @1.65V Typical Use VDD (including VDDF max current)[7, 8] @1.35V Typical Use VDD (including VDDF max current)[8, 9] @1.65V High Use VDD (including VDDF max current)[8, 9] @1.35V High Use VSTBY[10]	IDD IDD IDD IDD IDD IDD IDD IDD IDD IDD IDD IDD IDD_{STBY}	- - - - - - - - - - - - -	600 480 **TBD** **TBD** 522 418 **TBD** **TBD** 390 312 **TBD** **TBD** 100	mA mA mA mA mA mA mA mA mA mA mA mA µA
28	Operating Current 3.3V Supplies @ 133MHz: VDD33[11] VFLASH VDDSYN	IDD_{33} I_{VFLASH} I_{DDSYN}	- - -	2 + values derived from procedure of Footnote [11] 10 15	mA mA mA
29	Operating Current 5.0V Supplies @ 133MHz: VDDA Analog Reference Supply Current (VRH, VRL) VPP	IDD_A I_{REF} I_{PP}	- - -	20.0 1.0 25	mA mA mA

Table 8. DC Electrical Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
30	Operating Current VDDE[12] Supplies @ 133MHz: VDDEH1 VDDE2 VDDE3 VDDEH4 VDDE5 VDDEH6 VDDE7 VDDEH8 VDDEH9	 IDD1 IDD2 IDD3 IDD4 IDD5 IDD6 IDD7 IDD8 IDD9	 - - - - - - - - -	See Footnote 12	 mA mA mA mA mA mA mA mA mA
31	Fast I/O Weak Pull Up/Down Current[13] 1.62V - 1.98V 2.25V - 2.75V 3.0V - 3.6V	I_{ACT_F}	 10 20 20	 100 130 150	 µA µA µA
32	Slow/Medium I/O Weak Pull Up/Down Current[14] 3.0V - 3.6V 4.5V - 5.5V	I_{ACT_S}	 10 20	 150 170	 µA µA
33	I/O Input Leakage Current[15]	I_{INACT_D}	- 2.5	2.5	µA
34	DC Injection Current (per pin)	I_{IC}	- 1.0	1.0	mA
35	Analog Input Current, Channel Off[16]	I_{INACT_A}	-150	150	nA
36	VSS Differential Voltage[17]	VSS - VSSA	- 100	100	mV
37	Analog Reference Low Voltage	VRL	VSSA - 0.1	VSSA + 0.1	V
38	VRL Differential Voltage	VRL - VSSA	-100	100	mV
39	Analog Reference High Voltage	VRH	VDDA - 0.1	VDDA + 0.1	V
40	V_{REF} Differential Voltage	VRH - VRL	4.5	5.25	V
41	VSSSYN to VSS Differential Voltage	VSSSYN - VSS	-50	50	mV
42	VRCVSS to VSS Differential Voltage	VRCVSS - VSS	-50	50	mV
43	VDDF to VDD Differential Voltage[2]	VDDF - VDD	-100	100	mV
44	Analog Input Differential Signal Range (with common mode 2.5V)	V_{IDIFF}	- 2.5	2.5	V
45	Operating Temperature Range - Ambient (Packaged)	T_A (T_L to T_H)	- 40.0	125.0	°C
46	Slew rate on power supply pins	-	-	50	V/ms

NOTES:
[1] | VDDA0 -VDDA1 | must be < 0.1V
[2] The VDDF supply is connected to VDD in the package substrate. This specification applies to non-packaged devices only.
[3] VPP is only required for program and erase operations. During normal operation this pin may not be powered.
[4] During standby operation. If standby operation is not required, VSTBY can be connected to ground.
[5] Applies to CLKOUT, external bus pins, and Nexus pins.
[6] Applies to the FCK, SDI, SDO, and SDS_B pins.

[7]Average current measured on Automotive benchmark.

[8]Peak currents may be higher on specialized code.

[9]High use current measured on **TBD** Automotive benchmark.

[10]VSTBY current specified at 1.0V at a junction temperature of 85 °C. VSTBY current is 300uA maximum at a junction temperature of 150 °C.

[11]Power requirements for the VDD33 supply are dependent on the frequency of operation and load of all I/O pins, and the voltages on the I/O segments. See Table 10 for values to calculate power dissipation for specific operation.

[12]Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Table 9 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[13]Absolute value of current, measured at V_{IL} and V_{IH}.

[14]Absolute value of current, measured at V_{IL} and V_{IH}.

[15]Weak pull up/down inactive. Measured at VDDE = 3.6 V and VDDEH = 5.25 V. Applies to pad types: pad_fc, pad_sh, and pad_mh.

[16]Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to pad types: pad_a and pad_ae.

[17]VSSA refers to both VSSA0 and VSSA1. | VSSA0 -VSSA1 | must be < 0.1V

2.8.1 I/O Pad Current Specifications

The power consumption of an I/O segment is dependent on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 9 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 9.

Table 9. I/O Pad Average DC Current[1]

Num	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive Select	Current (mA)
1	Slow	I_{DRV_SH}	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium	I_{DRV_MH}	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9

Table 9. I/O Pad Average DC Current[1] (continued)

Num	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive Select	Current (mA)
9	Fast	I_{DRV_FC}	66	10	3.6	00	2.8
10			66	20	3.6	01	5.2
11			66	30	3.6	10	8.5
12			66	50	3.6	11	11.0
13			66	10	1.98	00	1.6
14			66	20	1.98	01	2.9
15			66	30	1.98	10	4.2
16			66	50	1.98	11	6.7
17			56	10	3.6	00	2.4
18			56	20	3.6	01	4.4
19			56	30	3.6	10	7.2
20			56	50	3.6	11	9.3
21			56	10	1.98	00	1.3
22			56	20	1.98	01	2.5
23			56	30	1.98	10	3.5
24			56	50	1.98	11	5.7
25			40	10	3.6	00	1.7
26			40	20	3.6	01	3.1
27			40	30	3.6	10	5.1
28			40	50	3.6	11	6.6
29			40	10	1.98	00	1.0
30			40	20	1.98	01	1.8
31			40	30	1.98	10	2.5
32			40	50	1.98	11	4.0

NOTES:
[1]These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.
[2]All loads are lumped.

2.8.2 I/O Pad VDD33 Current Specifications

The power consumption of the VDD33 supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin VDD33 currents for all I/O segments. The output pin VDD33 current can be calculated from Table 10 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin VDD33 current can be calculated from Table 10 based on the voltage, frequency, and load on all pad_sh and pad_sh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

Table 10. VDD33 Pad Average DC Current[1]

Num	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	Current (mA)
Inputs								
1	Slow	I_{33_SH}	66	0.5	3.6	5.5	NA	0.003
2	Medium	I_{33_MH}	66	0.5	3.6	5.5	NA	0.003
Outputs								
3	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.7
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

NOTES:
[1]These are typical values that are estimated from simulation and not tested. Currents apply to output pins only for the fast pads and to input pins only for the slow and medium pads.

[2]All loads are lumped.

2.9 Oscillator and FMPLL Electrical Characteristics

Table 11. HiP7 FMPLL Electrical Specifications

(V_{DDSYN} = 3.0V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H) (f_{sys} = 80 MHz, 112 MHz, 132 MHz)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range: Crystal reference External reference Dual Controller (1:1 mode)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 20 20 $f_{sys}/2$	MHz
2	System Frequency [1]	f_{sys}	$f_{ico(min)} \div 2^{RFD}$	f_{sys}	MHz
2A	PLL ICO Frequency [2]	f_{ICO}	—	f_{sys}	MHz
3	System Clock Period	t_{CYC}	-	$1 / f_{sys}$	ns
4	Loss of Reference Frequency [3]	f_{LOR}	100	1000	kHz
5	Self Clocked Mode (SCM) Frequency [4]	f_{SCM}	7.4	16.5	MHz
6	EXTAL Input High Voltage Crystal Mode [5] All other modes (Dual Controller (1:1), Bypass, External Reference)	 V_{IHEXT} V_{IHEXT}	 Vxtal + 0.4v ((VDDE5/2) + 0.4v)	 — —	 V V
7	EXTAL Input Low Voltage Crystal Mode [6] All other modes (Dual Controller (1:1), Bypass, External Reference)	 V_{ILEXT} V_{ILEXT}	 — —	 Vxtal - 0.4v ((VDDE5/2) - 0.4v)	 V V
8	XTAL Current [7]	I_{XTAL}	1	3	mA
9	Total On-chip stray capacitance on XTAL	C_{S_XTAL}		1.5	pF
10	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}		1.5	pF
11	Crystal manufacturer's recommended capacitive load	C_L	See crystal spec	See crystal spec	pF
12	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}		$2*C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [8]	pF
13	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}		$2*C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$ [8]	pF

Table 11. HiP7 FMPLL Electrical Specifications (continued)

(V_{DDSYN} = 3.0V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H) (f_{sys} = 80 MHz, 112 MHz, 132 MHz)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
14	PLL Lock Time[9]	t_{lpll}	—	750	µs
15	Dual Controller (1:1) Clock Skew (between CLKOUT and EXTAL) [10]	t_{skew}	-1	1	ns
16	Duty Cycle of reference	t_{dc}	40	60	%
17	Frequency un-LOCK Range	f_{UL}	- 4.0	4.0	% f_{sys}
18	Frequency LOCK Range	f_{LCK}	- 2.0	2.0	% f_{sys}
19	CLKOUT Period Jitter,[11, 12] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter (Averaged over 2 ms interval)	C_{jitter}	— —	5.0 .01	% f_{clkout}
20	Frequency Modulation Range Limit [13] (f_{sys}Max must not be exceeded)	C_{mod}	0.8	2.4	%f_{sys}
21	ICO Frequency. f_{ico}=[f_{ref}*(MFD+4)]/(PREDIV+1)[14]	f_{ico}	48	f_{sys}	MHz

NOTES:
[1] All internal registers retain data at 0 Hz.
[2] Maximum frequency input to the RFD
[3] "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.
[4] Self clocked mode (SCM) frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR}. This frequency is measured on the CLKOUT pin with the divider set to divide-by-2 of the system clock. NOTE: In SCM, the MFD has no effect and the RFD is bypassed.
[5] This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, V_{extal} - V_{xtal} >= 400mV criteria has to be met for oscillator's comparator to produce output clock.
[6] This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, V_{xtal} - V_{extal} >= 400mV criteria has to be met for oscillator's comparator to produce output clock.
[7] I_{xtal} is the oscillator bias current out of the xtal pin with both Extal and Xtal pins grounded.
[8] C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively
[9] This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.
[10] PLL is operating in 1:1 PLL mode.
[11] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval. CLKOUT divider set to divide-by-2.
[12] Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter + Cmod.
[13] Modulation depth selected must not result in f_{sys} value greater than the f_{sys} maximum specified value.
[14] $f_{sys} = f_{ico} / (2^{RFD})$

2.10 eQADC Electrical Characteristics

Table 12. eQADC Conversion Specifications (Operating)

Num	Characteristic	Symbol	Min	Max	Unit
1	ADC Clock (ADCLK) Frequency[1]	F_{ADCLK}	1	12	MHz
2	Conversion Cycles	CC	15	128+16	ADCLK cycles
3	Stop Mode Recovery Time[2]	T_{SR}	10	—	µs
4	Resolution[3]	—	1.25	—	mV
5	INL: 6 MHz ADC Clock	INL6	-4	4	Counts[3]
6	INL: 12 MHz ADC Clock	INL12	-8	8	Counts
7	DNL: 6 MHz ADC Clock	DNL6	-3[4]	3[4]	Counts
8	DNL: 12 MHz ADC Clock	DNL12	-6[4]	6[4]	Counts
9	Offset Error with Calibration	OFFWC	-8[5]	8[5]	Counts
10	Full Scale Gain Error with Calibration	GAINWC	-8[6]	8[6]	Counts
11	Disruptive Input Injection Current[7, 8, 9, 10]	I_{INJ}	-1	1	mA
12	Incremental Error due to injection current. All channels have same 10kΩ < Rs <100kΩ Channel under test has Rs=10kΩ, I_{INJ}=I_{INJMAX},I_{INJMIN}	E_{INJ}	-4	4	Counts
13	Total Unadjusted Error for single ended conversions with calibration[11, 12, 13]	TUE	-4	4	Counts

NOTES:

[1]Conversion characteristics vary with F_{ADCLK} rate. Reduced conversion accuracy occurs at maximum F_{ADCLK} rate. The maximum value is based on 800KS/s and the minimum value is based on 20MHz oscillator clock frequency divided by a max imum 16 factor.

[2]Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.

[3]At VRH – VRL = 5.12 V, one lsb = 1.25 mV = one count

[4]Guaranteed 10-bit monotonicity

[5]The absolute value of the offset error without calibration ≤ 100 counts.

[6]The absolute value of the full scale gain error without calibration ≤ 120 counts.

[7]Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

[8]Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

[9]Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5V$ and $V_{NEGCLAMP} = -0.3$ V, then use the larger of the calculated values.

[10]Condition applies to two adjacent pins.

[11]The TUE specification will always be better than the sum of the INL, DNL, offset, and gain errors due to canceling errors.

[12]TUE does not apply to differential conversions.

[13]Measured at 6 MHz ADC clock. TUE with a 12 MHz ADC clock is: -16 counts < TUE < 16 counts.

2.11 H7Fa Flash Memory Electrical Characteristics

Table 13. Flash Program and Erase Specifications[1], [2]

Num	Characteristic	Symbol	Min	Typ	Initial Max[3]	Max[4]	Unit
1	16KB Block Erase Time[5]	$T_{16kerase}$	-	250	-	-	ms
2	128KB Block Erase Time[5]	$T_{128kerase}$	-	630	-	-	ms
3	Double Word (64 bits) Program Time	$T_{dwprogram}$	-	10	-	TBD	µs
4	Page Program Time	$T_{pprogram}$	-	22	44[6]	TBD	µs
5	16KB Block Program Time	$T_{16kprogram}$	-	15	-	-	ms
6	128KB Block Program Time	$T_{128kprogram}$	-	120	-	-	ms
7	16KB Block Pre-program and Erase Time	$T_{16kpperase}$	-	265	-	TBD	ms
8	128KB Block Pre-program and Erase Time	$T_{128kpperase}$	-	750	1250	TBD	ms

NOTES:

[1]Typical program and erase times assume nominal supply values and operation at 25 ^{o}C.

[2]The Flash Program and Erase Specifications table is valid up to 1K program/erase cycles.

[3]Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, typical supply voltage, 80MHz minimum system frequency.

[4]Worst case maximum conditions: supply voltage and temperature.

[5] Assumes all cells are pre-programmed. Time will increase with number of unprogrammed bits in block.

[6]Page size is 256 bits (8 words).

Table 14. Flash EEPROM Module Life (Full Temperature Range)

Num	Characteristic	Symbol	Min	Max	Unit
1	Number of Program/Erase cycles per block before failure	P/E	100,000	-	cycles
2	Data retention Blocks with 0 - 1,000 P/E cycles Blocks with 1,001 - 100,000 P/E cycles	Retention	 20 5	-	years

2.12 AC Specifications

2.12.1 Pad AC Specifications

Table 15. Pad AC Specifications (VDDEH = 5.0V, VDDE = 1.8V)[1]

Num	Pad	SRC/DSC	Out Delay[2, 3, 4] (ns)	Rise/Fall[4, 5] (ns)	Load Drive (pF)
1	Slow	11	26	15	50
			82	60	200
		01	75	40	50
			137	80	200
		00	377	200	50
			476	260	200
2	Medium	11	16	8	50
			43	30	200
		01	34	15	50
			61	35	200
		00	192	100	50
			239	125	200
3	Fast	00	3.1	2.7	10
		01		2.5	20
		10		2.4	30
		11		2.3	50
4	Pull Up/Down (3.6V max)	-	-	7500	50
5	Pull Up/Down (5.5V max)	-	-	9000	50

NOTES:
[1]These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDE = 1.62V to 1.98V, VDDEH = 4.5V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH.

[2]This parameter is supplied for reference and is not guaranteed by design and not tested.

[3]Out delay is shown in Figure 2. Add a maximum of one system clock to the output delay for delay with respect to system clock.

[4]Delay and rise/fall are measured to 20% or 80% of the respective signal.

[5]This parameter is guaranteed by characterization before qualification rather than 100% tested.

Table 16. De-rated Pad AC Specifications (VDDEH = 3.3V, VDDE = 3.3V)[1]

Num	Pad	SRC/DSC	Out Delay[2, 3, 4] (ns)	Rise/Fall[3, 5] (ns)	Load Drive (pF)
1	Slow	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200
3	Fast	00	3.2	2.4	10
		01		2.2	20
		10		2.1	30
		11		2.1	50
4	Pull Up/Down (3.6V max)	-	-	7500	50
5	Pull Up/Down (5.5V max)	-	-	9500	50

NOTES:
[1]These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDE = 3.0V to 3.6V, VDDEH = 3.0V to 3.6V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH.

[2]This parameter is supplied for reference and is not guaranteed by design and not tested.

[3]Delay and rise/fall are measured to 20% or 80% of the respective signal.

[4]Out delay is shown in Figure 2. Add a maximum of one system clock to the output delay for delay with respect to system clock.

[5]This parameter is guaranteed by characterization before qualification rather than 100% tested.

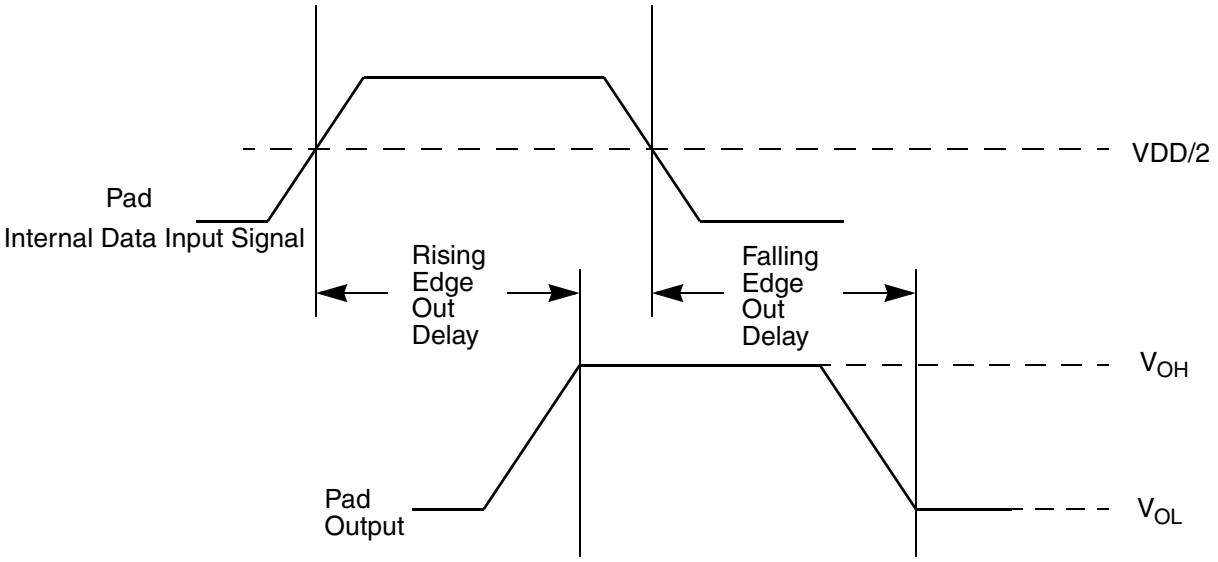

Figure 2. Pad Output Delay

2.13 AC Timing

2.13.1 Reset and Configuration Pin Timing

Table 17. Reset and Configuration Pin Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	-	t_{CYC}
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	-	t_{CYC}
3	PLLCFG, BOOTCFG, WKPCFG, $\overline{\text{RSTCFG}}$ Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	-	t_{CYC}
4	PLLCFG, BOOTCFG, WKPCFG, $\overline{\text{RSTCFG}}$ Hold Time from $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	-	t_{CYC}

NOTES:
[1]Reset timing specified at F_{SYS} = 132MHz, VDDEH = 3.0V to 5.25V, VDD = 1.35V to 1.65V, T_A = TL to TH.

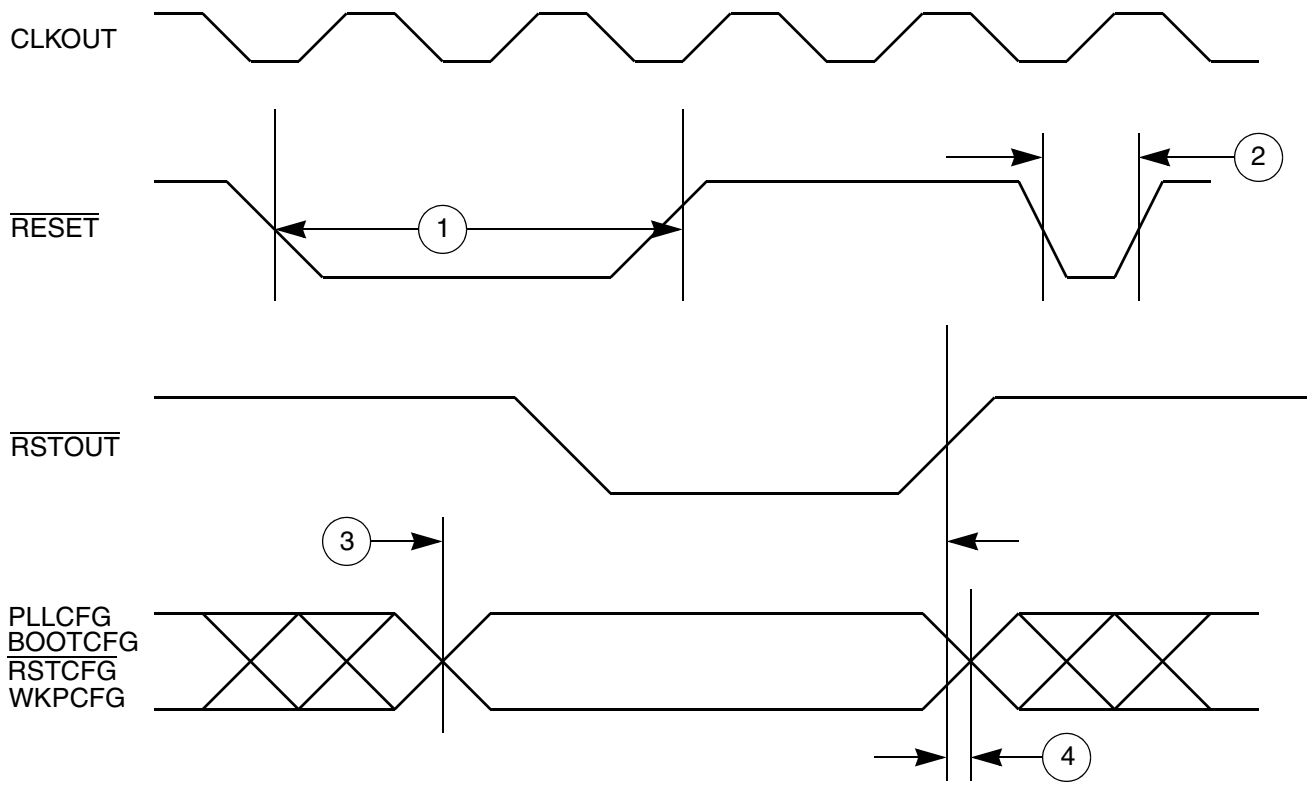

Figure 3. Reset and Configuration Pin Timing

2.13.2 IEEE 1149.1 Interface Timing

Table 18. JTAG Pin AC Electrical Characteristics[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	-	ns
2	TCK Clock Pulse Width (Measured at VDDE/2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40% - 70%)	$t_{TCKRISE}$	-	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	-	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	-	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	-	20	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	-	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	-	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	-	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	-	ns

Table 18. JTAG Pin AC Electrical Characteristics[1] (continued)

Num	Characteristic	Symbol	Min	Max	Unit
11	TCK Falling Edge to Output Valid	t_{BSDV}	-	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	-	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	-	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	-	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	-	

NOTES:
[1]JTAG timing specified at VDD = 1.35V to 1.65V, VDDE = 3.0V to 3.6V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 30pF with DSC = 0b10, SRC = 0b11. These specifications apply to JTAG boundary scan only. See Table 19 for functional specifications.

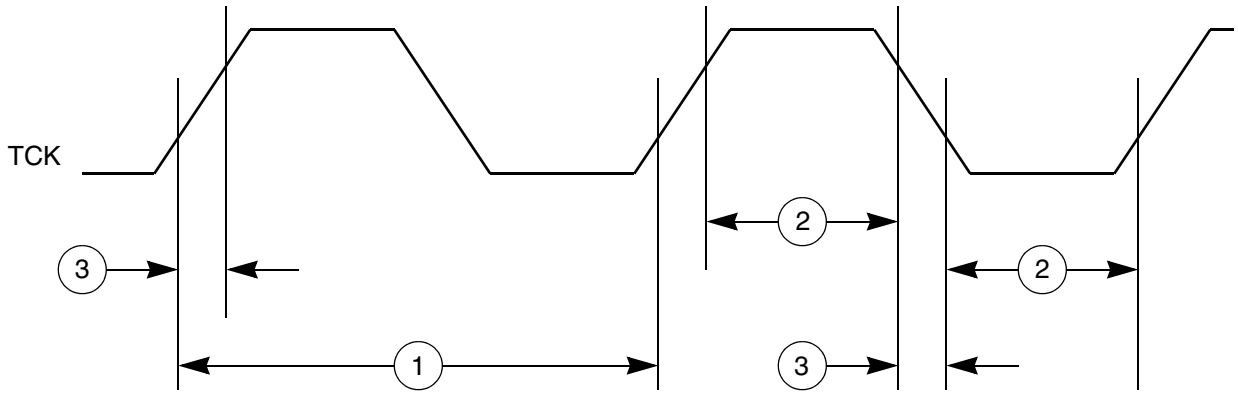

Figure 4. JTAG Test Clock Input Timing

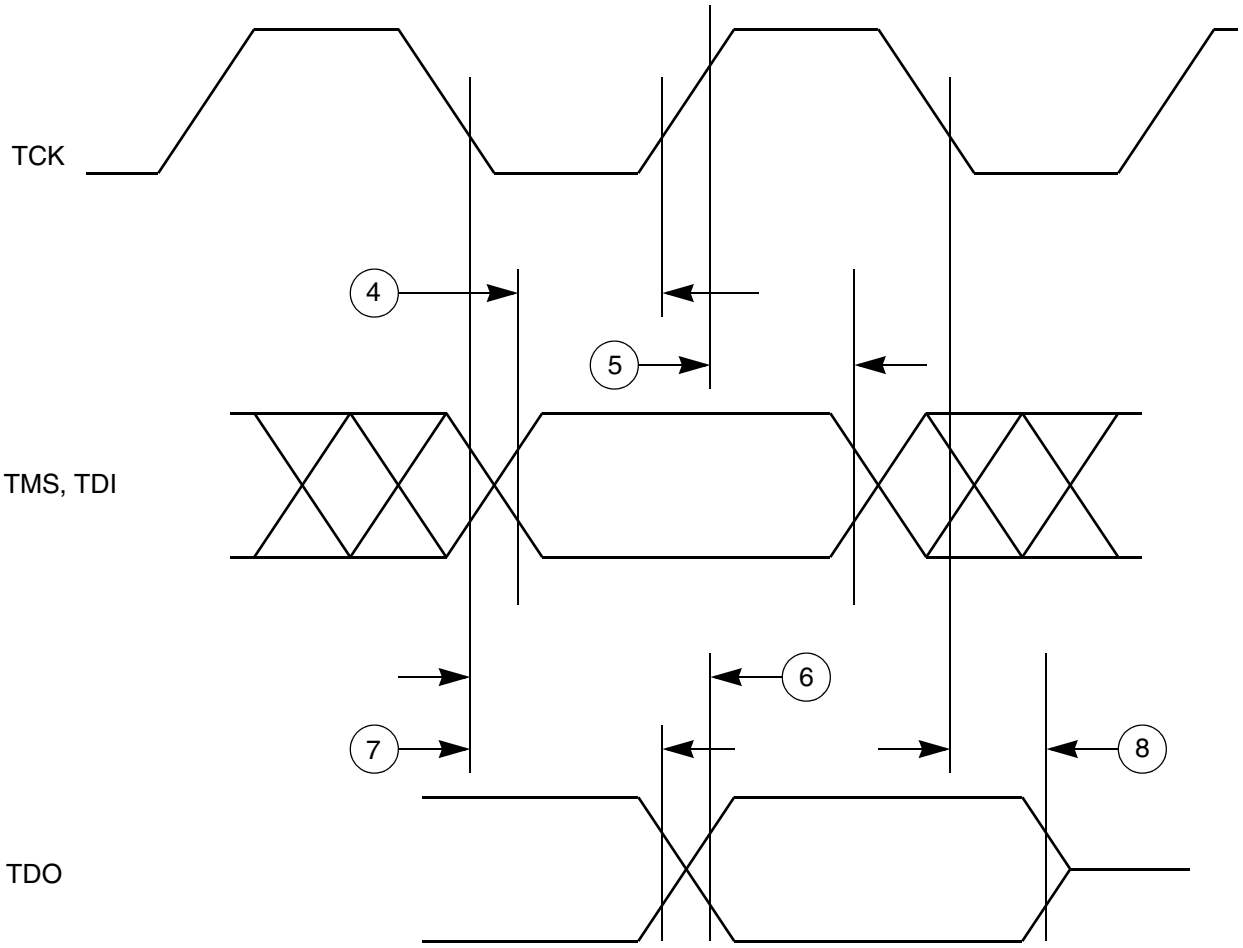

Figure 5. JTAG Test Access Port Timing

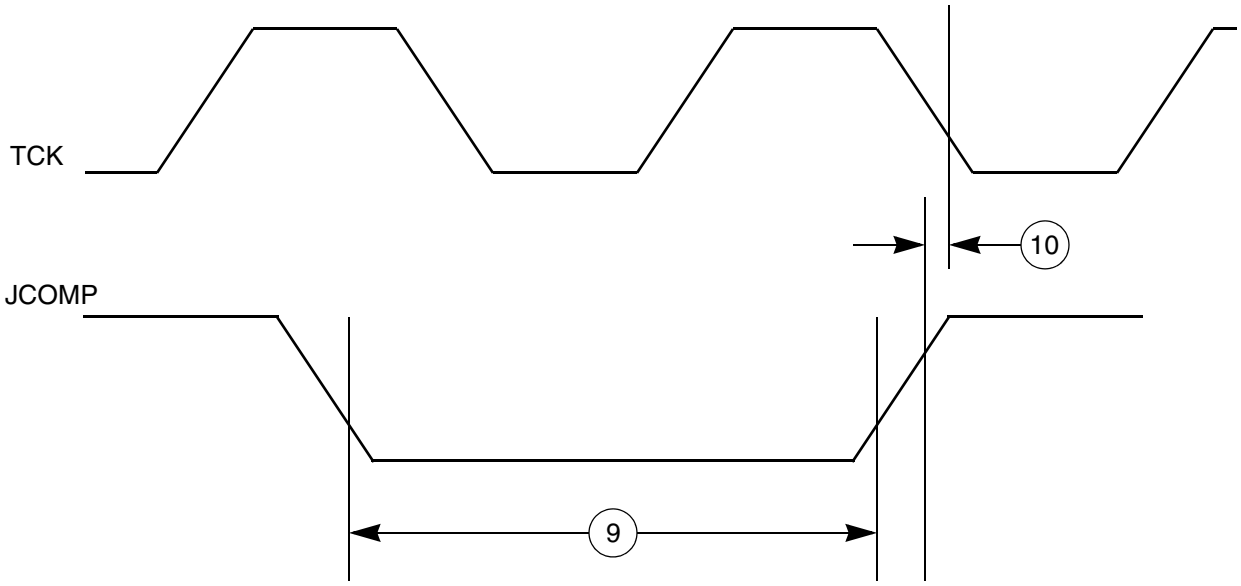

Figure 6. JTAG JCOMP Timing

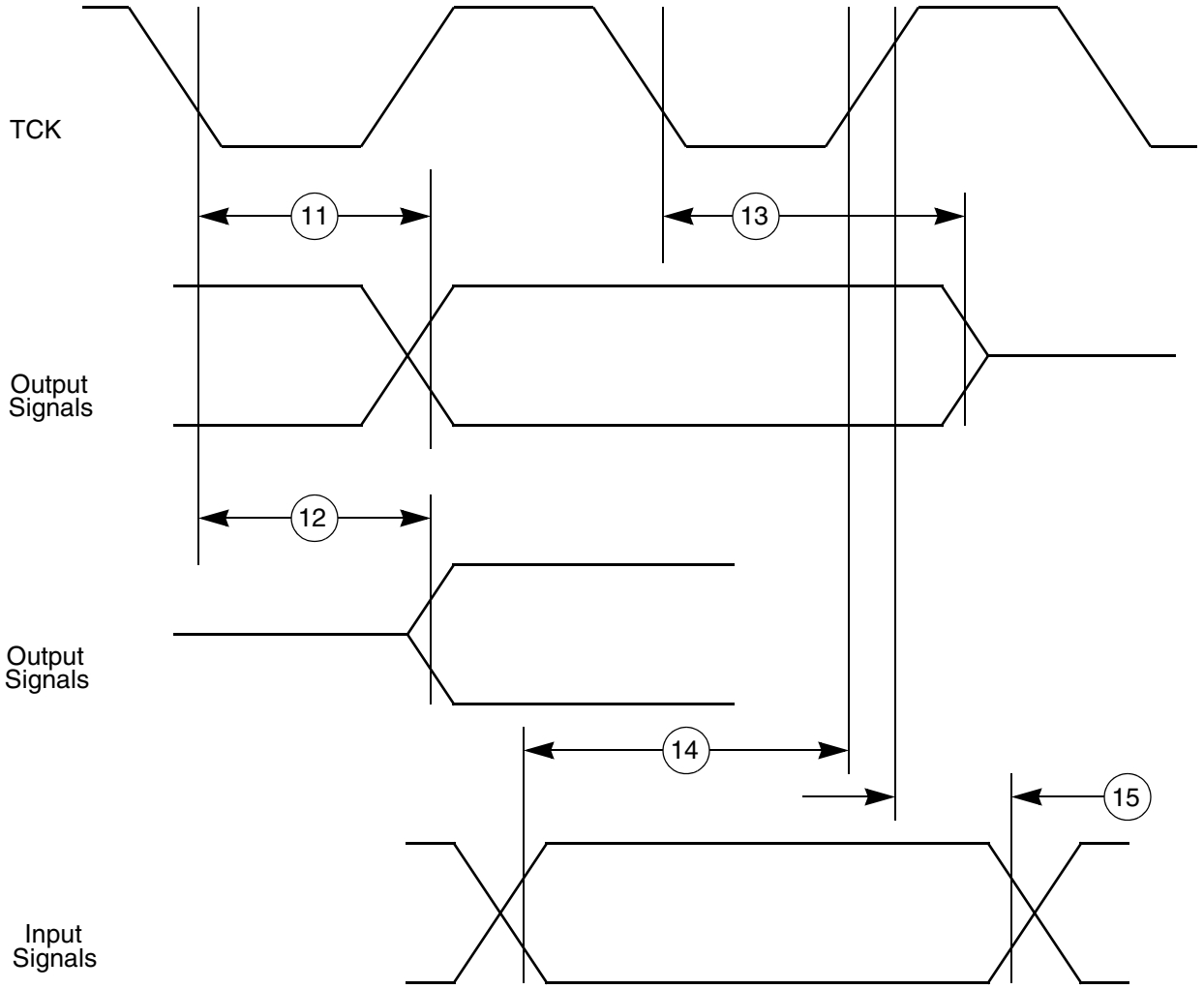

Figure 7. JTAG Boundary Scan Timing

2.13.3 Nexus Timing

Table 19. Nexus Debug Port Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	2	8	t_{CYC}
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[2]	t_{MDOV}	-1.5	3.0	ns
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[2]	t_{MSEOV}	-1.5	3.0	ns
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[2]	t_{EVTOV}	-1.5	3.0	ns
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	-	t_{TCYC}

Table 19. Nexus Debug Port Timing[1] (continued)

Num	Characteristic	Symbol	Min	Max	Unit
7	EVTO Pulse Width	t_{EVTOPW}	1		t_{MCYC}
8	TCK Cycle Time	t_{TCYC}	4[3]	-	t_{CYC}
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	-	ns
11	TDI, TMS Data Hold Time	t_{NTDIH}, t_{NTMSH}	5	-	ns
12	TCK Low to TDO Data Valid	t_{JOV}	0	12	ns
13	$\overline{RDY}$ Valid to MCKO[4]	-	-	-	-

NOTES:
[1]All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at VDD = 1.35V to 1.65V, VDDE = 2.25V to 3.6V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 30pF with DSC = 0b10.
[2]MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.
[3]The maximum frequency must be limited to approximately 30 MHz to meet the timing specification for t_{JOV} of 0.2 x t_{JCYC} as outlined in the IEEE-ISTO 5001-2003 specification.
[4]The $\overline{RDY}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

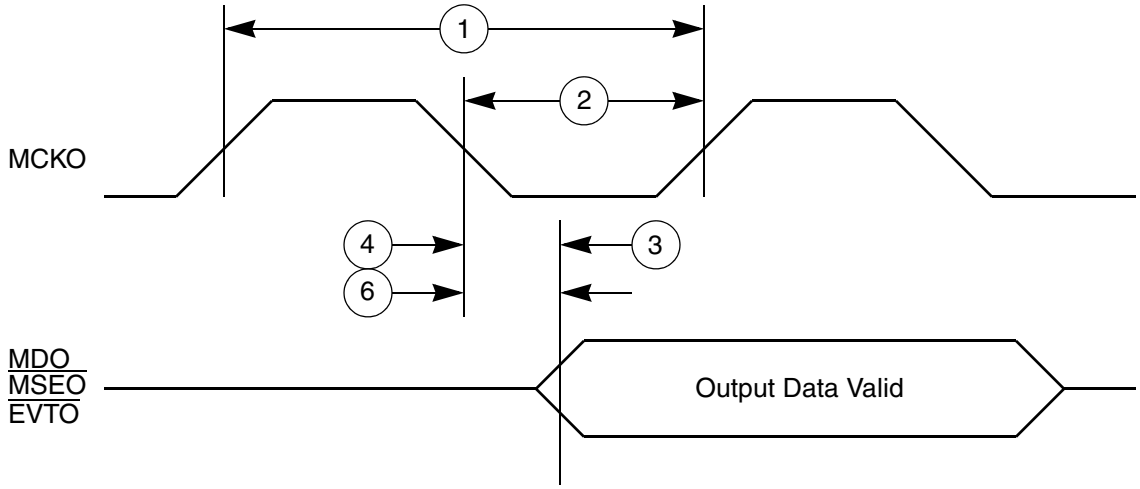

Figure 8. Nexus Output Timing

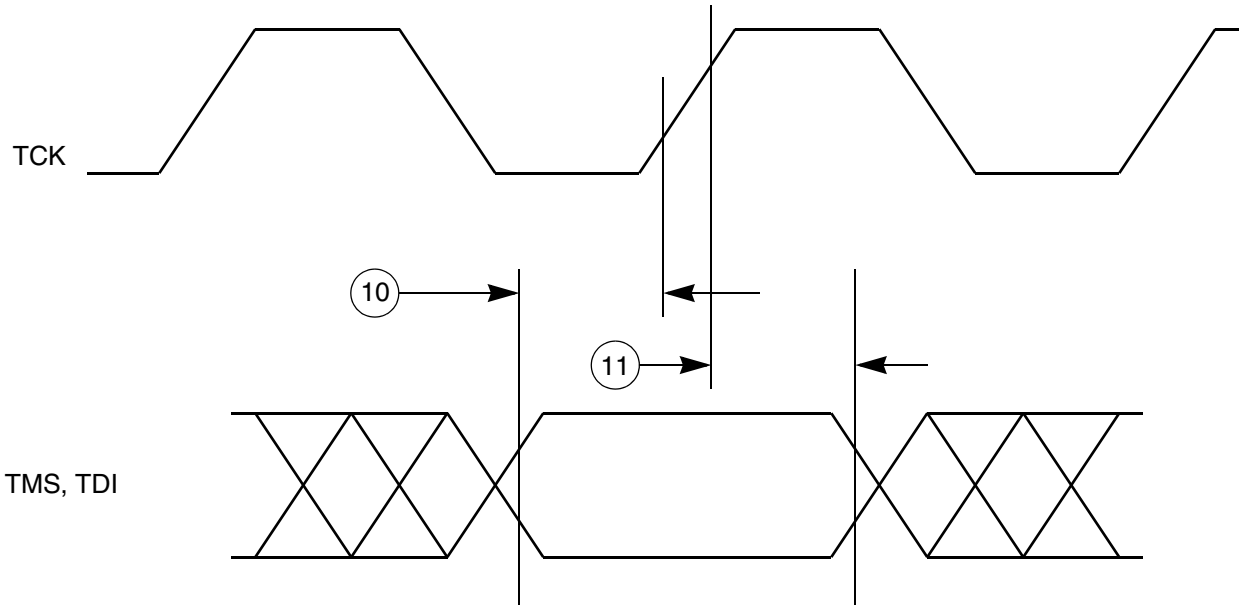

Figure 9. Nexus TDI, TMS Timing

2.13.4 External Bus Interface (EBI) Timing

Table 20. Bus Operation Timing[1]

#	Characteristic/Description	Symbol	40 MHz (ext. bus)[2]		56 MHz (ext. bus)[2]		66 MHz (ext. bus)[2]		Unit	Notes
			Min	Max	Min	Max	Min	Max		
1	CLKOUT Period	T_C	25.0	-	17.9	-	15.2	-	ns	Signals are measured at 50% VDDE.
2	CLKOUT duty cycle	t_{CDC}	45%	55%	45%	55%	45%	55%	T_C	
3	CLKOUT rise time	t_{CRT}	-	3	-	3	-	3	ns	
4	CLKOUT fall time	t_{CFT}	-	3	-	3	-	3	ns	

Table 20. Bus Operation Timing[1] (continued)

#	Characteristic/Description	Symbol	40 MHz (ext. bus)[2]		56 MHz (ext. bus)[2]		66 MHz (ext. bus)[2]		Unit	Notes
			Min	Max	Min	Max	Min	Max		
5	CLKOUT Posedge to Output Signal Invalid or High Z(Hold Time) ADDR[8:31] $\overline{BDIP}$ $\overline{BG}$[4] $\overline{BR}$[5] $\overline{CS}$[0:3] DATA[0:31] $\overline{OE}$ $\overline{RD\_WR}$ $\overline{TA}$ $\overline{TEA}$ $\overline{TS}$ TSIZ[0:1] $\overline{WE}$[0:3]/$\overline{BE}$[0:3]	t_{COH}	1.0[6]/ 1.5	-	1.0[6]/ 1.5	-	1.0[6]/ 1.5	-	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS=0/EBTS=1
6	CLKOUT Posedge to Output Signal Valid (Output Delay) ADDR[8:31] $\overline{BDIP}$ $\overline{BG}$[4] $\overline{BR}$[5] $\overline{CS}$[0:3] DATA[0:31] $\overline{OE}$ RD_$\overline{WR}$ $\overline{TA}$ $\overline{TEA}$ $\overline{TS}$ TSIZ[0:1] $\overline{WE}$[0:3]/$\overline{BE}$[0:3]	t_{COV}	-	10.0[6]/ 11.0	-	7.5[6]/ 8.5	-	6.0[6]/ 7.0	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS=0/EBTS=1
7	Input Signal Valid to CLKOUT Posedge (Setup Time) ADDR[8:31] $\overline{BB}$ $\overline{BG}$[5] $\overline{BR}$[5] DATA[0:31] RD_$\overline{WR}$ $\overline{TA}$ $\overline{TEA}$ $\overline{TS}$ TSIZ[0:1]	t_{CIS}	10.0	-	7.0	-	5.0	-	ns	

Table 20. Bus Operation Timing[1] (continued)

#	Characteristic/Description	Symbol	40 MHz (ext. bus)[2]		56 MHz (ext. bus)[2]		66 MHz (ext. bus)[2]		Unit	Notes
			Min	Max	Min	Max	Min	Max		
8	CLKOUT Posedge to Input Signal Invalid (Hold Time) ADDR[8:31] $\overline{BB}$ $\overline{BG}$[5] $\overline{BR}$[5] DATA[0:31] RD_$\overline{WR}$ $\overline{TA}$ $\overline{TEA}$ $\overline{TS}$ TSIZ[0:1]	t_{CIH}	1.0	-	1.0	-	1.0	-	ns	

NOTES:
[1]EBI timing specified at VDD = 1.35V to 1.65V, VDDE = 1.6V to 3.6V (unless stated otherwise), VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 30pF with DSC = 0b10.
[2]The external bus is limited to half the speed of the internal bus.
[3]Refer to Fast Pad timing in Table 15 and Table 16 (different values for 1.8V vs 3.3V).
[4]Internal Arbitration
[5]External Arbitration
[6]The EBTS=0 timings are only valid/ tested at VDDE=2.25-3.6V, whereas EBTS=1 timings are valid/tested at 1.6-3.6V.

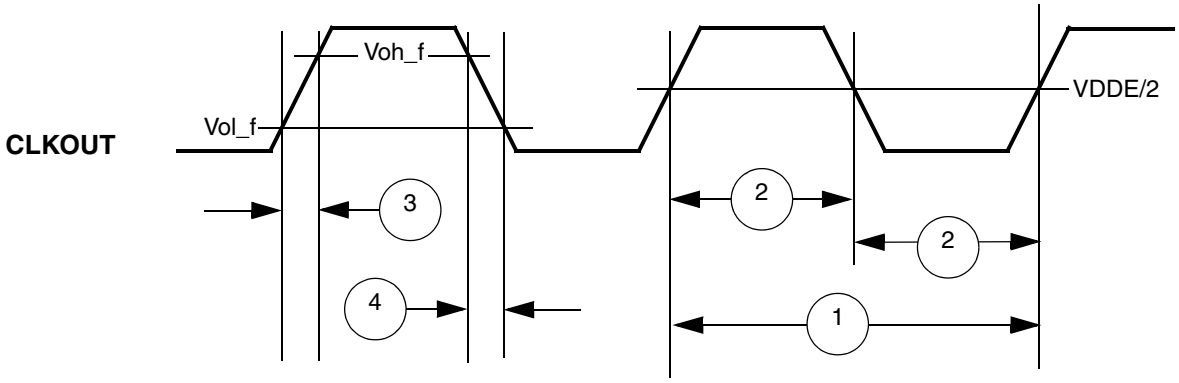

Figure 10. CLKOUT Timing

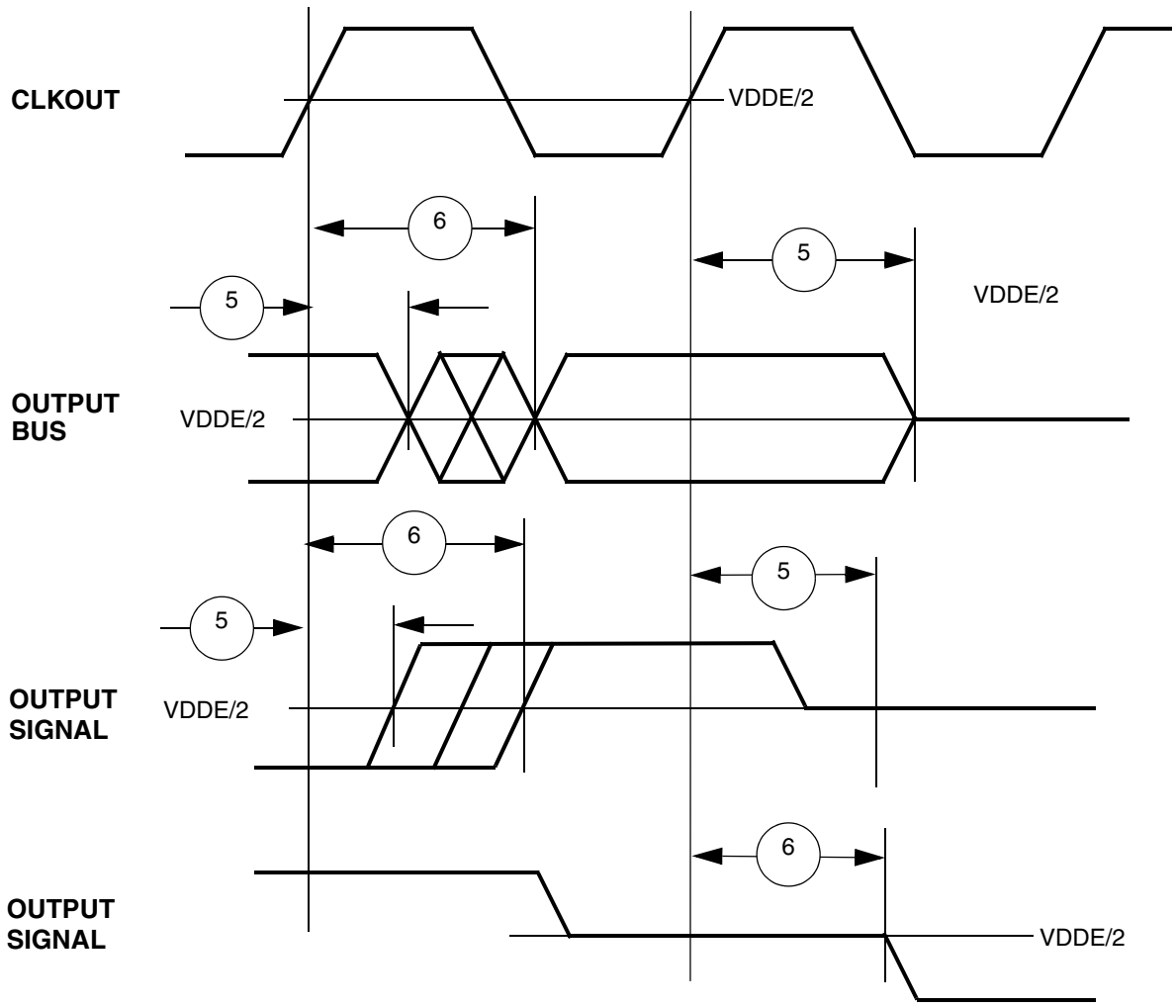

Figure 11. Synchronous Output Timing

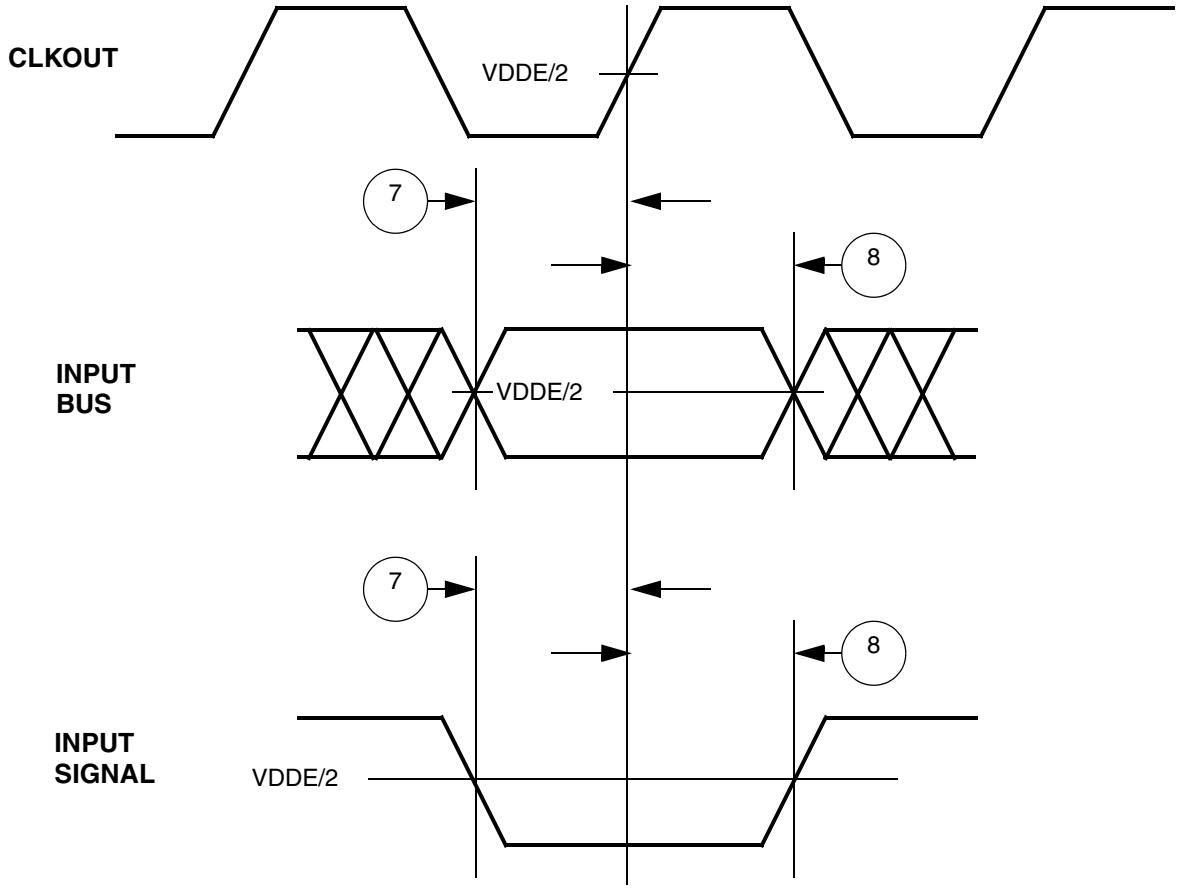

Figure 12. Synchronous Input Timing

2.13.5 External Interrupt Timing (IRQ Pin)

Table 21. External Interrupt Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	-	t_{CYC}
2	IRQ Pulse Width High	T_{IPWH}	3	-	t_{CYC}
3	IRQ Edge to Edge Time[2]	t_{ICYC}	6	-	t_{CYC}

NOTES:
[1]IRQ timing specified at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDEH = 3.0V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 200pF with SRC = 0b11.
[2]Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

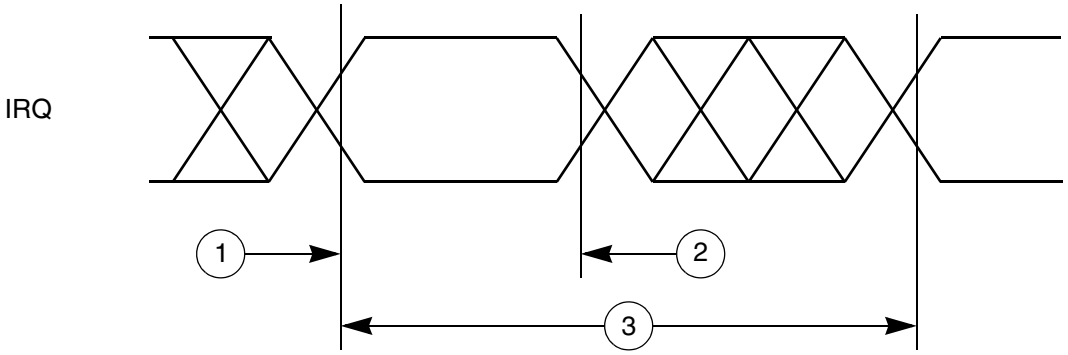

Figure 13. External Interrupt Timing

Figure 14. External Interrupt Setup Timing

2.13.6 eTPU Timing

Table 22. eTPU Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	-	t_{CYC}
2	eTPU Output Channel Pulse Width	t_{OCPW}	2	-	t_{CYC}

NOTES:
[1]eTPU timing specified at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDEH = 3.0V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 200pF with SRC = 0b11.

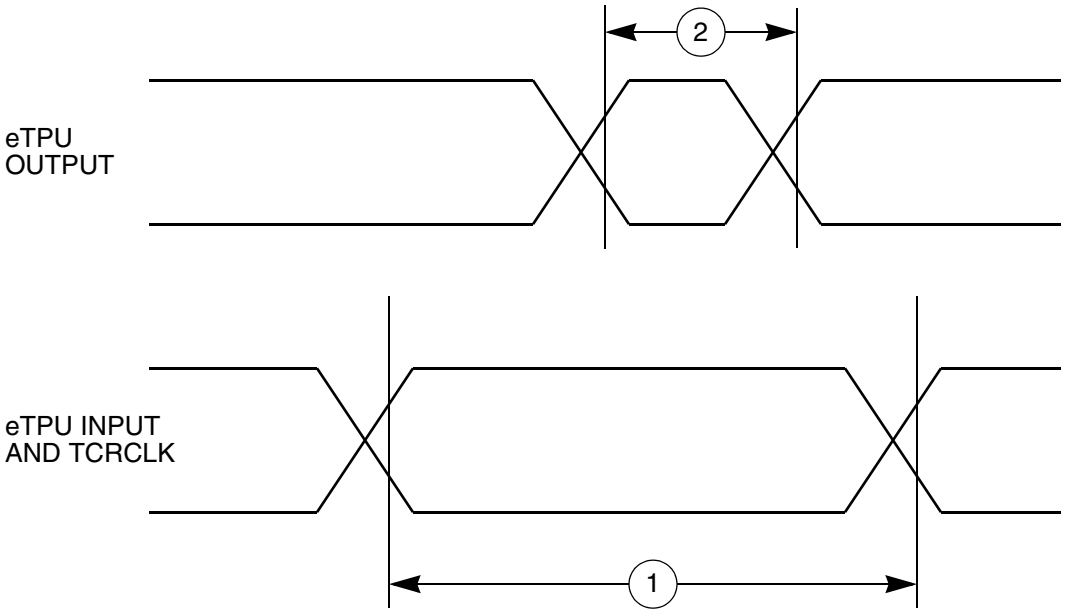

Figure 15. eTPU Timing

2.13.7 MTS (eMIOS) Timing

Table 23. MTS Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	MTS (eMIOS) Input Pulse Width	t_{MIPW}	4	-	t_{CYC}
2	MTS (eMIOS) Output Pulse Width	t_{MOPW}	1	-	t_{CYC}

NOTES:
[1]MTS timing specified at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDEH = 3.0V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 50pF with SRC = 0b11.

2.13.8 DSPI Timing

Table 24. DSPI Timing[1]

Num	Characteristic	Symbol	80 MHz		112 MHz		132 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	SCK Cycle TIme[2,3]	t_{SCK}	25ns	2.9ms	17.9ns	2.0ms	15.2ns	1.7ms	-
2	PCS to SCK Delay[4]	t_{CSC}	23	-	15	-	13	-	ns
3	After SCK Delay[5]	t_{ASC}	22	-	14	-	12	-	ns
4	SCK Duty Cycle	t_{SDC}	$t_{SCK}/2$ - 2ns	$t_{SCK}/2$ + 2ns	-	-	-	-	ns

Table 24. DSPI Timing[1] (continued)

Num	Characteristic	Symbol	80 MHz		112 MHz		132 MHz		Unit
			Min	Max	Min	Max	Min	Max	
5	Slave Access Time ($\overline{SS}$ active to SOUT driven)	t_A	-	23	-	23	-	23	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	-	19	-	19	-	19	ns
7	PCSx to $\overline{PCSS}$ time	t_{PCSC}	4	-	4	-	4	-	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	5	-	5	-	5	-	ns
9	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	t_{SUI}	 20 2 -4 20	 - - - -	 20 2 3 20	 - - - -	 20 2 6 20	 - - - -	 ns ns ns ns
10	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	t_{HI}	 -4 7 21 -4	 - - - -	 -4 7 14 -4	 - - - -	 -4 7 12 -4	 - - - -	 ns ns ns ns
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA=0) Master (MTFE = 1, CPHA=1)	t_{SUO}	 - - - -	 5 25 18 5	 - - - -	 5 25 14 5	 - - - -	 5 25 13 5	ns ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{HO}	 -5 6 8 -5	 - - - -	 -5 6 4 -5	 - - - -	 -5 6 3 -5	 - - - -	 ns ns ns ns

NOTES:
[1]DSPI timing specified at VDD = 1.35V to 1.65V, VDDEH = 3.0V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 50pF with SRC = 0b11.

[2]The minimum SCK Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC5554 devices communicating over a DSPI link.

[3] The actual minimum SCK Cycle Time is limited by pad performance.

[4] The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]

[5] The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC]

[6]This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

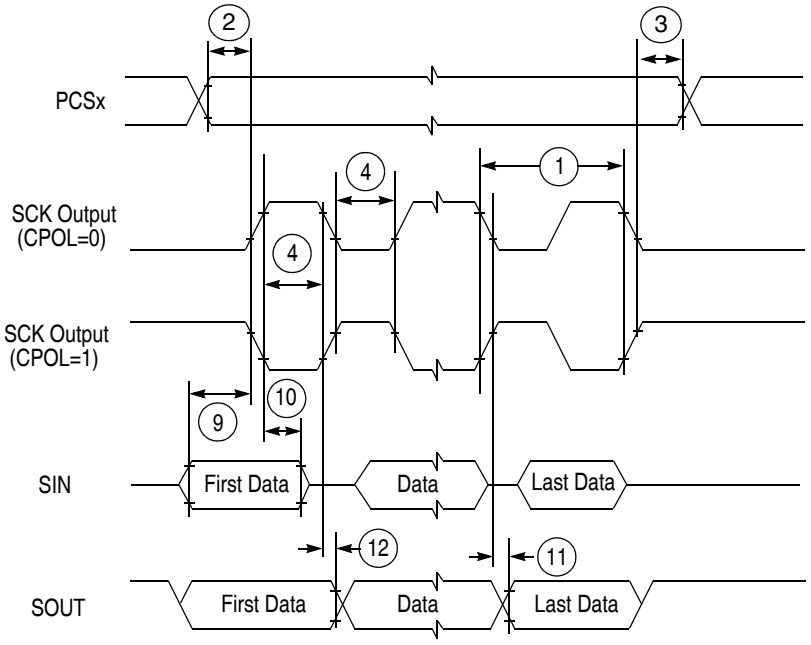

Figure 16. DSPI Classic SPI Timing - Master, CPHA = 0

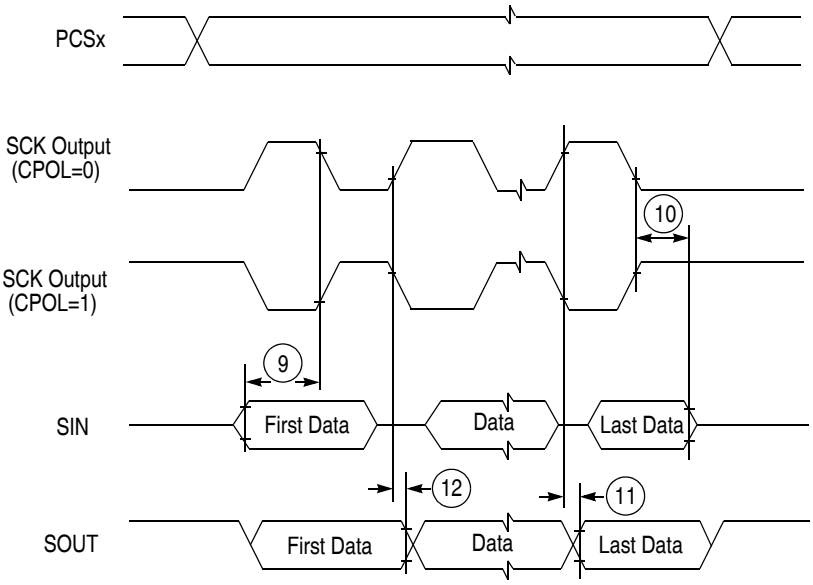

Figure 17. DSPI Classic SPI Timing - Master, CPHA = 1

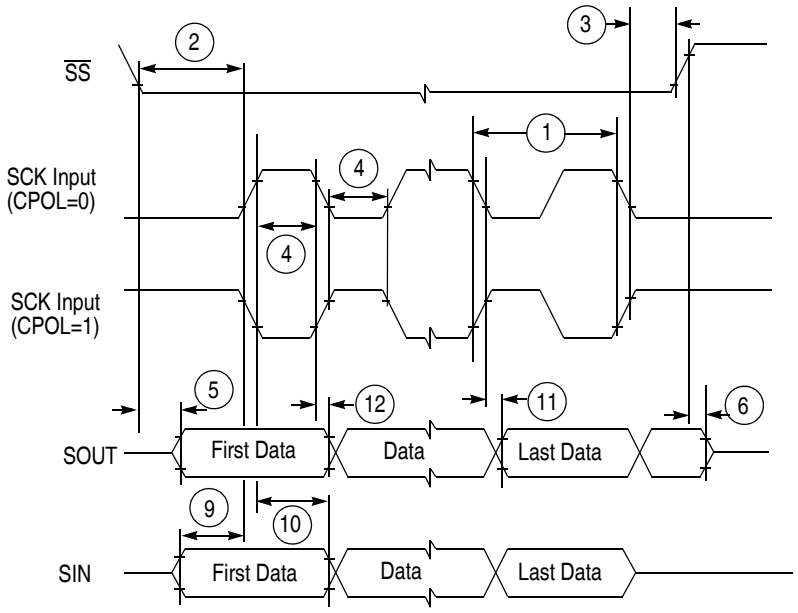

Figure 18. DSPI Classic SPI Timing - Slave, CPHA = 0

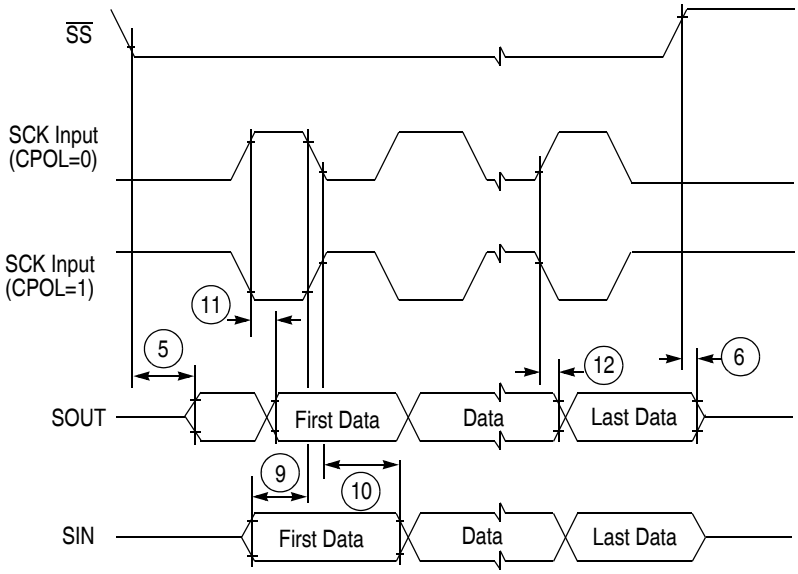

Figure 19. DSPI Classic SPI Timing - Slave, CPHA = 1

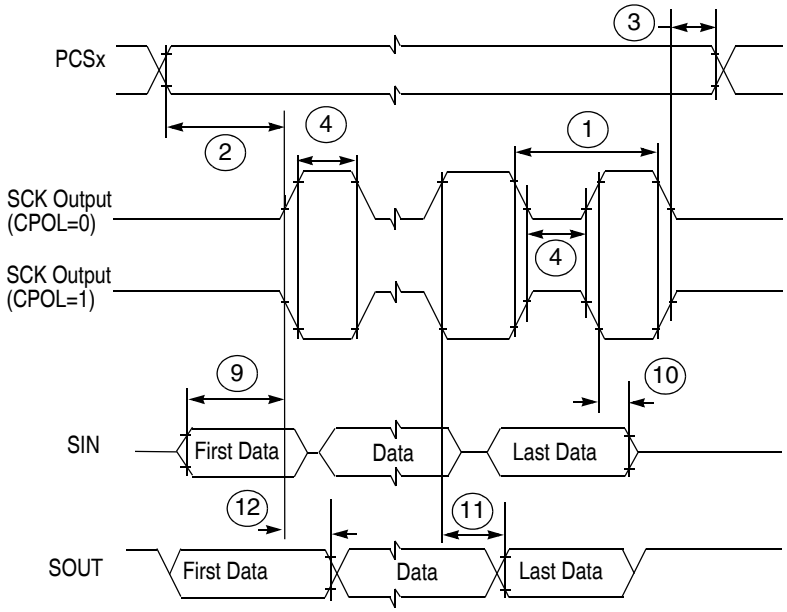

Figure 20. DSPI Modified Transfer Format Timing - Master, CPHA = 0

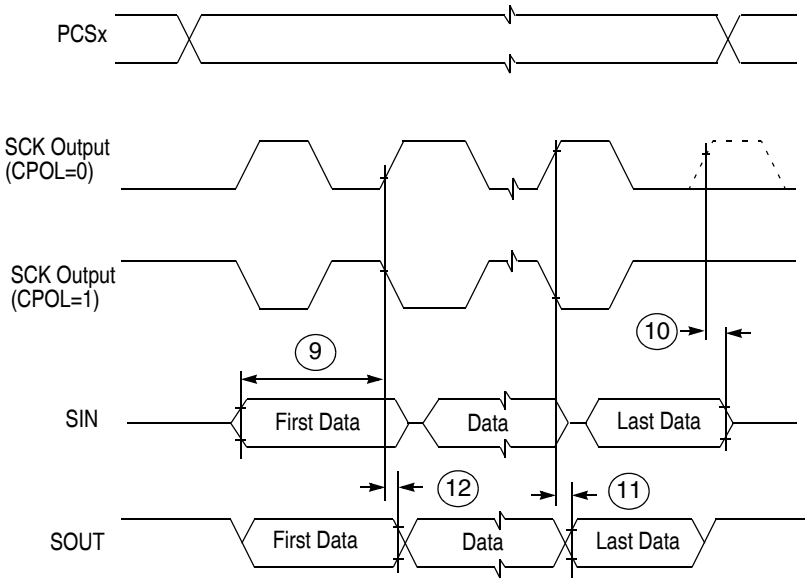

Figure 21. DSPI Modified Transfer Format Timing - Master, CPHA = 1

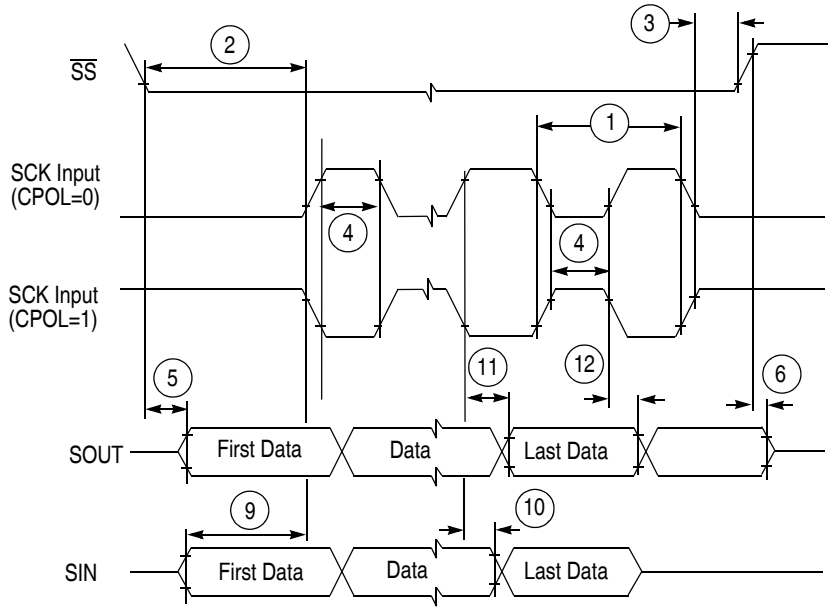

Figure 22. DSPI Modified Transfer Format Timing - Slave, CPHA =0

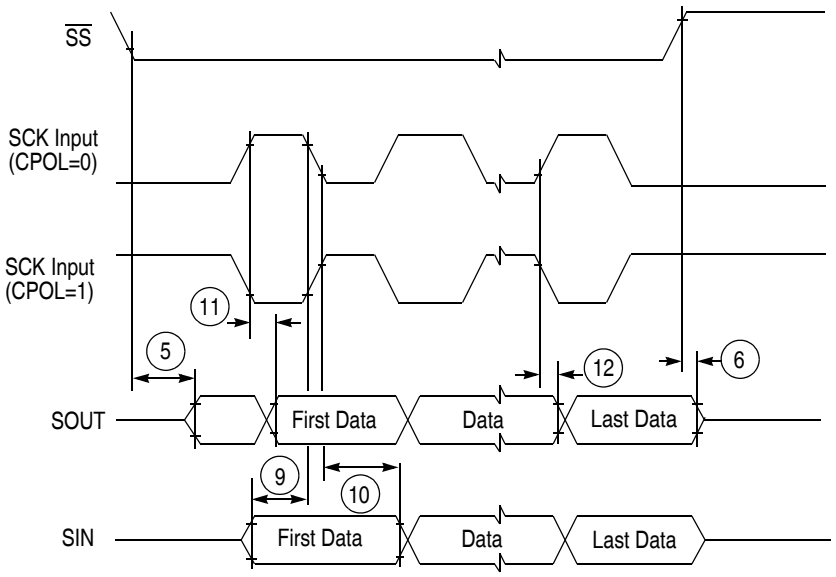

Figure 23. DSPI Modified Transfer Format Timing - Slave, CPHA =1

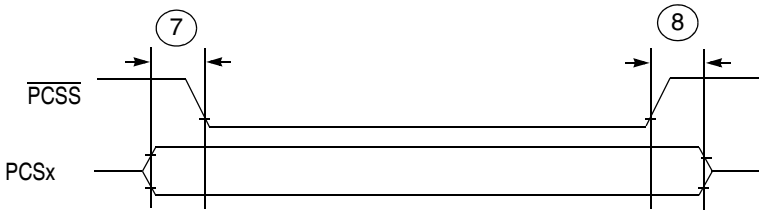

Figure 24. DSPI PCS Strobe ($\overline{PCSS}$) Timing

2.13.9 EQADC SSI Timing

Table 25. EQADC SSI Timing Characteristics (pads at 3.3V or at 5.0V) [1]

CLOAD = 25pF on all outputs. Pad drive strength set to maximum.						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	FCK Frequency [2, 3]	f_{FCK}	1/17	-	1/2	f_{SYS_CLK}
2	FCK Period (t_{FCK} = 1/ f_{FCK})	t_{FCK}	2	-	17	t_{SYS_CLK}
3	Clock (FCK) High Time	t_{FCKHT}	t_{SYS_CLK} − 6.5	-	9* t_{SYS_CLK} + 6.5	ns
4	Clock (FCK) Low Time	t_{FCKLT}	t_{SYS_CLK} − 6.5	-	8* t_{SYS_CLK} + 6.5	ns
5	SDS Lead/Lag Time	t_{SDS_LL}	-7.5	-	+7.5	ns
6	SDO Lead/Lag Time	t_{SDO_LL}	-7.5	-	+7.5	ns
7	EQADC Data Setup Time (Inputs)	t_{EQ_SU}	22	-	-	ns
8	EQADC Data Hold Time (Inputs)	t_{EQ_HO}	1	-	-	ns

NOTES:
[1]SS timing specified at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDEH = 3.0V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 50pF with SRC = 0b11.
[2]Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.
[3]FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

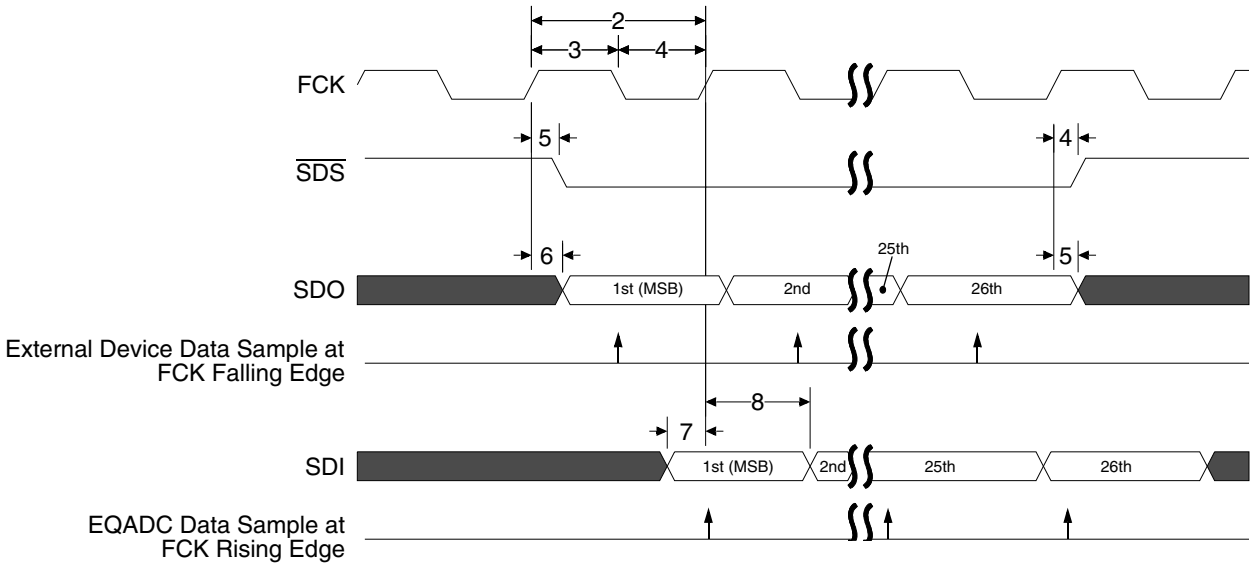

Figure 25. EQADC SSI Timing

3 Mechanicals

3.1 Pinouts

3.1.1 MPC5554 416 PBGA Pinout

Figure 26 is a pinout for the MPC5554 416 PBGA package.

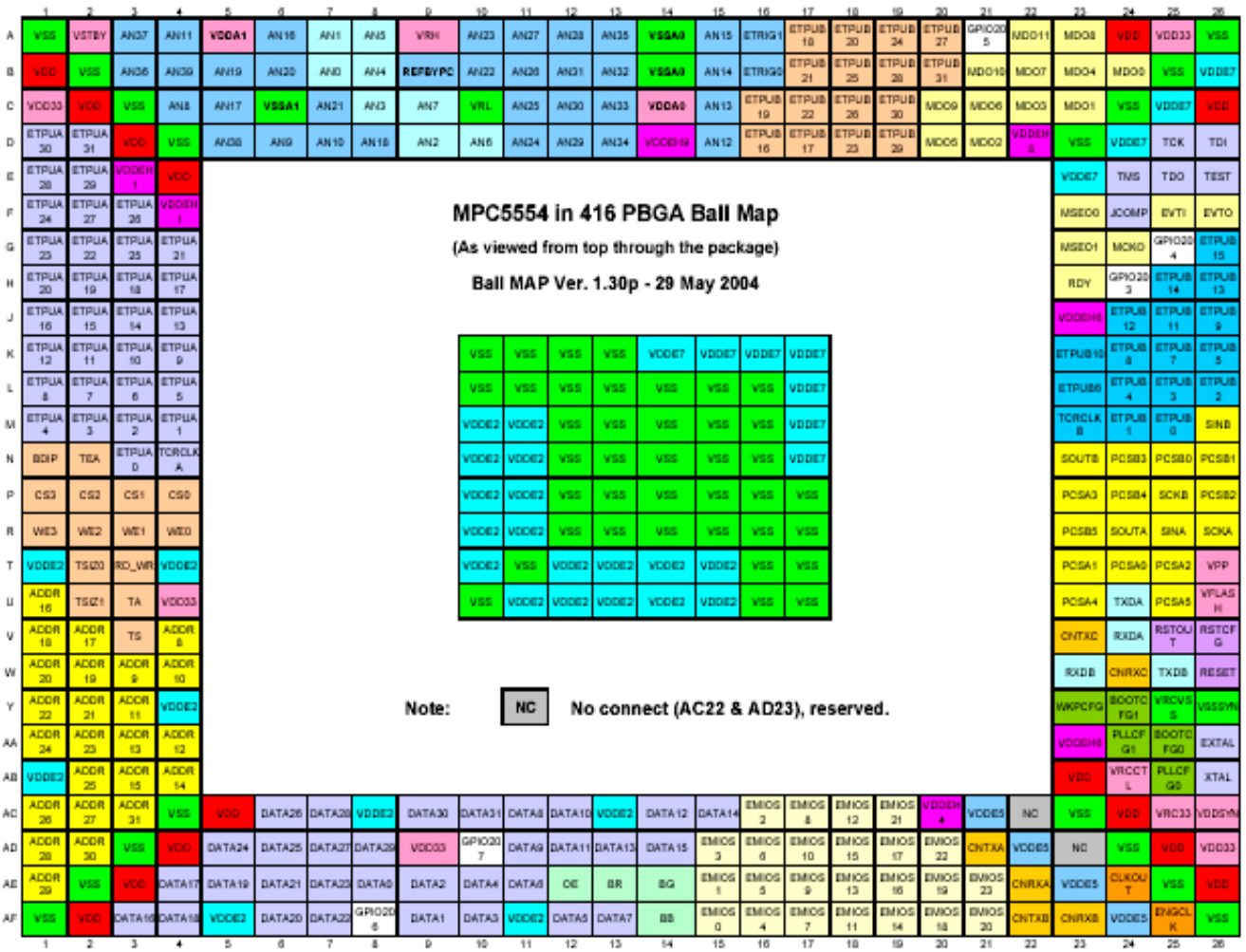

Figure 26. MPC5554 Pinout Diagram

3.2 Package Dimensions

3.2.1 MPC5554 416 Pin Package

Figure 27 is a package drawing of the MPC5554 416 pin TEPBGA package.

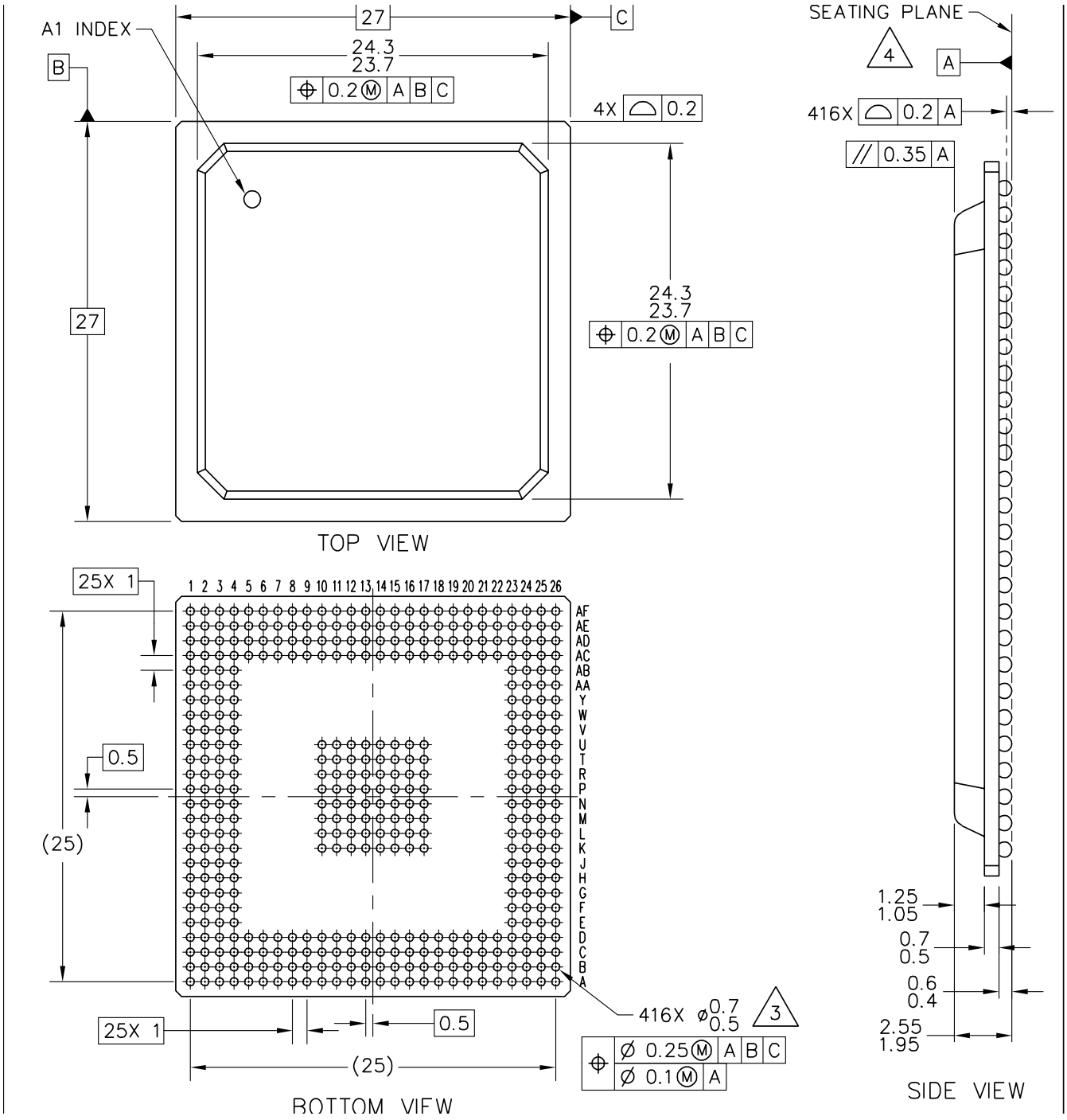

Figure 27. MPC5554 416 TEPBGA Package

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