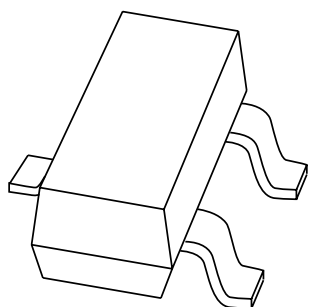


DATA SHEET



BSS84

P-channel enhancement mode
vertical D-MOS transistor

Product specification
Supersedes data of 1997 Jun 18

2003 Aug 04

P-channel enhancement mode vertical
D-MOS transistor

BSS84

FEATURES

- Low threshold voltage
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high speed and line transformer drivers.

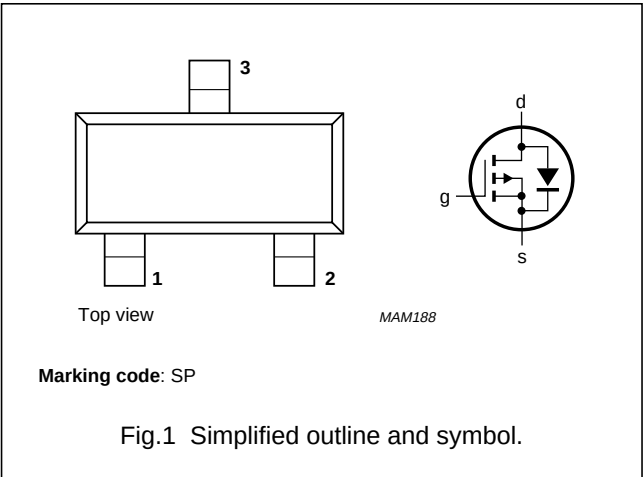
DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport and handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	–	± 20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1\text{ mA}$; $V_{DS} = V_{GS}$	–0.8	–	–2	V
I_D	drain current (DC)		–	–	–130	mA
R_{DSon}	drain-source on-state resistance	$I_D = -130\text{ mA}$; $V_{GS} = -10\text{ V}$	–	6	10	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$	–	–	250	mW

P-channel enhancement mode vertical D-MOS transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	± 20	V
I_D	drain current (DC)		–	–130	mA
I_{DM}	peak drain current		–	–520	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	500	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board.

CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = -10\text{ }\mu\text{A}$	–50	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = -1\text{ mA}$	–0.8	–	–2	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = -40\text{ V}$	–	–	–100	nA
		$V_{GS} = 0$; $V_{DS} = -50\text{ V}$	–	–	–10	μA
		$V_{GS} = 0$; $V_{DS} = -50\text{ V}$; $T_j = 125\text{ °C}$	–	–	–60	μA
I_{GSS}	gate leakage current	$V_{DS} = 0$; $V_{GS} = \pm 20\text{ V}$	–	–	± 100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10\text{ V}$; $I_D = -130\text{ mA}$	–	6	10	Ω
$ y_{fs} $	forward transfer admittance	$V_{DS} = -25\text{ V}$; $I_D = -130\text{ mA}$	50	–	–	mS
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = -25\text{ V}$; $f = 1\text{ MHz}$	–	25	45	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = -25\text{ V}$; $f = 1\text{ MHz}$	–	15	25	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = -25\text{ V}$; $f = 1\text{ MHz}$	–	3.5	12	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0\text{ to }-10\text{ V}$; $V_{DD} = -40\text{ V}$; $I_D = -200\text{ mA}$	–	3	–	ns
t_{off}	turn-off time	$V_{GS} = -10\text{ to }0\text{ V}$; $V_{DD} = -40\text{ V}$; $I_D = -200\text{ mA}$	–	7	–	ns

P-channel enhancement mode vertical
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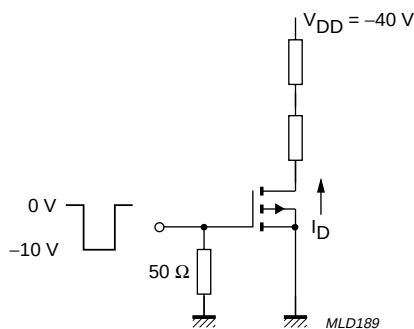


Fig.2 Switching time test circuit.

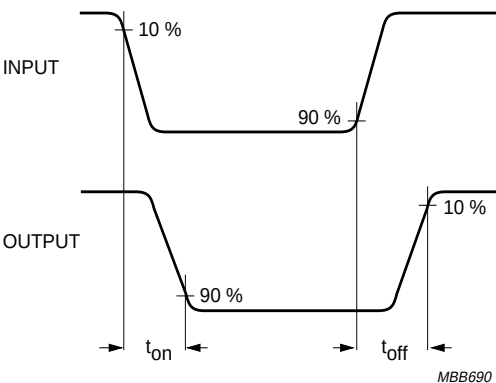


Fig.3 Input and output waveforms.

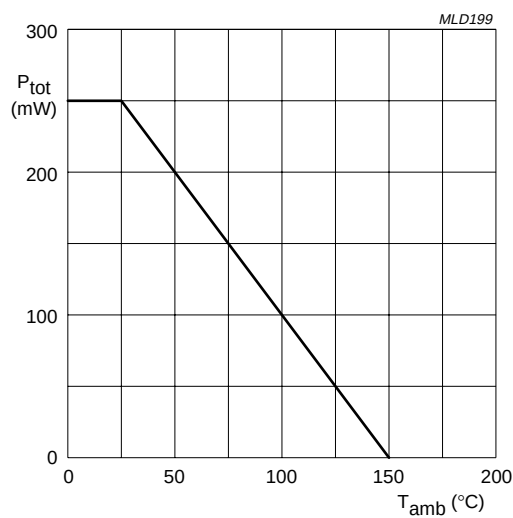
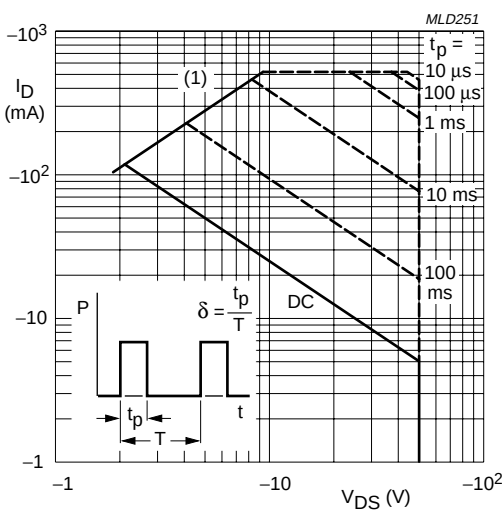


Fig.4 Power derating curve.

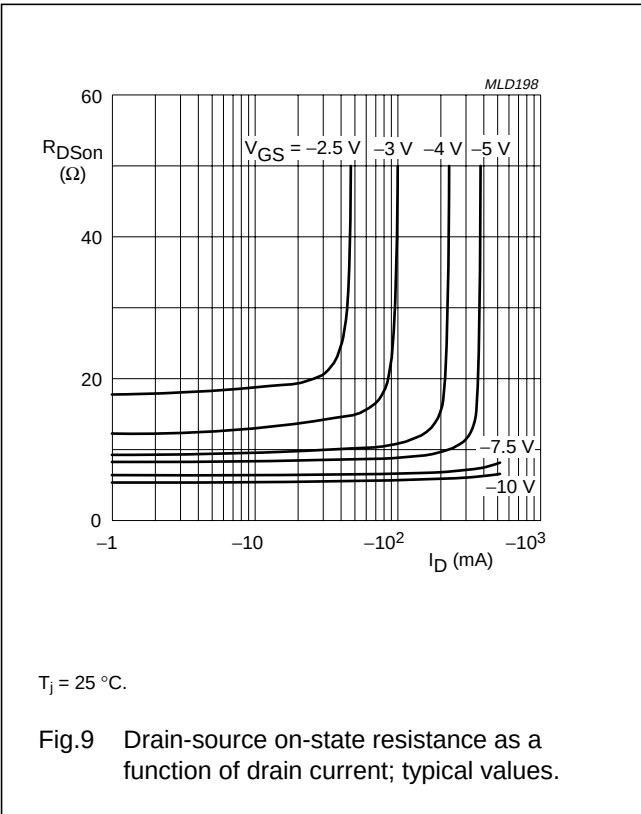
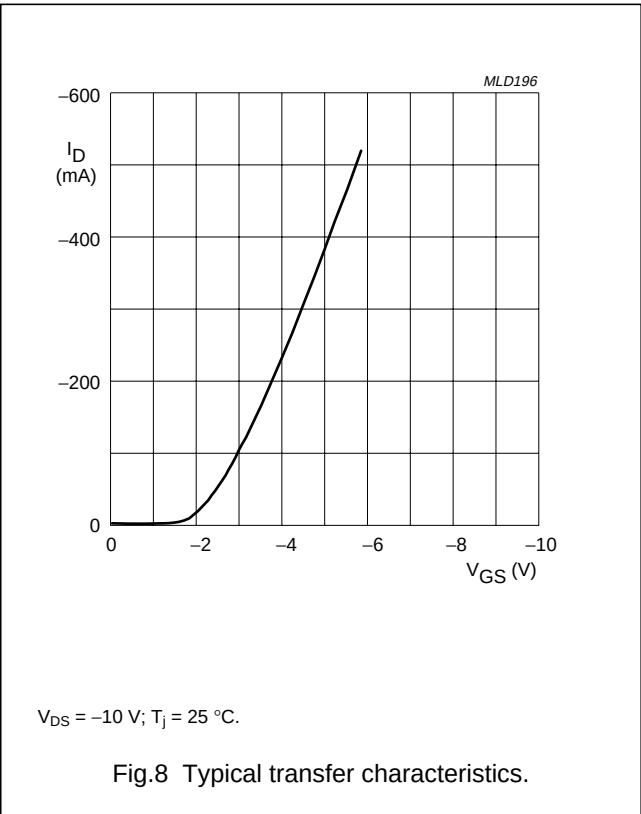
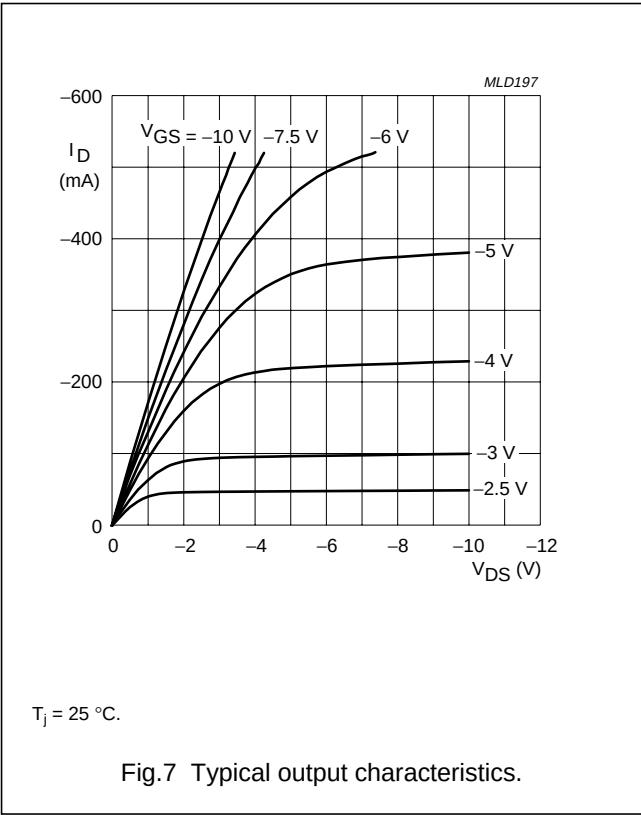
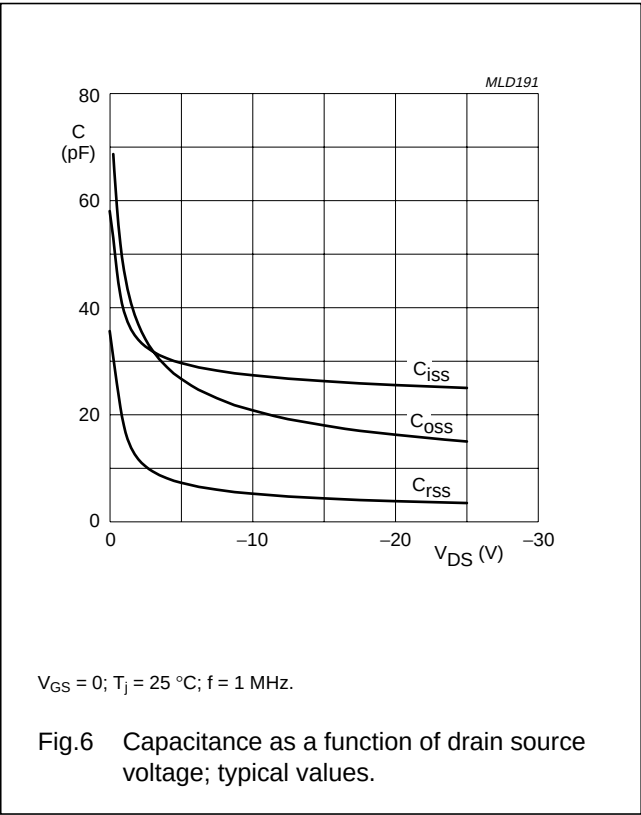


$\delta = 0.01$.
 $T_{amb} = 25\text{ }^{\circ}\text{C}$.
(1) R_{DSon} limitation.

Fig.5 DC SOAR.

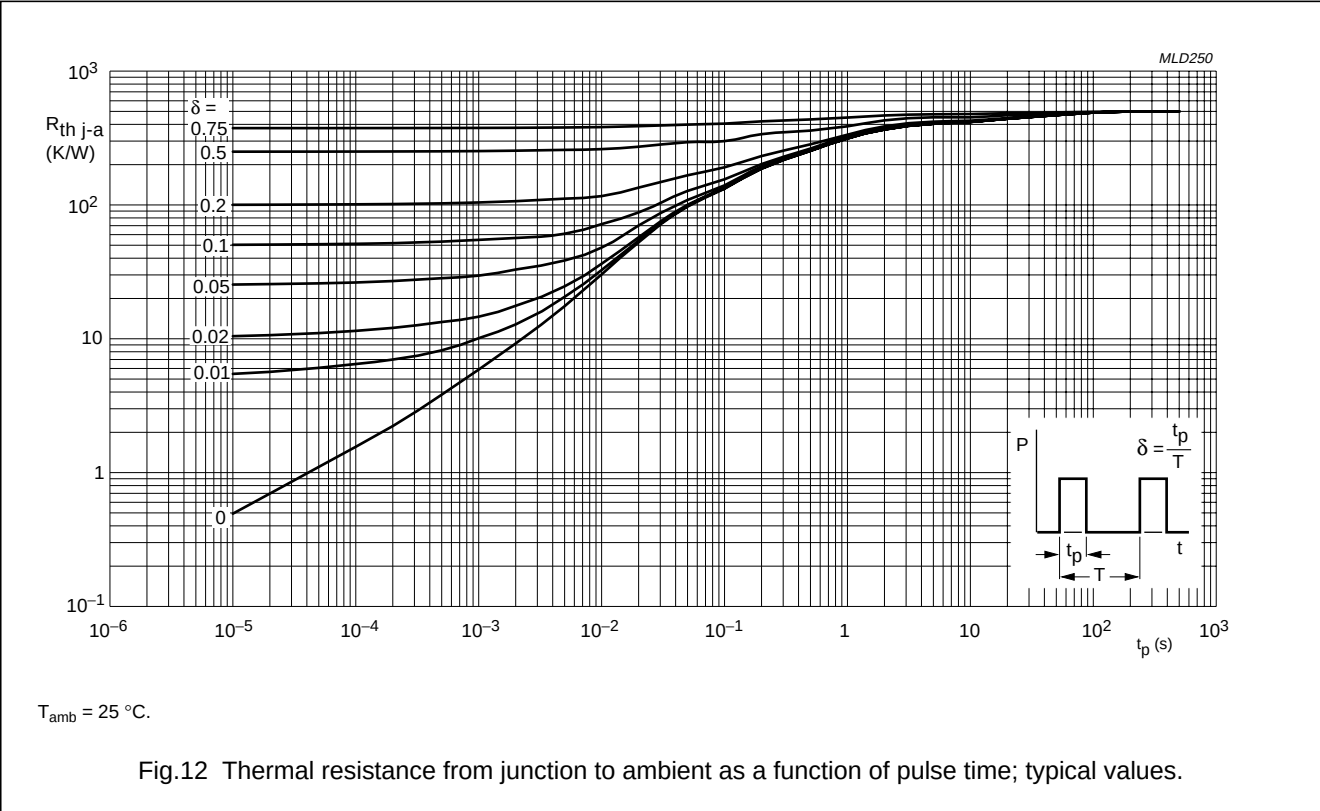
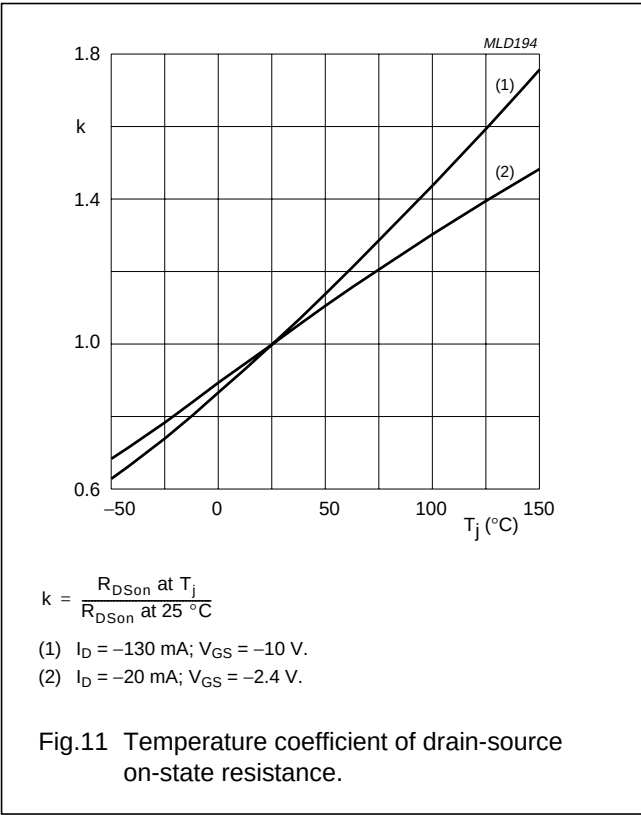
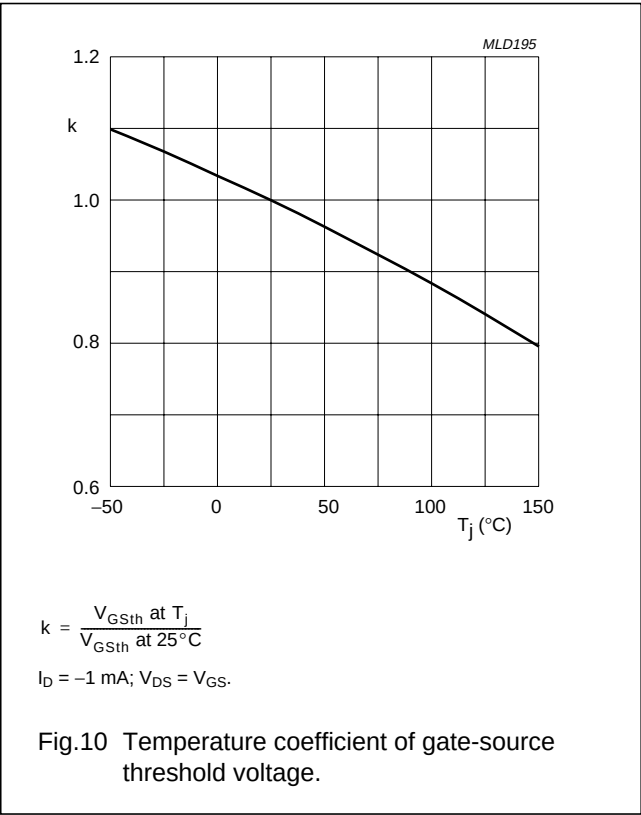
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D-MOS transistor

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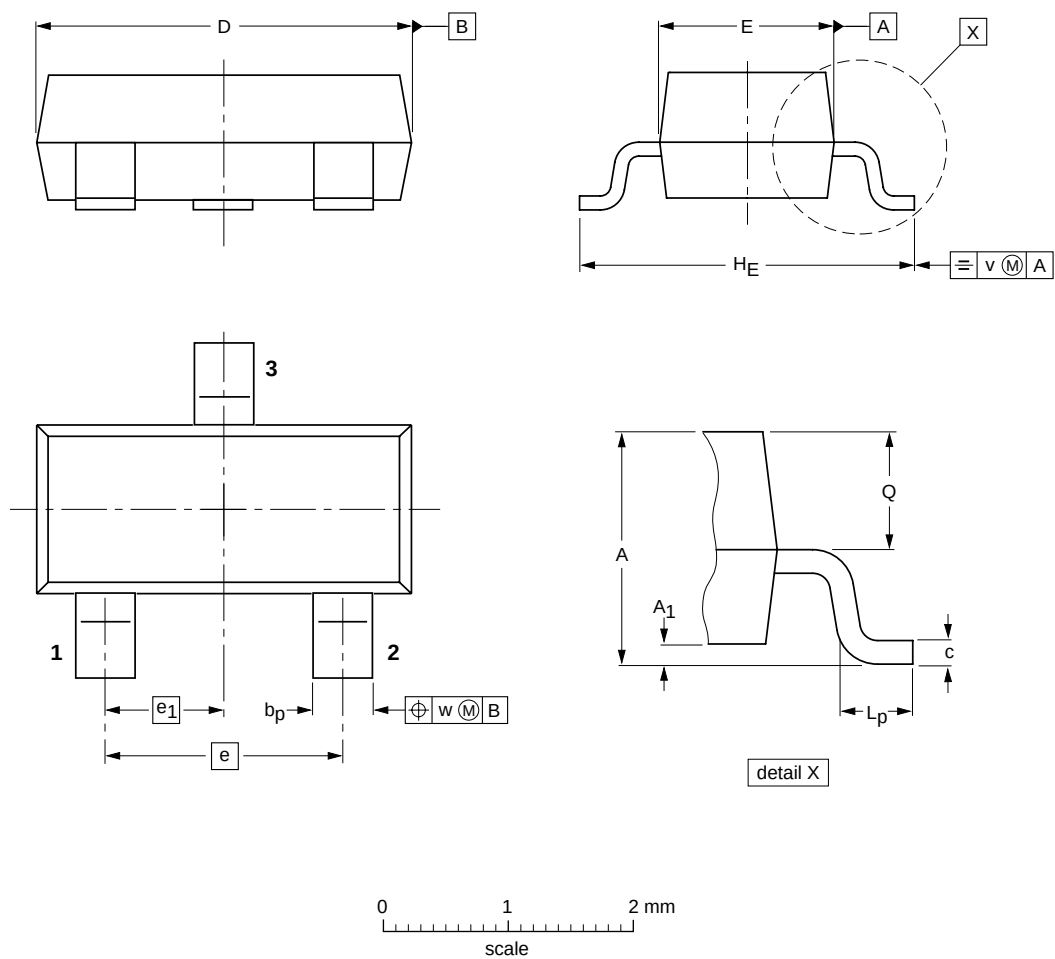
P-channel enhancement mode vertical
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PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23		TO-236AB				97-02-28 99-09-13

P-channel enhancement mode vertical D-MOS transistor

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LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
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