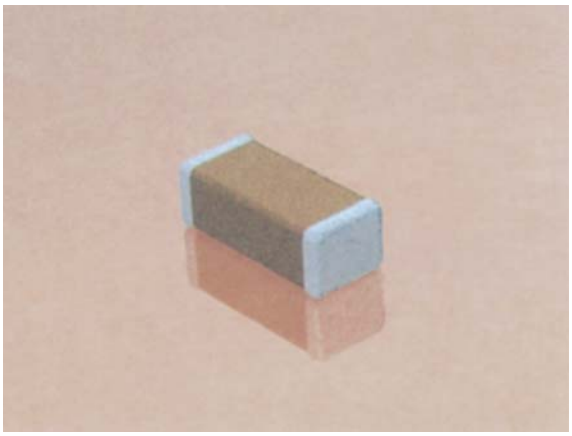
High Voltage MLC Chips

For 600V to 5000V Application



High value, low leakage and small size are difficult parameters to obtain in capacitors for high voltage systems. AVX special high voltage MLC chips capacitors meet these performance characteristics and are designed for applications such as snubbers in high frequency power converters, resonators in SMPS, and high voltage coupling/DC blocking. These high voltage chip designs exhibit low ESRs at high frequencies.

Larger physical sizes than normally encountered chips are used to make high voltage chips. These larger sizes require that special precautions be taken in applying these chips in surface mount assemblies. This is due to differences in the coefficient of thermal expansion (CTE) between the substrate materials and chip capacitors. Apply heat at less than 4°C per second during the preheat. The preheat temperature must be within 50°C of the peak temperature reached by the ceramic bodies through the soldering process. Chips 1808 and larger to use reflow soldering only.

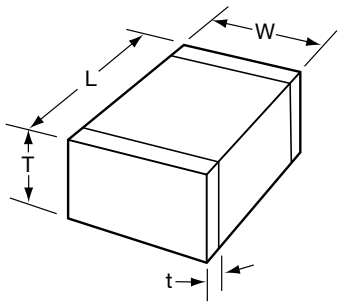
Capacitors may require protective surface coating to prevent external arcing.

HOW TO ORDER

1808	A	A	271	K	A	1	1	A
AVX Style	**Voltage**	**Temperature Coefficient**	**Capacitance Code** (2 significant digits + no. of zeros)	**Capacitance Tolerance**	**Test Level**	**Termination***	**Packaging**	**Special Code**
1206	600V = C	C0G = A	Examples:	C0G: J = ±5%	A = Standard	1 = Pd/Ag	1 = 7" Reel	A = Standard
1210	1000V = A	X7R = C	10 pF = 100	K = ±10%		T = Plated	3 = 13" Reel	
1808	1500V = S		100 pF = 101	M = ±20%		Ni and Sn	9 = Bulk	
1812	2000V = G		1,000 pF = 102	X7R: K = ±10%		J = 5% Min Pb		
1825	2500V = W		22,000 pF = 223	M = ±20%				
2220	3000V = H		220,000 pF = 224	Z = +80%, -20%				
2225	4000V = J		1 µF = 105					
3640	5000V = K							

***Note:** Leaded terminations are available.
Styles 1825, 2225, & 3640 are available with "N", "L" or "J" leads as seen on page 9.
"V" denotes uncoated leaded units similar to SM0 product.
"W" denotes leaded epoxy coated units similar to SM5 product.
IE 1825AA103KAV00J would be uncoated leaded part with "J" style leads.

Note: Capacitors with X7R dielectrics are not intended for applications across AC supply mains or AC line filtering with polarity reversal. Contact plant for recommendations.



DIMENSIONS

millimeters (inches)

SIZE	1206	1210	1808*	1812*	1825*	2220*	2225*	3640*
(L) Length	3.20 ± 0.2 (0.126 ± 0.008)	3.20 ± 0.2 (0.126 ± 0.008)	4.57 ± 0.25 (0.180 ± 0.010)	4.50 ± 0.3 (0.177 ± 0.012)	4.50 ± 0.3 (0.177 ± 0.012)	5.7 ± 0.4 (0.224 ± 0.016)	5.72 ± 0.25 (0.225 ± 0.010)	9.14 ± 0.25 (0.360 ± 0.010)
(W) Width	1.60 ± 0.2 (0.063 ± 0.008)	2.50 ± 0.2 (0.098 ± 0.008)	2.03 ± 0.25 (0.080 ± 0.010)	3.20 ± 0.2 (0.126 ± 0.008)	6.40 ± 0.3 (0.252 ± 0.012)	5.0 ± 0.4 (0.197 ± 0.016)	6.35 ± 0.25 (0.250 ± 0.010)	10.2 ± 0.25 (0.400 ± 0.010)
(T) Thickness Max.	1.52 (0.060)	1.70 (0.067)	2.03 (0.080)	2.54 (0.100)	2.54 (0.100)	3.3 (0.130)	2.54 (0.100)	2.54 (0.100)
(t) terminal min.	0.25 (0.010)	0.25 (0.010)	0.25 (0.010)	0.25 (0.010)	0.25 (0.010)	0.25 (0.010)	0.25 (0.010)	0.76 (0.030)
max.	0.75 (0.030)	0.75 (0.030)	1.02 (0.040)	1.02 (0.040)	1.02 (0.040)	1.02 (0.040)	1.02 (0.040)	1.52 (0.060)

*Reflow Soldering Only

High Voltage MLC Chips

For 600V to 5000V Applications

C0G Dielectric

Performance Characteristics

Capacitance Range	10 pF to 0.047 µF (25°C, 1.0 ±0.2 Vrms at 1kHz, for ≤ 1000 pF use 1 MHz)
Capacitance Tolerances	±5%, ±10%, ±20%
Dissipation Factor	0.1% max. (+25°C, 1.0 ±0.2 Vrms, 1kHz, for ≤ 1000 pF use 1 MHz)
Operating Temperature Range	-55°C to +125°C
Temperature Characteristic	0 ±30 ppm/°C (0 VDC)
Voltage Ratings	600, 1000, 1500, 2000, 2500, 3000, 4000 & 5000 VDC (+125°C)
Insulation Resistance (+25°C, at 500 VDC)	100K MΩ min. or 1000 MΩ - µF min., whichever is less
Insulation Resistance (+125°C, at 500 VDC)	10K MΩ min. or 100 MΩ - µF min., whichever is less
Dielectric Strength	120% rated voltage for 5 seconds at 50 mA max. current

HIGH VOLTAGE C0G CAPACITANCE VALUES

VOLTAGE		1206	1210	1808	1812	1825	2220	2225	3640
600	min.	10 pF	100 pF	100 pF	100 pF	1000 pF	1000 pF	1000 pF	1000 pF
	max.	680 pF	1500 pF	2700 pF	5600 pF	0.012 µF	0.012 µF	0.015 µF	0.047 µF
1000	min.	10 pF	10 pF	100 pF	100 pF	100 pF	1000 pF	1000 pF	1000 pF
	max.	470 pF	820 pF	1500 pF	2700 pF	6800 pF	0.010 µF	0.010 µF	0.018 µF
1500	min.	10 pF	10 pF	10 pF	10 pF	100 pF	100 pF	100 pF	100 pF
	max.	150 pF	330 pF	470 pF	1000 pF	2700 pF	2700 pF	3300 pF	8200 pF
2000	min.	10 pF	10 pF	10 pF	10 pF	100 pF	100 pF	100 pF	100 pF
	max.	68 pF	150 pF	270 pF	680 pF	1800 pF	2200 pF	2200 pF	5600 pF
2500	min.	—	—	10 pF	10 pF	10 pF	100 pF	100 pF	100 pF
	max.	—	—	150 pF	390 pF	1000 pF	1000 pF	1200 pF	3900 pF
3000	min.	—	—	10 pF	10 pF	10 pF	10 pF	10 pF	100 pF
	max.	—	—	100 pF	330 pF	680 pF	680 pF	820 pF	2200 pF
4000	min.	—	—	10 pF	10 pF	10 pF	10 pF	10 pF	100 pF
	max.	—	—	39 pF	100 pF	220 pF	220 pF	330 pF	1000 pF
5000	min.	—	—	—	—	—	—	—	10 pF
	max.	—	—	—	—	—	—	—	680 pF

X7R Dielectric

Performance Characteristics

Capacitance Range	10 pF to 0.56 µF (25°C, 1.0 ±0.2 Vrms at 1kHz)
Capacitance Tolerances	±10%; ±20%; +80%, -20%
Dissipation Factor	2.5% max. (+25°C, 1.0 ±0.2 Vrms, 1kHz)
Operating Temperature Range	-55°C to +125°C
Temperature Characteristic	±15% (0 VDC)
Voltage Ratings	600, 1000, 1500, 2000, 2500, 3000, 4000 & 5000 VDC (+125°C)
Insulation Resistance (+25°C, at 500 VDC)	100K MΩ min. or 1000 MΩ - µF min., whichever is less
Insulation Resistance (+125°C, at 500 VDC)	10K MΩ min. or 100 MΩ - µF min., whichever is less
Dielectric Strength	120% rated voltage for 5 seconds at 50 mA max. current

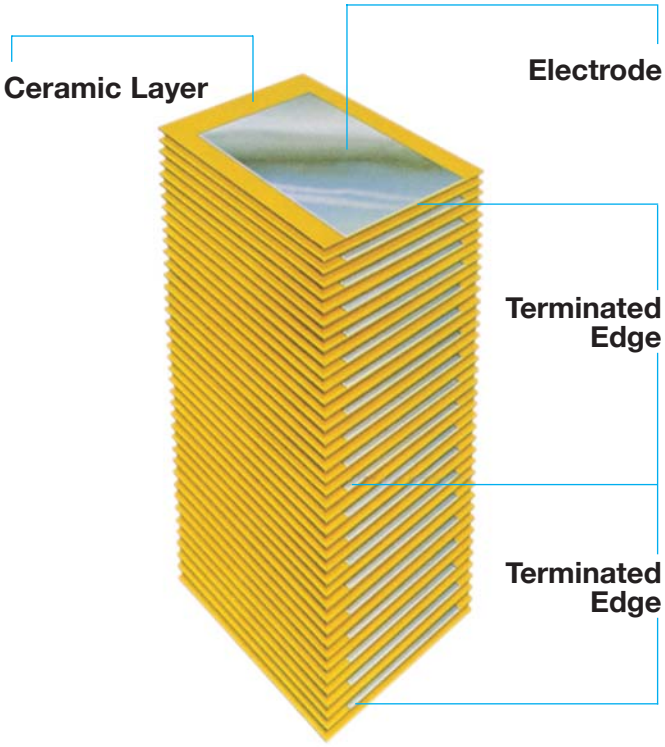
HIGH VOLTAGE X7R MAXIMUM CAPACITANCE VALUES

VOLTAGE		1206	1210	1808	1812	1825	2220	2225	3640
600	min.	1000 pF	1000 pF	1000 pF	1000 pF	0.01 µF	0.01 µF	0.01 µF	0.01 µF
	max.	0.015 µF	0.033 µF	0.056 µF	0.10 µF	0.18 µF	0.22 µF	0.22 µF	0.56 µF
1000	min.	100 pF	1000 pF	1000 pF	1000 pF	1000 pF	1000 pF	1000 pF	0.01 µF
	max.	5600 pF	0.015 µF	0.018 µF	0.027 µF	0.10 µF	0.10 µF	0.10 µF	0.22 µF
1500	min.	100 pF	100 pF	100 pF	100 pF	1000 pF	1000 pF	1000 pF	1000 pF
	max.	1800 pF	3900 pF	6800 pF	0.012 µF	0.033 µF	0.039 µF	0.047 µF	0.068 µF
2000	min.	10 pF	100 pF	100 pF	100 pF	100 pF	1000 pF	1000 pF	1000 pF
	max.	1000pF	2200 pF	2700 pF	4700 pF	0.01 µF	0.01 µF	0.015 µF	0.027 µF
2500	min.	—	—	10 pF	10 pF	100 pF	100 pF	100 pF	1000 pF
	max.	—	—	1800 pF	3300 pF	6800 pF	8200 pF	0.01 µF	0.022 µF
3000	min.	—	—	10 pF	10 pF	100 pF	100 pF	100 pF	1000 pF
	max.	—	—	1500 pF	2200 pF	4700 pF	4700 pF	6800 pF	0.018 µF
4000	min.	—	—	—	—	—	—	—	100 pF
	max.	—	—	—	—	—	—	—	6800 pF
5000	min.	—	—	—	—	—	—	—	100 pF
	max.	—	—	—	—	—	—	—	3300 pF

MLC Chip Capacitors

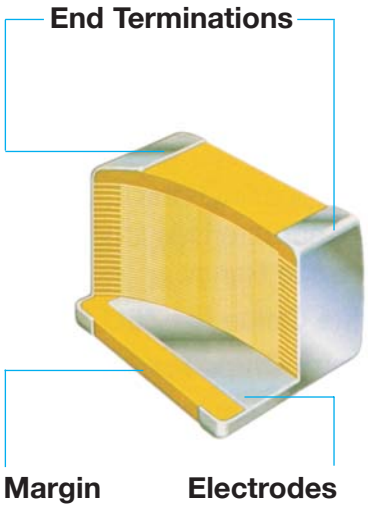
Basic Construction

A multilayer ceramic (MLC) capacitor is a monolithic block of ceramic containing two sets of offset, interleaved planar electrodes that extend to two opposite surfaces of the ceramic dielectric. This simple structure requires a considerable amount of sophistication, both in material and in manufacture, to produce it in the quality and quantities needed in today's electronic equipment.



Terminations

- Standard Nickel Barrier
  T = Lead Free Tin Plate
  J = 5% minimum Lead Plated
- Leach resistance to 90 seconds at 260°C
- Solderable plated for dimensional control
- Special materials as required



QUALITY STATEMENT

AVX focus is customer satisfaction – Customer satisfaction in the broadest sense: Products, service, price, delivery, technical support, and all the aspects of a business that impact you, the customer.

Our long term strategy is for continuous improvement which is defined by our Quality Vision 2000. This is a total quality management system developed by and supported by AVX corporate management. The foundation of QV2000 is built upon military and commercial standards and systems including ISO9001. QV2000 is a natural extension of past quality efforts with world class techniques for ensuring a total quality environment to satisfy our customers during this decade and into the 21st century.

As your components supplier, we invite you to experience the quality, service, and commitment of AVX.

Table 1: EIA and MIL Temperature Stable and General Application Codes

EIA CODE Percent Capacity Change Over Temperature Range	
RS198	**Temperature Range**
X7	-55°C to +125°C
X5	-55°C to +85°C
Y5	-30°C to +85°C
Z5	+10°C to +85°C
Code	**Percent Capacity Change**
D	±3.3%
E	±4.7%
F	±7.5%
P	±10%
R	±15%
S	±22%
T	+22%, -33%
U	+22%, - 56%
V	+22%, -82%

EXAMPLE – A capacitor is desired with the capacitance value at 25°C to increase no more than 7.5% or decrease no more than 7.5% from -30°C to +85°C. EIA Code will be Y5F.

MIL CODE		
Symbol	**Temperature Range**	
A	-55°C to +85°C	
B	-55°C to +125°C	
C	-55°C to +150°C	
Symbol	**Cap. Change Zero Volts**	**Cap. Change Rated Volts**
Q	+15%, -15%	+15%, -50%
R	+15%, -15%	+15%, -40%
W	+22%, -56%	+22%, -66%
X	+15%, -15%	+15%, -25%
Y	+30%, -70%	+30%, -80%
Z	+20%, -20%	+20%, -30%

Temperature characteristic is specified by combining range and change symbols, for example BR or AW. Specification slash sheets indicate the characteristic applicable to a given style of capacitor.

In specifying capacitance change with temperature for Class 2 materials, EIA expresses the capacitance change over an operating temperature range by a 3 symbol code. The first symbol represents the cold temperature end of the temperature range, the second represents the upper limit of the operating temperature range and the third symbol represents the capacitance change allowed over the operating temperature range. Table 1 provides a detailed explanation of the EIA system.

Effects of Voltage – Variations in voltage have little effect on Class 1 dielectric but does affect the capacitance and dissipation factor of Class 2 dielectrics. The application of DC voltage reduces both the capacitance and dissipation factor while the application of an AC voltage within a reasonable range tends to increase both capacitance and dissipation factor readings. If a high enough AC voltage is applied, eventually it will reduce capacitance just as a DC voltage will. Figure 2 shows the effects of AC voltage.

Cap. Change vs. A.C. Volts
X7R

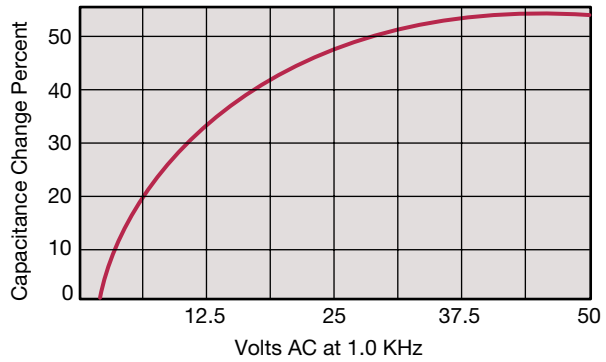


Figure 2

Capacitor specifications specify the AC voltage at which to measure (normally 0.5 or 1 VAC) and application of the wrong voltage can cause spurious readings.

Typical Cap. Change vs. Temperature
X7R

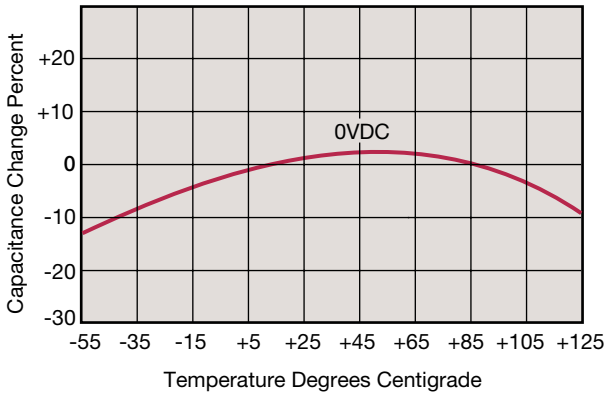


Figure 3

Effects of Time – Class 2 ceramic capacitors change capacitance and dissipation factor with time as well as temperature, voltage and frequency. This change with time is known as aging. Aging is caused by a gradual re-alignment of the crystalline structure of the ceramic and produces an exponential loss in capacitance and decrease in dissipation factor versus time. A typical curve of aging rate for semi-stable ceramics is shown in Figure 4.

If a Class 2 ceramic capacitor that has been sitting on the shelf for a period of time, is heated above its curie point, (125°C for 4 hours or 150°C for ½ hour will suffice) the part will de-age and return to its initial capacitance and dissipation factor readings. Because the capacitance changes rapidly, immediately after de-aging, the basic capacitance measurements are normally referred to a time period sometime after the de-aging process. Various manufacturers use different time bases but the most popular one is one day or twenty-four hours after "last heat." Change in the aging curve can be caused by the application of voltage and other stresses. The possible changes in capacitance due to de-aging by heating the unit explain why capacitance changes are allowed after test, such as temperature cycling, moisture resistance, etc., in MIL specs. The application of high voltages such as dielectric withstanding voltages also tends to de-age capacitors and is why re-reading of capacitance after 12 or 24 hours is allowed in military specifications after dielectric strength tests have been performed.

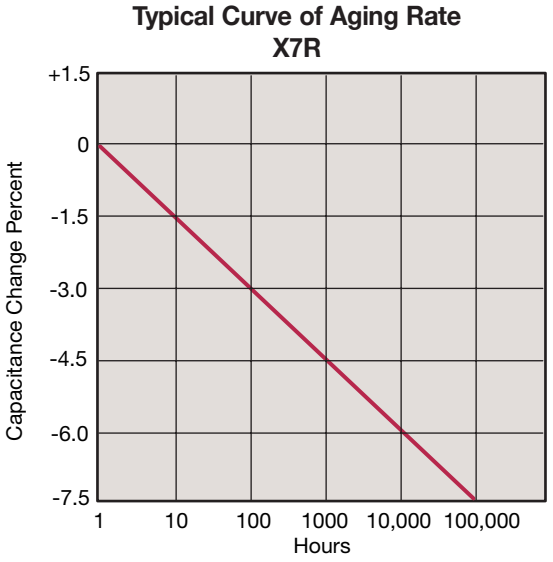


Figure 4

Effects of Frequency – Frequency affects capacitance and impedance characteristics of capacitors. This effect is much more pronounced in high dielectric constant ceramic formulation than in low K formulations. AVX's SpiCalci software generates impedance, ESR, series inductance, series resonant frequency and capacitance all as functions of frequency, temperature and DC bias for standard chip sizes and styles. It is available free from AVX and can be downloaded for free from AVX website: www.avx.com.

Effects of Mechanical Stress – High "K" dielectric ceramic capacitors exhibit some low level piezoelectric reactions under mechanical stress. As a general statement, the piezoelectric output is higher, the higher the dielectric constant of the ceramic. It is desirable to investigate this effect before using high "K" dielectrics as coupling capacitors in extremely low level applications.

Reliability – Historically ceramic capacitors have been one of the most reliable types of capacitors in use today. The approximate formula for the reliability of a ceramic capacitor is:

$$\frac{L_o}{L_t} = \left(\frac{V_t}{V_o}\right)^X \left(\frac{T_t}{T_o}\right)^Y$$

where

L_o = operating life
L_t = test life
V_t = test voltage
V_o = operating voltage
T_t = test temperature and
T_o = operating temperature in °C
X,Y = see text

Historically for ceramic capacitors exponent X has been considered as 3. The exponent Y for temperature effects typically tends to run about 8.

General Description

A capacitor is a component which is capable of storing electrical energy. It consists of two conductive plates (electrodes) separated by insulating material which is called the dielectric. A typical formula for determining capacitance is:

$$C = \frac{.224\ KA}{t}$$

C = capacitance (picofarads)
K = dielectric constant (Vacuum = 1)
A = area in square inches
t = separation between the plates in inches (thickness of dielectric)
.224 = conversion constant (.0884 for metric system in cm)

Capacitance – The standard unit of capacitance is the farad. A capacitor has a capacitance of 1 farad when 1 coulomb charges it to 1 volt. One farad is a very large unit and most capacitors have values in the micro (10^{-6}), nano (10^{-9}) or pico (10^{-12}) farad level.

Dielectric Constant – In the formula for capacitance given above the dielectric constant of a vacuum is arbitrarily chosen as the number 1. Dielectric constants of other materials are then compared to the dielectric constant of a vacuum.

Dielectric Thickness – Capacitance is indirectly proportional to the separation between electrodes. Lower voltage requirements mean thinner dielectrics and greater capacitance per volume.

Area – Capacitance is directly proportional to the area of the electrodes. Since the other variables in the equation are usually set by the performance desired, area is the easiest parameter to modify to obtain a specific capacitance within a material group.

Energy Stored – The energy which can be stored in a capacitor is given by the formula:

$$E = \tfrac{1}{2}CV^2$$

E = energy in joules (watts-sec)
V = applied voltage
C = capacitance in farads

Potential Change – A capacitor is a reactive component which reacts against a change in potential across it. This is shown by the equation for the linear charge of a capacitor:

$$I_{ideal} = C\frac{dV}{dt}$$

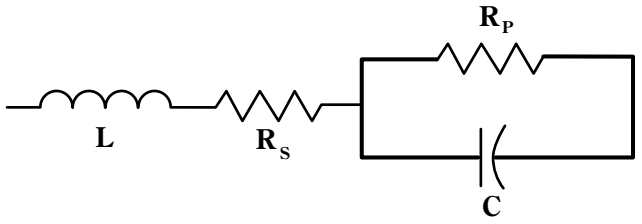
where

I = Current
C = Capacitance
dV/dt = Slope of voltage transition across capacitor

Thus an infinite current would be required to instantly change the potential across a capacitor. The amount of current a capacitor can "sink" is determined by the above equation.

Equivalent Circuit – A capacitor, as a practical device, exhibits not only capacitance but also resistance and inductance. A simplified schematic for the equivalent circuit is:

C = Capacitance **L** = Inductance
R_s = Series Resistance **R_p** = Parallel Resistance



Reactance – Since the insulation resistance (R_p) is normally very high, the total impedance of a capacitor is:

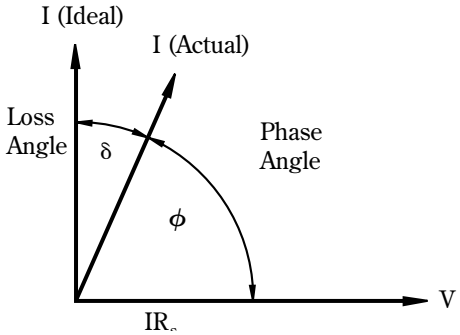
$$Z = \sqrt{R_S^2 + (X_C - X_L)^2}$$

where

Z = Total Impedance
R_s = Series Resistance
X_C = Capacitive Reactance = $\frac{1}{2\pi fC}$
X_L = Inductive Reactance = $2\pi fL$

The variation of a capacitor's impedance with frequency determines its effectiveness in many applications.

Phase Angle – Power Factor and Dissipation Factor are often confused since they are both measures of the loss in a capacitor under AC application and are often almost identical in value. In a "perfect" capacitor the current in the capacitor will lead the voltage by 90°.

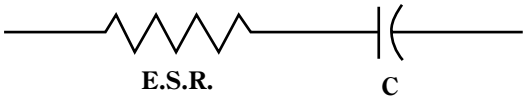


In practice the current leads the voltage by some other phase angle due to the series resistance R_S. The complement of this angle is called the loss angle and:

Power Factor (P.F.) = Cos ϕ or Sine δ
Dissipation Factor (D.F.) = tan δ

for small values of δ the tan and sine are essentially equal which has led to the common interchangeability of the two terms in the industry.

Equivalent Series Resistance – The term E.S.R. or Equivalent Series Resistance combines all losses both series and parallel in a capacitor at a given frequency so that the equivalent circuit is reduced to a simple R-C series connection.



Dissipation Factor – The DF/PF of a capacitor tells what percent of the apparent power input will turn to heat in the capacitor.

$$\textbf{Dissipation Factor} = \frac{\textbf{E.S.R.}}{\textbf{X}_c} = \textbf{(2 } \pi \textbf{ fC) (E.S.R.)}$$

The watts loss are:

Watts loss = (2 π fCV^2) (D.F.)

Very low values of dissipation factor are expressed as their reciprocal for convenience. These are called the "Q" or Quality factor of capacitors.

Parasitic Inductance – The parasitic inductance of capacitors is becoming more and more important in the decoupling of today's high speed digital systems. The relationship between the inductance and the ripple voltage induced on the DC voltage line can be seen from the simple inductance equation:

$$V = L \frac{di}{dt}$$

The $\frac{di}{dt}$ seen in current microprocessors can be as high as 0.3 A/ns, and up to 10A/ns. At 0.3 A/ns, 100pH of parasitic inductance can cause a voltage spike of 30mV. While this does not sound very drastic, with the Vcc for microprocessors decreasing at the current rate, this can be a fairly large percentage.

Another important, often overlooked, reason for knowing the parasitic inductance is the calculation of the resonant frequency. This can be important for high frequency, by-pass capacitors, as the resonant point will give the most signal attenuation. The resonant frequency is calculated from the simple equation:

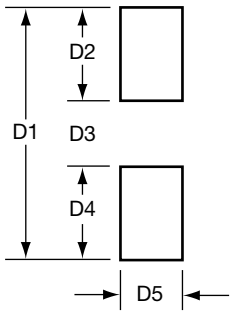
$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

Insulation Resistance – Insulation Resistance is the resistance measured across the terminals of a capacitor and consists principally of the parallel resistance R_P shown in the equivalent circuit. As capacitance values and hence the area of dielectric increases, the I.R. decreases and hence the product (C x IR or RC) is often specified in ohm farads or more commonly megohm-microfarads. Leakage current is determined by dividing the rated voltage by IR (Ohm's Law).

Dielectric Strength – Dielectric Strength is an expression of the ability of a material to withstand an electrical stress. Although dielectric strength is ordinarily expressed in volts, it is actually dependent on the thickness of the dielectric and thus is also more generically a function of volts/mil.

Dielectric Absorption – A capacitor does not discharge instantaneously upon application of a short circuit, but drains gradually after the capacitance proper has been discharged. It is common practice to measure the dielectric absorption by determining the "reappearing voltage" which appears across a capacitor at some point in time after it has been fully discharged under short circuit conditions.

Corona – Corona is the ionization of air or other vapors which causes them to conduct current. It is especially prevalent in high voltage units but can occur with low voltages as well where high voltage gradients occur. The energy discharged degrades the performance of the capacitor and can in time cause catastrophic failures.



SOLDER PAD DESIGN

millimeters (inches)

Case Size	D1	D2	D3	D4	D5
0805	3.00 (0.120)	1.00 (0.040)	1.00 (0.040)	1.00 (0.040)	1.25 (0.050)
1206	4.00 (0.160)	1.00 (0.040)	2.00 (0.090)	1.00 (0.040)	1.60 (0.060)
1210	4.00 (0.160)	1.00 (0.040)	2.00 (0.090)	1.00 (0.040)	2.50 (0.100)
***1808**	5.60 (0.220)	1.00 (0.040)	3.60 (0.140)	1.00 (0.040)	2.00 (0.080)
***1812**	5.60 (0.220)	1.00 (0.040)	3.60 (0.140)	1.00 (0.040)	3.00 (0.120)
***1825**	5.60 (0.220)	1.00 (0.040)	3.60 (0.140)	1.00 (0.040)	6.35 (0.250)
***2220**	6.60 (0.260)	1.00 (0.040)	4.60 (0.180)	1.00 (0.040)	5.00 (0.200)
***2225**	6.60 (0.260)	1.00 (0.040)	4.60 (0.180)	1.00 (0.040)	6.35 (0.250)
***HQCC**	6.60 (0.260)	1.00 (0.040)	4.60 (0.180)	1.00 (0.040)	6.35 (0.250)
***3640**	10.67 (0.427)	1.52 (0.060)	7.62 (0.300)	1.52 (0.060)	10.16 (0.400)
***HQCE**	10.67 (0.427)	1.52 (0.060)	7.62 (0.300)	1.52 (0.060)	10.16 (0.400)

*AVX recommends reflow soldering only.

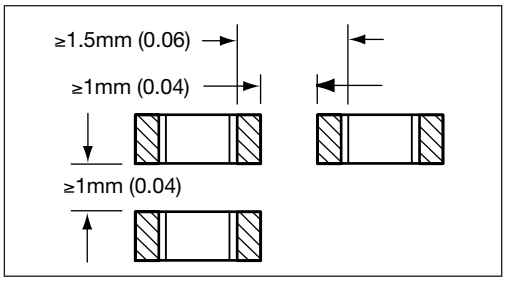
Component Pad Design

Component pads should be designed to achieve good solder filets and minimize component movement during reflow soldering. Pad designs are given for the most common sizes of multilayer ceramic capacitors for both wave and reflow soldering. The basis of these designs is:

- Pad width equal to component width. It is permissible to decrease this to as low as 85% of component width but it is not advisable to go below this.
- Pad overlap 0.5mm beneath component.
- Pad extension 0.5mm beyond components for reflow and 1.0mm for wave soldering.

Component Spacing

For wave soldering components, must be spaced sufficiently far apart to avoid bridging or shadowing (inability of solder to penetrate properly into small spaces). This is less important for reflow soldering but sufficient space must be allowed to enable rework should it be required.



Preheat & Soldering

The rate of preheat should not exceed 4°C/second to prevent thermal shock. A better maximum figure is about 2°C/second.

For capacitors size 1206 and below, with a maximum thickness of 1.25mm, it is generally permissible to allow a temperature differential from preheat to soldering of 150°C. In all other cases this differential should not exceed 100°C.

For further specific application or process advice, please consult AVX.

Cleaning

Care should be taken to ensure that the capacitors are thoroughly cleaned of flux residues especially the space beneath the capacitor. Such residues may otherwise become conductive and effectively offer a low resistance bypass to the capacitor.

Ultrasonic cleaning is permissible, the recommended conditions being 8 Watts/litre at 20-45 kHz, with a process cycle of 2 minutes vapor rinse, 2 minutes immersion in the ultrasonic solvent bath and finally 2 minutes vapor rinse.

APPLICATION NOTES

Storage
Good solderability is maintained for at least twelve months, provided the components are stored in their "as received" packaging at less than 40°C and 70% RH.

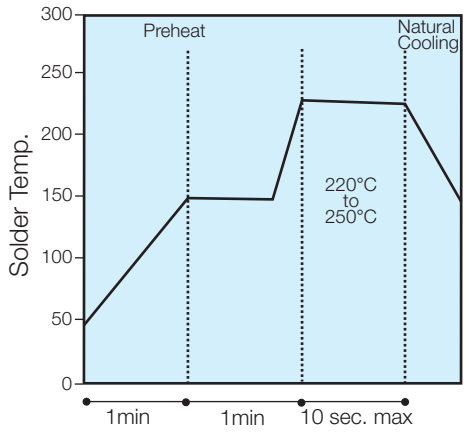
Solderability
Terminations to be well soldered after immersion in a 60/40 tin/lead solder bath at 235 ± 5°C for 2 ± 1 seconds.

Leaching
Terminations will resist leaching for at least the immersion times and conditions shown below.

Termination Type	Solder Tin/Lead/Silver	Solder Temp. °C	Immersion Time Seconds
Nickel Barrier	60/40/0	260 ± 5	30 ± 1

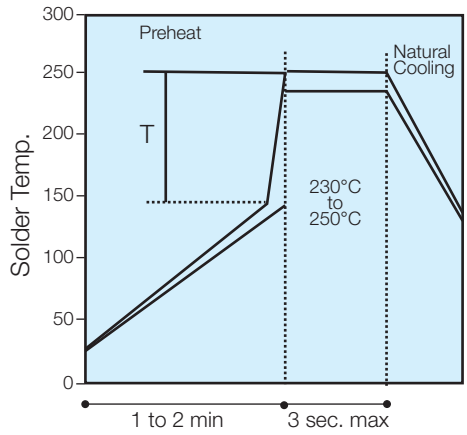
Recommended Soldering Profiles

Reflow



(Minimize soldering time)

Wave



(Preheat chips before soldering)
T/maximum 150°C

General
Surface mounting chip multilayer ceramic capacitors are designed for soldering to printed circuit boards or other substrates. The construction of the components is such that they will withstand the time/temperature profiles used in both wave and reflow soldering methods.

Handling
Chip multilayer ceramic capacitors should be handled with care to avoid damage or contamination from perspiration and skin oils. The use of tweezers or vacuum pick ups is strongly recommended for individual components. Bulk handling should ensure that abrasion and mechanical shock are minimized. Taped and reeled components provides the ideal medium for direct presentation to the placement machine. Any mechanical shock should be minimized during handling chip multilayer ceramic capacitors.

Preheat
It is important to avoid the possibility of thermal shock during soldering and carefully controlled preheat is therefore required. The rate of preheat should not exceed 4°C/second and a target figure 2°C/second is recommended. Although an 80°C to 120°C temperature differential is preferred, recent developments allow a temperature differential between the component surface and the soldering temperature of 150°C (Maximum) for capacitors of 1210 size and below with a maximum thickness of 1.25mm. The user is cautioned that the risk of thermal shock increases as chip size or temperature differential increases.

Soldering
Mildly activated rosin fluxes are preferred. The minimum amount of solder to give a good joint should be used. Excessive solder can lead to damage from the stresses caused by the difference in coefficients of expansion between solder, chip and substrate. AVX terminations are suitable for all wave and reflow soldering systems. If hand soldering cannot be avoided, the preferred technique is the utilization of hot air soldering tools.

Cooling
Natural cooling in air is preferred, as this minimizes stresses within the soldered joint. When forced air cooling is used, cooling rate should not exceed 4°C/second. Quenching is not recommended but if used, maximum temperature differentials should be observed according to the preheat conditions above.

Cleaning
Flux residues may be hygroscopic or acidic and must be removed. AVX MLC capacitors are acceptable for use with all of the solvents described in the specifications MIL-STD-202 and EIA-RS-198. Alcohol based solvents are acceptable and properly controlled water cleaning systems are also acceptable. Many other solvents have been proven successful, and most solvents that are acceptable to other components on circuit assemblies are equally acceptable for use with ceramic capacitors.

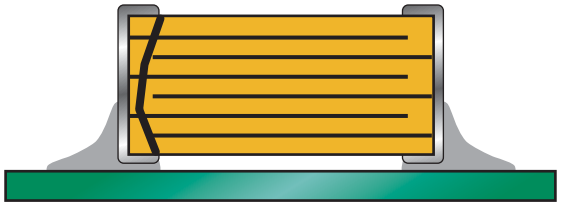
POST SOLDER HANDLING

Once SMP components are soldered to the board, any bending or flexure of the PCB applies stresses to the soldered joints of the components. For leaded devices, the stresses are absorbed by the compliancy of the metal leads and generally don't result in problems unless the stress is large enough to fracture the soldered connection.

Ceramic capacitors are more susceptible to such stress because they don't have compliant leads and are brittle in nature. The most frequent failure mode is low DC resistance or short circuit. The second failure mode is significant loss of capacitance due to severing of contact between sets of the internal electrodes.

Cracks caused by mechanical flexure are very easily identified and generally take one of the following two general forms:

Type A:
Angled crack between bottom of device to top of solder joint.



Type B:
Fracture from top of device to bottom of device.

Mechanical cracks are often hidden underneath the termination and are difficult to see externally. However, if one end termination falls off during the removal process from PCB, this is one indication that the cause of failure was excessive mechanical stress due to board warping.

COMMON CAUSES OF MECHANICAL CRACKING

The most common source for mechanical stress is board depanelization equipment, such as manual breakapart, v-cutters and shear presses. Improperly aligned or dull cutters may cause torqueing of the PCB resulting in flex stresses being transmitted to components near the board edge. Another common source of flexural stress is contact during parametric testing when test points are probed. If the PCB is allowed to flex during the test cycle, nearby ceramic capacitors may be broken.

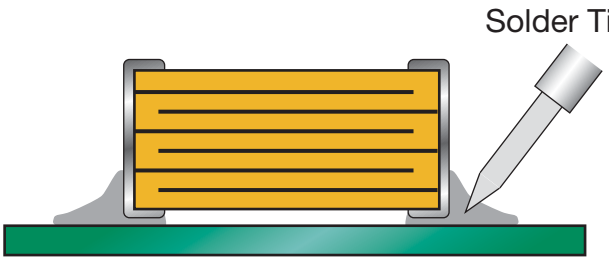
A third common source is board to board connections at vertical connectors where cables or other PCBs are connected to the PCB. If the board is not supported during the plug/unplug cycle, it may flex and cause damage to nearby components.

Special care should also be taken when handling large (>6" on a side) PCBs since they more easily flex or warp than smaller boards.

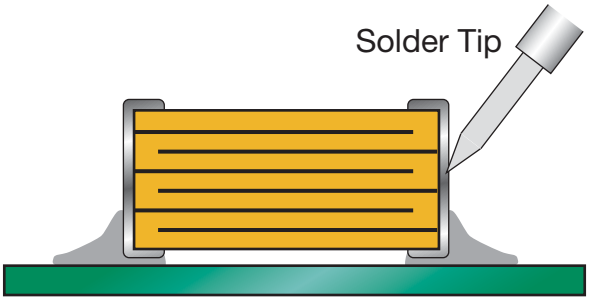
REWORKING OF MLCs

Thermal shock is common in MLCs that are manually attached or reworked with a soldering iron. *AVX strongly recommends that any reworking of MLCs be done with hot air reflow rather than soldering irons.* It is practically impossible to cause any thermal shock in ceramic capacitors when using hot air reflow.

However direct contact by the soldering iron tip often causes thermal cracks that may fail at a later date. If rework by soldering iron is absolutely necessary, it is recommended that the wattage of the iron be less than 30 watts and the tip temperature be <300ºC. *Rework should be performed by applying the solder iron tip to the pad and not directly contacting any part of the ceramic capacitor.*



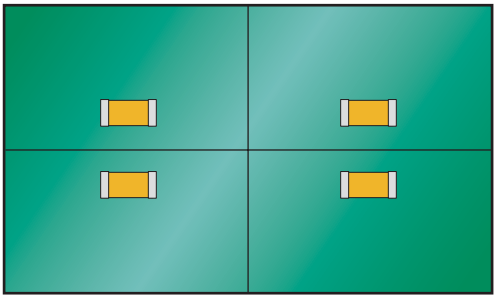
Preferred Method - No Direct Part Contact



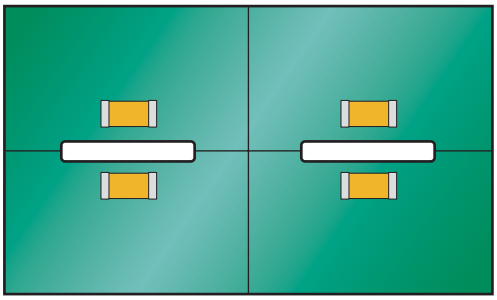
Poor Method - Direct Contact with Part

PCB BOARD DESIGN

To avoid many of the handling problems, AVX recommends that MLCs be located at least .2" away from nearest edge of board. However when this is not possible, AVX recommends that the panel be routed along the cut line, adjacent to where the MLC is located.



No Stress Relief for MLCs



Routed Cut Line Relieves Stress on MLC

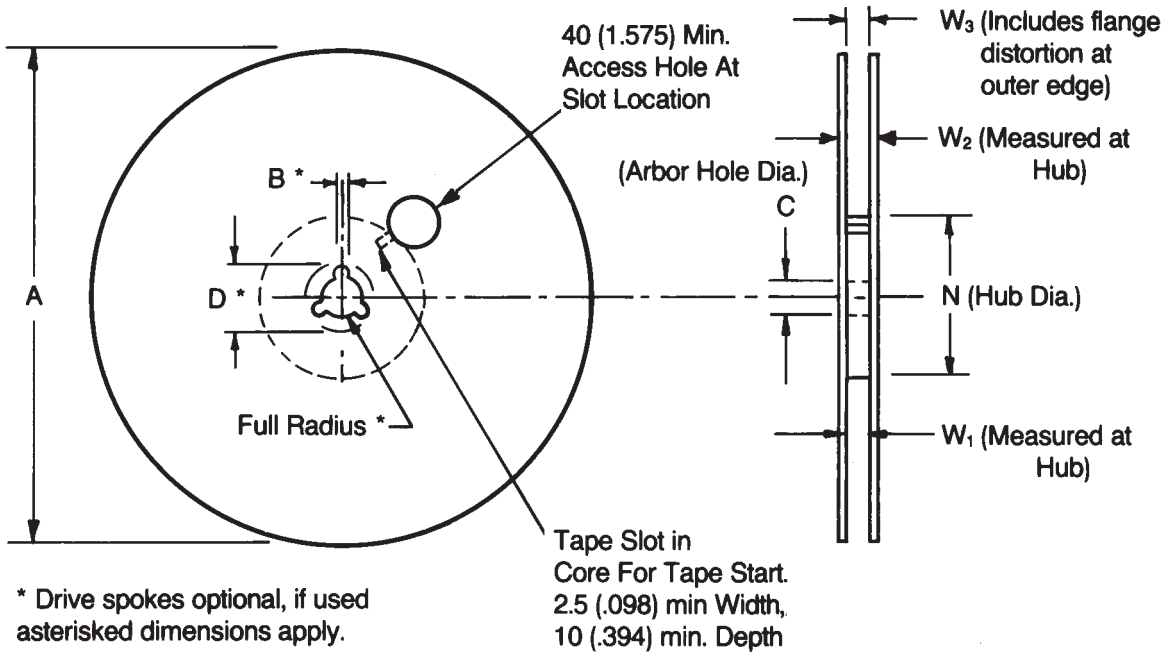
AUTOMATIC INSERTION PACKAGING

TAPE & REEL QUANTITIES

All tape and reel specifications are in compliance with EIA481 or IEC-286-3.

	8mm	12mm		24mm
	0805 1206 1210	1808	1812, 1825 2220, 2225, HQCC	3640 HQCE
Qty. per Reel/7" Reel	2000	2000	1000	N/A
Qty. per Reel/13" Reel	10,000	4000	4000	1000

REEL DIMENSIONS



DIMENSIONS

millimeters (inches)

Tape Size	A Max.	B* Min.	C	D* Min.	N Min.	W_1	W_2 Max.	W_3
8mm	330 (12.992)	1.5 (0.059)	13.0±0.20 (0.512±0.008)	20.2 (0.795)	50 (1.969)	$8.4^{+1.5}_{-0.0}$ $(0.331^{+.060}_{-0.0})$	14.4 (0.567)	7.9 Min. (0.311) 10.9 Max. (0.429)
12mm	330 (12.992)	1.5 (0.059)	13.0±0.20 (0.512±0.008)	20.2 (0.795)	50 (1.969)	$12.4^{+2.0}_{-0.0}$ $(0.488^{+.079}_{-0.0})$	18.4 (0.724)	11.9 Min. (0.469) 15.4 Max. (0.607)
24mm	360 (14.173)	1.5 (0.059)	$13.0^{+0.5}_{-0.2}$ $(0.512^{+.020}_{-.008})$	20.2 (0.795)	60 (2.362)	$24.4^{+2.0}_{-0.0}$ $(0.961^{+.079}_{-0.0})$	30.4 (1.197)	23.9 Min. (0.941) 27.4 Max. (1.079)