

CMOS 32K x 8 ZEROPOWER SRAM

PRELIMINARY DATA

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
 - M48Z35: $4.5V \leq V_{PFD} \leq 4.75V$
 - M48Z35Y: $4.2V \leq V_{PFD} \leq 4.5V$
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY
- SNAPHAT HOUSING (BATTERY) REPLACEABLE
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 32K x 8 SRAMs

DESCRIPTION

The M48Z35 ZEROPOWER® RAM is an 32K x 8 non-volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A14	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
$\bar{W}$	Write Enable
V _{CC}	Supply Voltage
V _{SS}	Ground

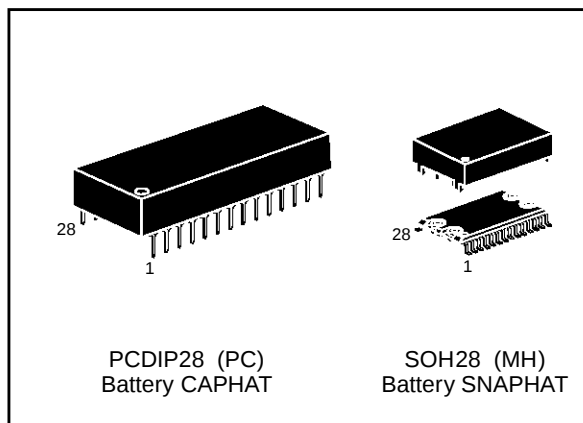


Figure 1. Logic Diagram

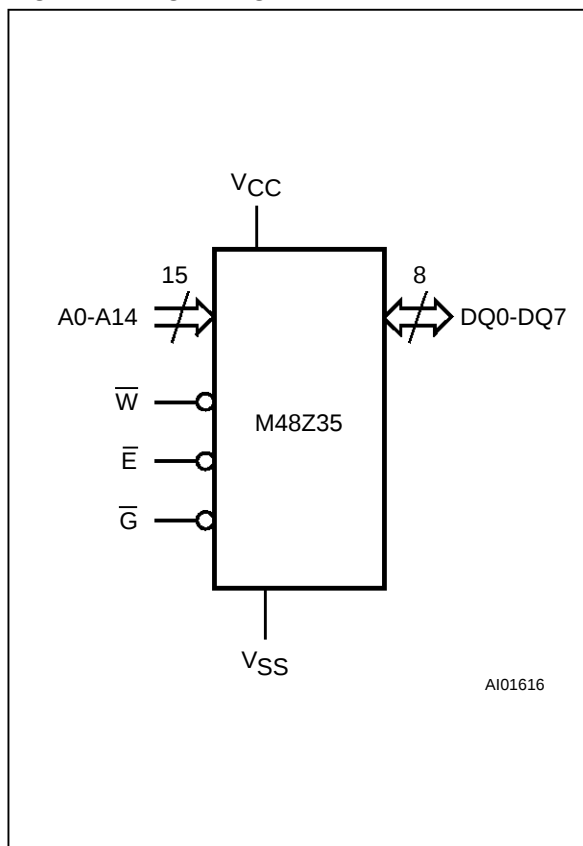


Figure 2A. DIP Pin Connections

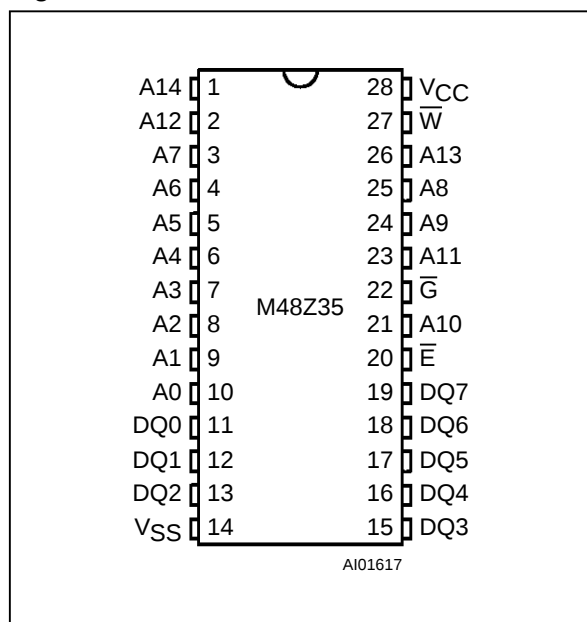


Figure 2B. SO Pin Connections

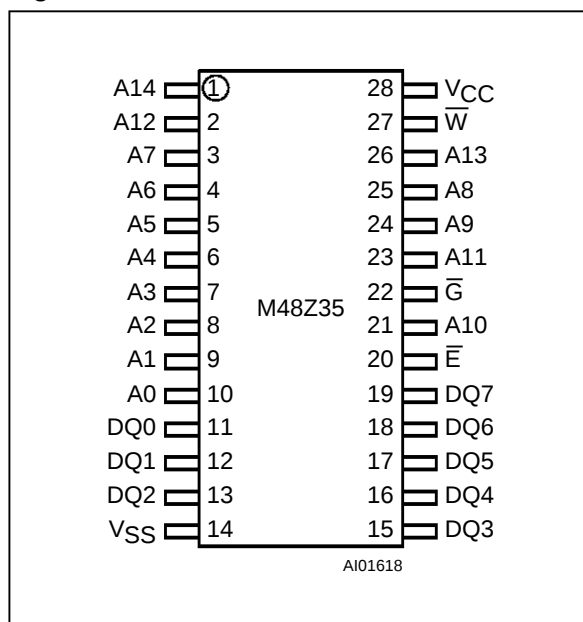


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	-40 to 85	°C
V_{IO}	Input or Output Voltages	-0.3 to 7	V
V_{CC}	Supply Voltage	-0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.

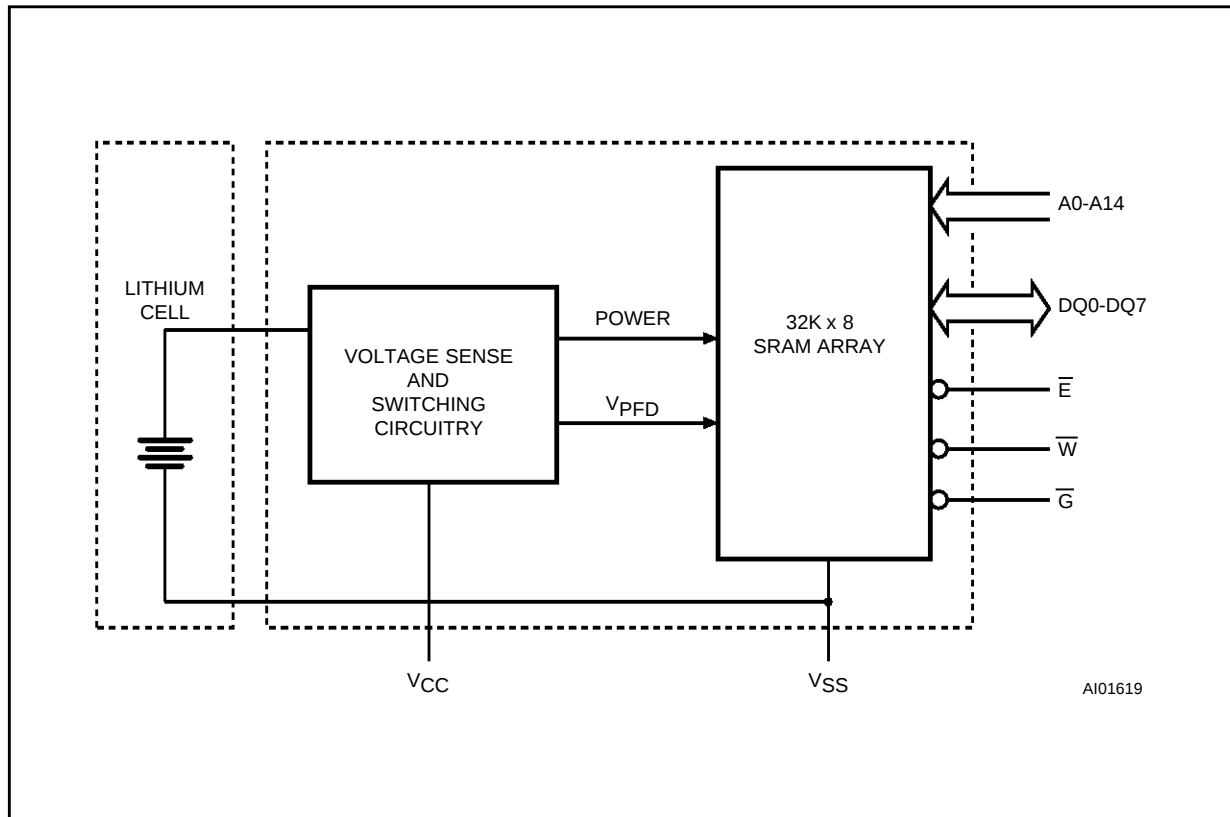
Table 3. Operating Modes ⁽¹⁾

Mode	V_{CC}	$\bar{E}$	$\bar{G}$	$\bar{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) ⁽²⁾	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Notes: 1. X = V_{IH} or V_{IL} .

2. See Table 6 for details.

Figure 3. Block Diagram

**DESCRIPTION (cont'd)**

The M48Z35 is a non-volatile pin and function equivalent to any JEDEC standard 32K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48Z35 silicon with a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

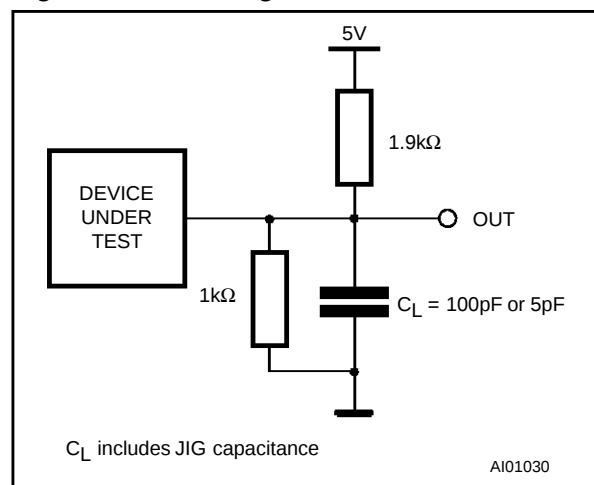


Table 4. Capacitance ^(1, 2) ($T_A = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		10	pF
$C_{IO}^{(3)}$	Input / Output Capacitance	$V_{OUT} = 0V$		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.

2. Sampled only, not 100% tested.

3. Outputs deselected.

Table 5. DC Characteristics ($T_A = 0\text{ to }70^{\circ}\text{C}$; $V_{CC} = 4.75V\text{ to }5.5V\text{ or }4.5V\text{ to }5.5V$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		± 1	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		± 5	μA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\bar{E} = V_{CC} - 0.2V$		3	mA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -1mA$	2.4		V

Table 6. Power Down/Up Trip Points DC Characteristics ⁽¹⁾ ($T_A = 0\text{ to }70^{\circ}\text{C}$)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z35)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z35Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
$t_{DR}^{(2)}$	Expected Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS} .

2. @ $25\text{ }^{\circ}\text{C}$

DESCRIPTION (cont'd)

For the 28 lead SO, the battery package (i.e. SNAPBAT) part number is "M4Z28-BR00SH1".

The M48Z35 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition.

When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC} . As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

Table 7. Power Down/Up Mode AC Characteristics ($T_A = 0$ to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\bar{E}$ or $\bar{W}$ at V_{IH} before Power Down	0		μs
$t_F^{(1)}$	$V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ V_{CC} Fall Time	300		μs
$t_{FB}^{(2)}$	$V_{PFD}(\text{min})$ to V_{SO} V_{CC} Fall Time	10		μs
t_R	$V_{PFD}(\text{min})$ to $V_{PFD}(\text{max})$ V_{CC} Rise Time	10		μs
t_{RB}	V_{SO} to $V_{PFD}(\text{min})$ V_{CC} Rise Time	1		μs
t_{REC}	$V_{PFD}(\text{max})$ to Inputs Recognized	40	200	ms

Notes: 1. $V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ fall time of less than t_F may result in deselection/write protection not occurring until 200 μs after V_{CC} passes $V_{PFD}(\text{min})$.
 2. $V_{PFD}(\text{min})$ to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

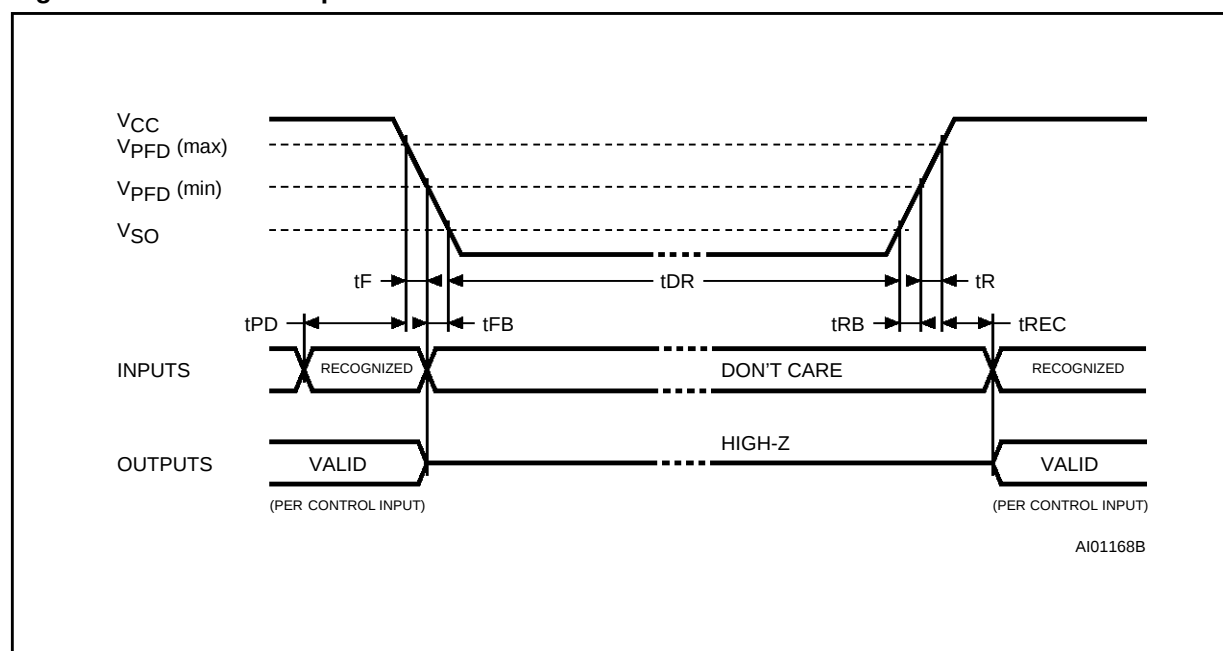
Figure 5. Power Down/Up Mode AC Waveforms

Table 8. Read Mode AC Characteristics(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z35 / 35Y		Unit
		-70		
		Min	Max	
t _{AVAV}	Read Cycle Time	70		ns
t _{AVQV} ⁽¹⁾	Address Valid to Output Valid		70	ns
t _{ELQV} ⁽¹⁾	Chip Enable Low to Output Valid		70	ns
t _{GLQV} ⁽¹⁾	Output Enable Low to Output Valid		35	ns
t _{ELQX} ⁽²⁾	Chip Enable Low to Output Transition	5		ns
t _{GLQX} ⁽²⁾	Output Enable Low to Output Transition	5		ns
t _{EHQZ} ⁽²⁾	Chip Enable High to Output Hi-Z		25	ns
t _{GHQZ} ⁽²⁾	Output Enable High to Output Hi-Z		25	ns
t _{AXQX} ⁽¹⁾	Address Transition to Output Transition	10		ns

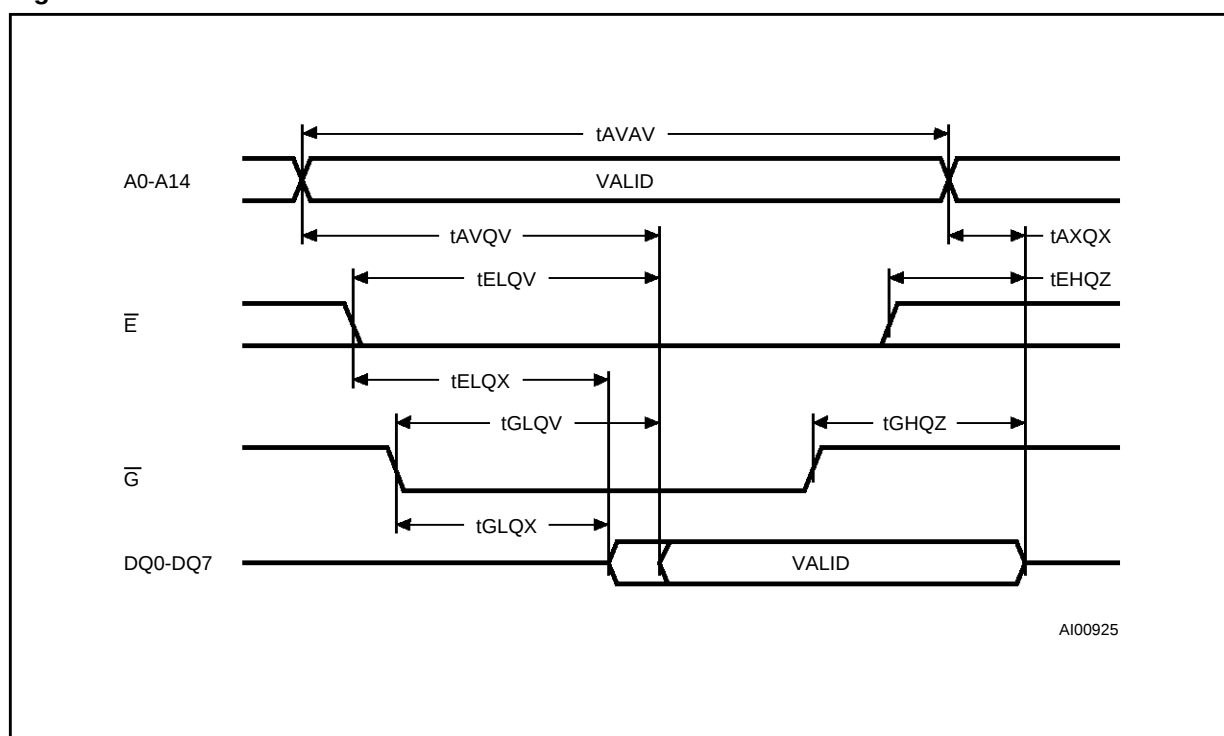
Notes: 1. C_L = 100pF (see Figure 4).2. C_L = 5pF (see Figure 4).**Figure 6. Read Mode AC Waveforms**Note: Write Enable ($\overline{W}$) = High.

Table 9. Write Mode AC Characteristics(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z35 / 35Y		Unit
		-70		
		Min	Max	
t _{AVAV}	Write Cycle Time	70		ns
t _{AVWL}	Address Valid to Write Enable Low	0		ns
t _{AVEL}	Address Valid to Chip Enable Low	0		ns
t _{WLWH}	Write Enable Pulse Width	50		ns
t _{LEH}	Chip Enable Low to Chip Enable High	55		ns
t _{WHAX}	Write Enable High to Address Transition	0		ns
t _{EHAX}	Chip Enable High to Address Transition	0		ns
t _{DVWH}	Input Valid to Write Enable High	30		ns
t _{DVEH}	Input Valid to Chip Enable High	30		ns
t _{WHDX}	Write Enable High to Input Transition	5		ns
t _{EHDX}	Chip Enable High to Input Transition	5		ns
t _{WLQZ} ^(1, 2)	Write Enable Low to Output Hi-Z		25	ns
t _{AVWH}	Address Valid to Write Enable High	60		ns
t _{AVEH}	Address Valid to Chip Enable High	60		ns
t _{WHQX} ^(1, 2)	Write Enable High to Output Transition	5		ns

Notes: 1. C_L = 5pF (see Figure 4).2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.**READ MODE**

The M48Z35 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 264,144 locations in the static storage array. Thus, the unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output

data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z35 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

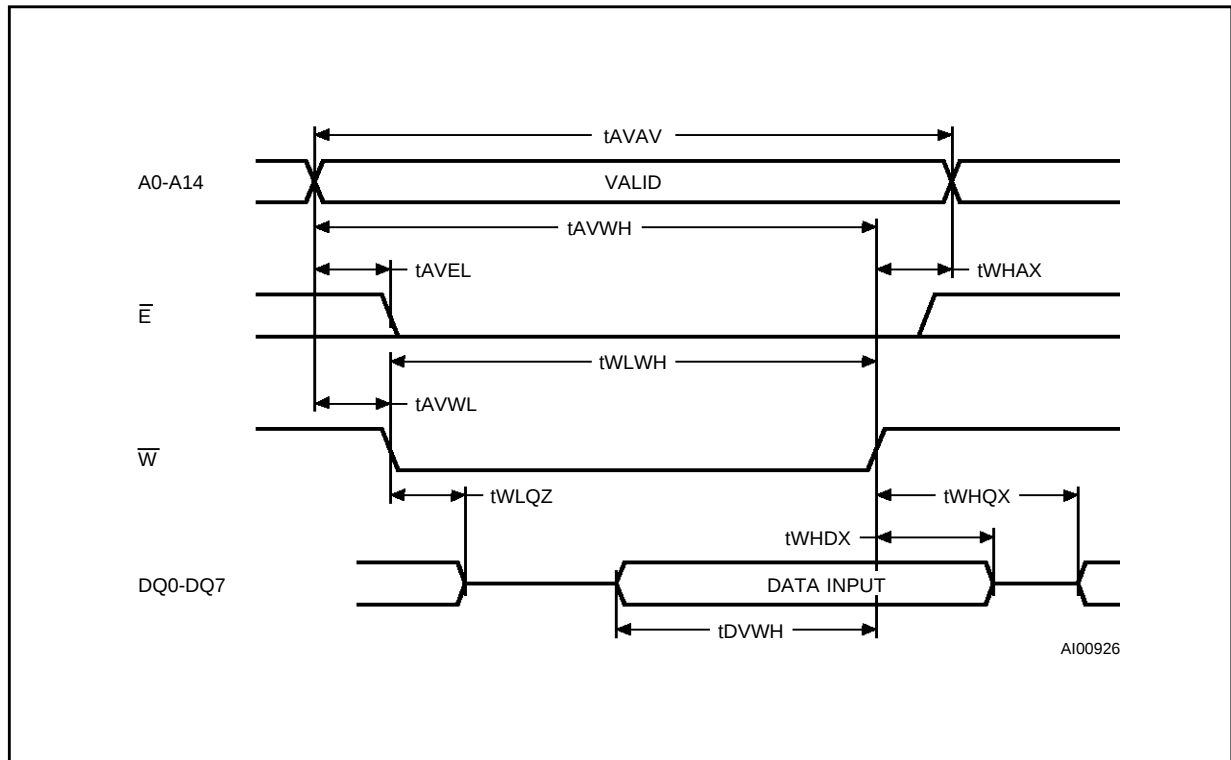
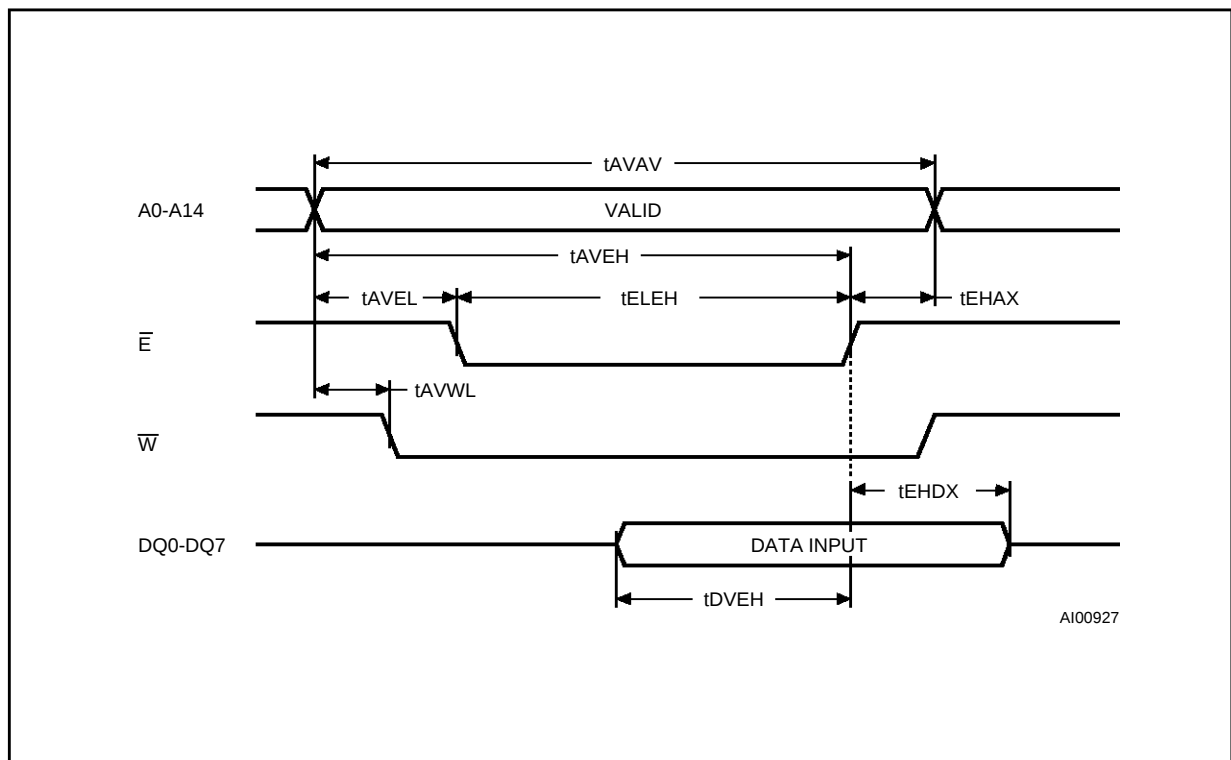


Figure 8. Chip Enable Controlled, Write AC Waveforms



DATA RETENTION MODE

With valid V_{CC} applied, the M48Z35 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the $V_{PFD(max)}$, $V_{PFD(min)}$ window. All outputs become high impedance, and all inputs are treated as "don't care."

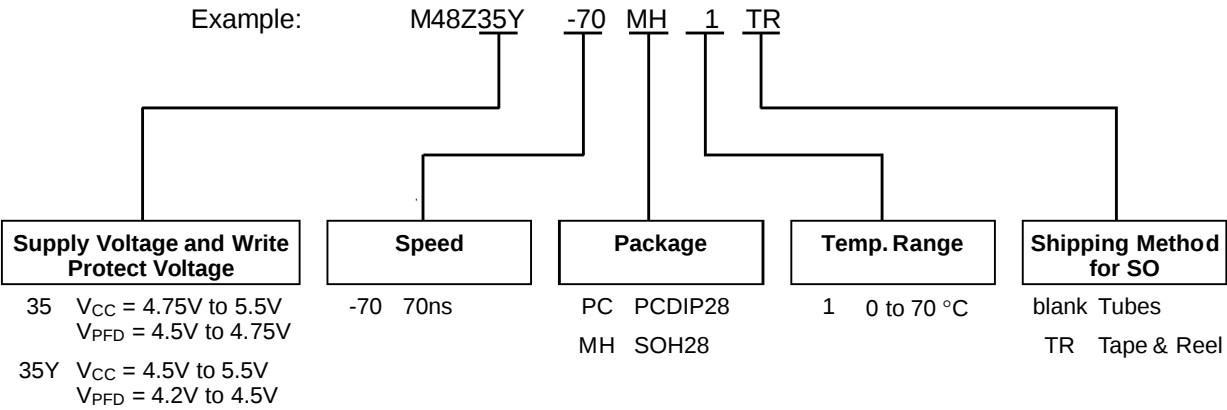
Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below $V_{PFD(min)}$, the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F . The M48Z35 may respond to transient noise spikes on

V_{CC} that reach into the deselect window during the time the device is sampling V_{CC} . Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO} , the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z35 for an accumulated period of at least 10 years when V_{CC} is less than V_{SO} .

As system power returns and V_{CC} rises above V_{SO} , the battery is disconnected, and the power supply is switched to external V_{CC} . Write protection continues for t_{REC} until V_{CC} reaches $V_{PFD(min)}$. Normal RAM operation can resume t_{REC} after V_{CC} exceeds $V_{PFD(max)}$.

ORDERING INFORMATION SCHEME



The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

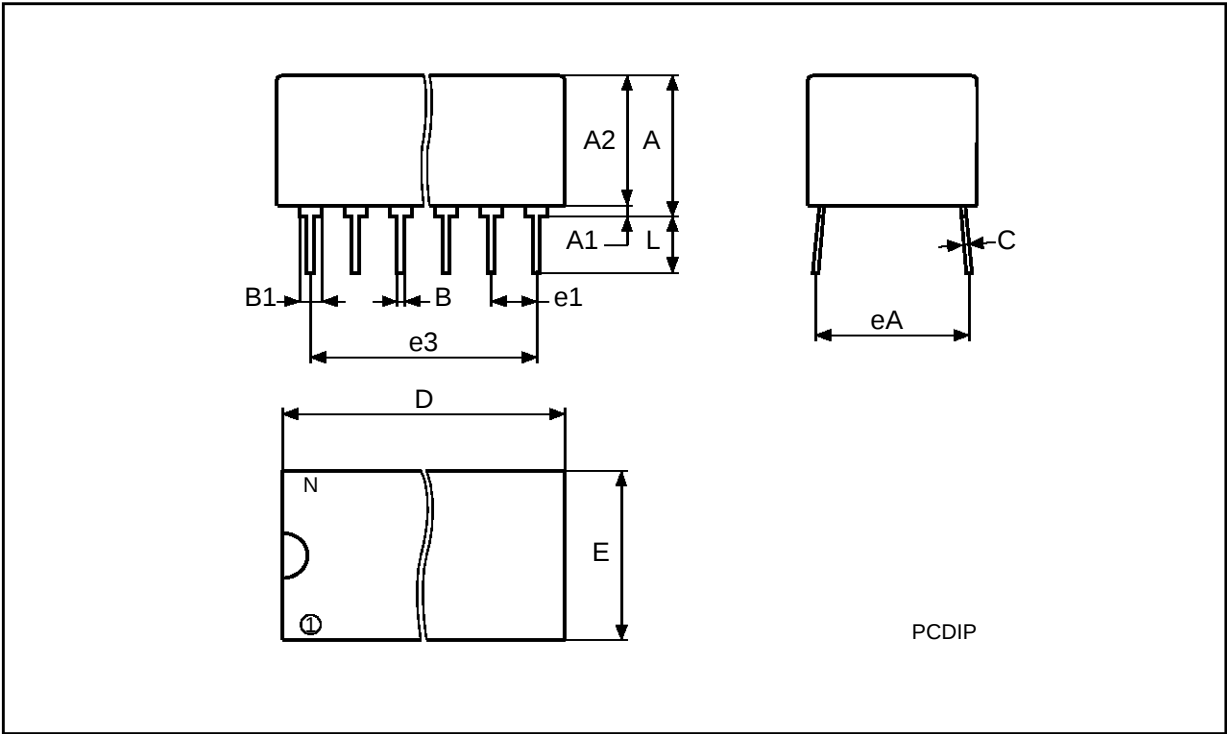
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28

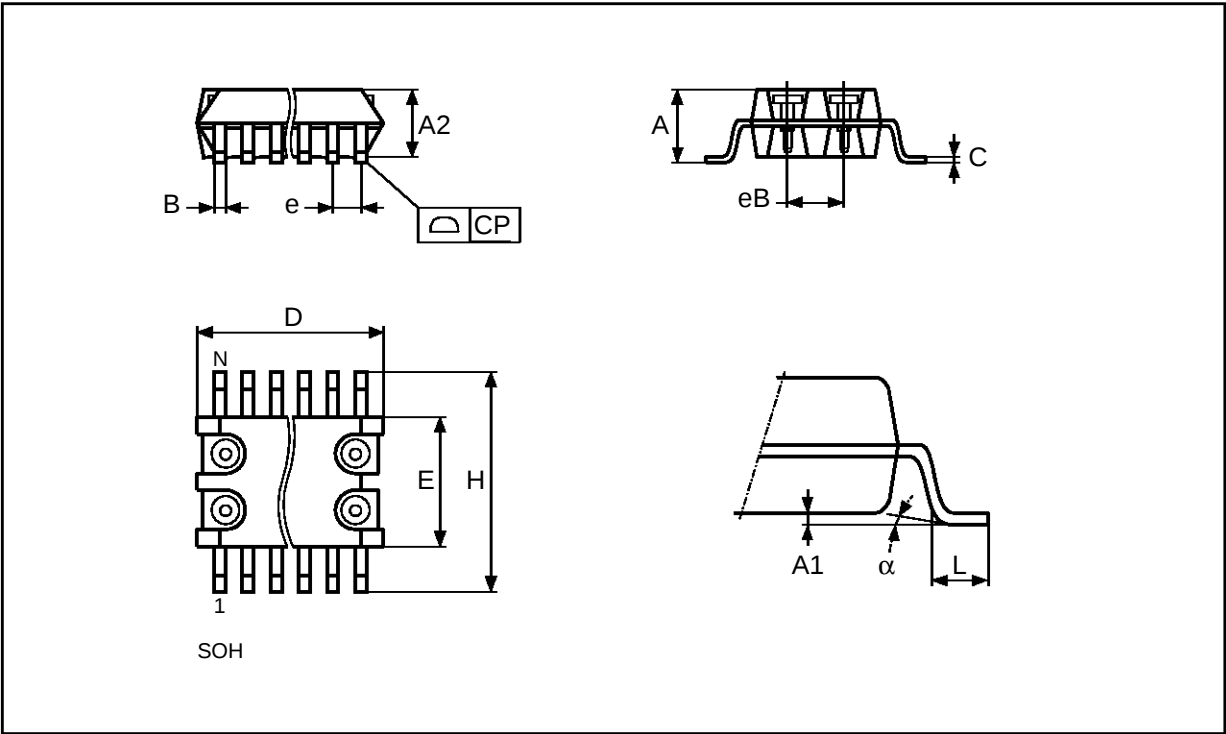


Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	—	—	0.050	—	—
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28

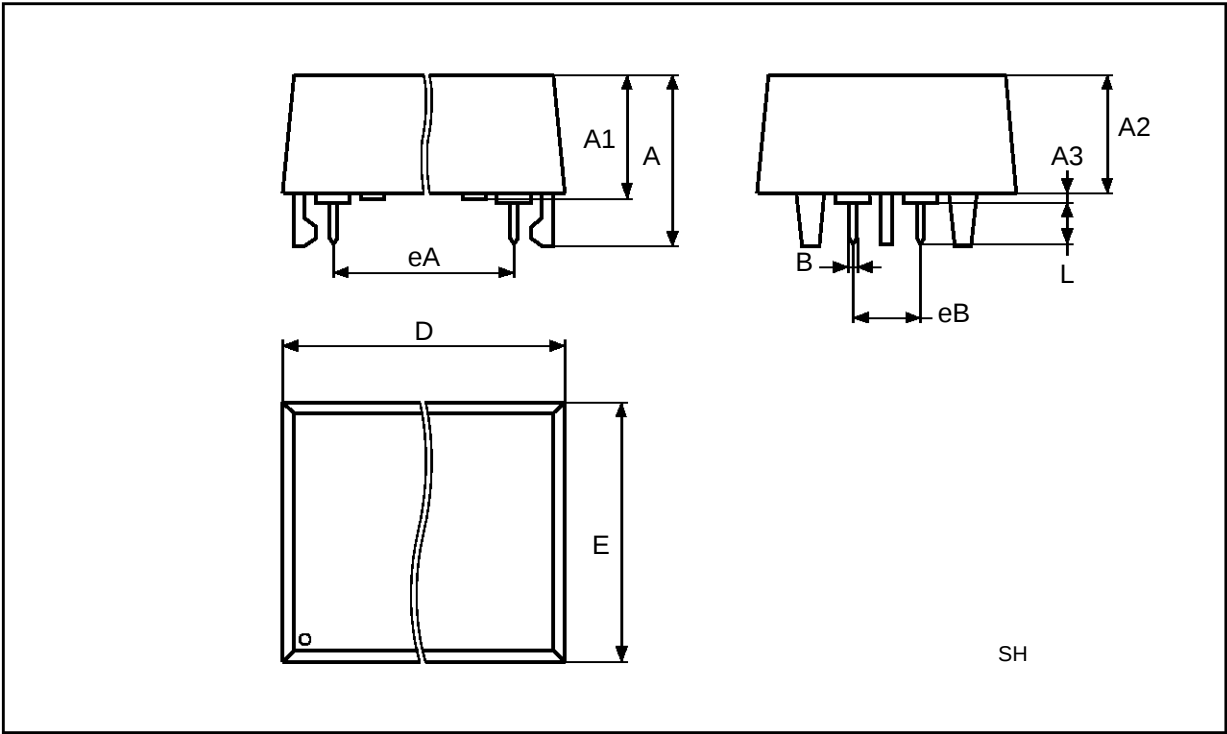


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SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28



Drawing is not to scale

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